Serial ATA International Organization:

Serial ATA Interoperability Program Unified Test Document Revision 1.01

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Revision History

Revision	Date	Comments
1.00	07/17/2006	Initial ratified release.
1.01	08/22/2006	Modified section 3.1.2 to allow any approved 1 meter straight-straight cables in the System Interop test configurations rather than referring to a single product number.

Table of Contents

1. Goals, Objectives, & Constraints

This document defines the test requirements specific to the SATA-IO Interoperability Program. Many of the test requirements are associated with a subset of requirements included in the Serial ATA (SATA) Revision 2.5 specification and these test requirements are based upon the requirements for the Serial ATA protocol and features, intended to verify a subset of the specification requirements and ensuring compatibility for Serial ATA. Not every feature or capability within the Serial ATA architecture may be included in the Integrator's List testing. The requirements are driven by the necessary capabilities of the specification that can be verified by functional testing. There are additional test requirements which are intended to verify general system interoperability which are not associated with any specification requirements.

Some of the goals and requirements for the Interoperability Program documentation include:

- Maintain adherence to Serial ATA specification(s) across all SATA products
- Maintain compatibility with older hosts & devices without compromising product adherence to the specification
- Deliver standard test requirements for Serial ATA products

1.1. References

This document is not a Serial ATA specification but includes requirements for testing adherence to a subset of the Serial ATA specification guidelines, in addition to system interoperability tests. This document makes reference to the following specifications and documents:

- Serial ATA Revision 2.5. Available for download at www.sata-io.org.
- AT Attachment with Packet Interface – 6 (ATA/ATAPI-6). Draft available at www.T13.org. Published ATA/ATAPI specifications available from ANSI at webstore.ansi.org or from Global Engineering.
- Serial ATA Interoperability Program Policy Document revision 1.0. Available for download at www.sata-io.org.
- Serial ATA Interoperability Program Description Document v4. Available for download at www.sata-io.org.

1.2. Definitions and Conventions

1.2.1. Definitions

1.2.1.1. Component

General reference to any SATA product supportable by the Interop Program for testing.

1.2.1.2. Device

A component falling under the Device component class which is a storage peripheral. This includes both hard disk drives and ATAPI devices.

1.2.1.3. Frame Information Structure (FIS)

The user payload of a frame, does not include the SOF, CRC, and EOF delimiters.

1.2.1.4. Frame

A frame is an indivisible unit of information exchanged between a host and device. A frame consists of a SOF primitive, a Frame Information Structure, a CRC calculated over the contents of the FIS, and an EOF primitive.

1.2.1.5. Host

A Host or Host Bus Adapter (HBA) is a component that connects to the host system's expansion bus to provide connectivity for devices. Host Bus Adapters are also often referred to as controller cards or merely controllers

1.2.2. Conventions

Lowercase is used for words having the normal English meaning. Certain words and terms used in this document have a specific meaning beyond the normal English meaning. These words and terms are defined either in clause 1.2.2.1 or in the text where they first appear.

The names of abbreviations, commands, fields, and acronyms used as signal names are in all uppercase (e.g., IDENTIFY DEVICE). Fields containing only one bit are usually referred to as the "name" bit instead of the "name" field.

Names of device registers begin with a capital letter (e.g., Cylinder Low register).

1.2.2.1. Keywords

Several keywords are used to differentiate between different levels of requirements and optionality.

1.2.2.1.1. mandatory

A keyword indicating items to be implemented as defined by this document.

1.2.2.1.2. may

A keyword that indicates flexibility of choice with no implied preference.

1.2.2.1.3. optional

A keyword that describes test requirements that are not required by this document. However, if any optional compliance point defined by the document is implemented, the feature shall be implemented in the way defined by the Serial ATA standard.

1.2.2.1.4. shall

A keyword indicating a mandatory requirement. Designers are required to implement all such mandatory requirements to ensure interoperability with other Serial ATA standard conformant products.

1.2.2.1.5. should

A keyword indicating flexibility of choice with a strongly preferred alternative. Equivalent to the phrase "it is recommended".

1.3. Component Classes

Due to the difference in architecture and design of Serial ATA products, the test requirements will be distinguishable between the following types of components:

- Device : hard disk drive or ATAPI device
- Cable

Each test associated with a specification requirement may have separately defined Expected Behavior for each of the above component classes. In each case, there may be different methodology for both testing the test requirement and determining the pass/fail criteria. Each

test requirement will include the following: Expected Behavior, Measurement Requirements, and Pass/Fail Criteria. The general definition of these subjects is below.

1.3.1. Expected Behavior

All of the test requirements have expected behavior as defined in Serial ATA Revision 2.5. All of the expected behavior for each test requirement directly shall refer to the appropriate Serial ATA specification requirement(s) being tested.

1.3.2. Measurement Requirements

Each test requirement contains detailed information necessary for developing tests for verification of the referenced Serial ATA requirement. This information could include types of equipment, testing methodologies, test setup routines, and other helpful information.

1.3.3. Pass/Fail Criteria

The Pass/Fail criteria defined will be clear and concise, and include specific information necessary to determine passing or failing of a test. Actual results gathered during testing must be documented in addition to determination of pass vs. fail for a test.

1.4. Methods of Implementation

A Method of Implementation (MOI) is defined as documentation specifying test tool details and procedures for the specific use of verifying the different Interoperability test areas. In the future a template for development of a MOI for a specific test tool may be developed, but at this time a MOI, at a minimum, must simply include the following:

- Hardware equipment model number(s)
- Software revision number(s)
- Hardware dependencies (e.g. test fixtures)
- Component dependencies (e.g. BIST modes, patterns)
- Detailed procedures for using the equipment to verify the specific Interop test requirements
- Procedures for extraction of results
- Approximate execution time of specific Interop test requirements

There are different MOI classes which are specific to the different test areas included in this Unified Test Document. Any test tool approved for use in Interoperability Testing must fall under test execution within one of the following MOI classes:

- Digital/protocol (device only)
- Phy electrical (device only)
- Phy TX/RX requirements (devices only)
- Device mechanical (device only)
- Cable mechanical (cable only)
- Cable electrical (cable only)
- System interoperability

It is feasible that separate MOIs are developed for each type of equipment used depending on the class of testing, or that a single MOI is used to cover an entire test class including the details for several pieces of test tool equipment. This will be determined by the appropriate test tool vendors with considerations from the SATA-IO.

Unless otherwise stated, it is expected that different test tools will evaluate a given result for a similar product within 5%.

1.5. Test Component Considerations

1.5.1. Device Considerations

A device vendor is required to supply at least three samples. In some cases up to two samples will be run through testing at a given time. The third sample could be available for backup in case of unexpected errors or failures.

For many of the Phy electrical tests, it is required that a device is able to transmit patterns which are identified within the specification. There are standard ways of doing this through the BIST protocol per definition within the specification. Although some of the BIST capabilities are optional, the support of these capabilities does somewhat ease the testing procedures in several areas. If a device does not specifically support either BIST T, A, S, or L capabilities then the vendor needs to bring all equipment to support vendor unique methods for transmitting the appropriate patterns. Note that this vendor unique process can have no substantial impact to the test during interoperability testing (e.g. significant growth in test execution time or complexity of equipment calibration/setup).

1.5.2. Cable Considerations

If a cable assembly product family consists of cables which differ only in their length (the connector design, cable construction, and assembly method is identical) and if the shortest and longest lengths pass the test requirements then all intermediate lengths are considered to be passing.

A cable vendor is required to supply at least two identical samples of each length tested.

2. Specification Requirement Tests

Table 1 outlines the test requirements for the different types of Serial ATA units under test.

Table 1 - Test requirements by Component Class

Test Area	Document Section	Test Requirement	Classification	Device - HDD	Device - ATAPI	Cable - Interface	Cable - Power
GDR	Section 2.1	GDR-01	Digital	M	M	--	--
		GDR-02	Digital	F	F	--	--
		GDR-03	Digital	M	M	--	--
		GDR-04	Digital	M	M	--	--
		GDR-05	Digital	M	M	--	--
NCQ	Section 2.2	NCQ-01	Digital	F	--	--	--
		NCQ-02	Digital	F	--	--	--
		NCQ-03	Digital	F	--	--	--
		NCQ-04	Digital	F	--	--	--
		NCQ-05	Digital	F	--	--	--
ASR	Section 2.3	ASR-01	Digital	M	M	--	--
		ASR-02	Digital	F	F	--	--
SSP	Section 2.4	SSP-01	Digital	F	--	--	--
		SSP-02	Digital	F	--	--	--
		SSP-03	Digital	F	F	--	--
		SSP-04	Digital	F	--	--	--
		SSP-05	Digital	F	F	--	--
		SSP-06	Digital	F	F	--	--
		SSP-07	Digital	F	F	--	--
		SSP-08	Digital	F	F	--	--

Test Area	Document Section	Test Requirement	Classification	Device - HDD	Device - ATAPI	Cable - Interface	Cable - Power
		SSP-09	Digital	F	F	--	--
		SSP-10	Digital	F	F	--	--
		SSP-11	Digital	F	--	--	--
IPM	Section 2.5	IPM-01	Digital	F	F	--	--
		IPM-02	Digital	F	F	--	--
		IPM-03	Digital	F	F	--	--
		IPM-04	Digital	F	F	--	--
		IPM-05	Digital	F	F	--	--
		IPM-06	Digital	F	F	--	--
		IPM-07	Digital	F	F	--	--
MCI	Section 2.6	MCI-01	CabCon	--	--	M	
		MCI-02	CabCon	--	--	M	
		MCI-03	CabCon	--	--	F	
		MCI-04	CabCon	--	--	F	
		MCI-05	CabCon	--	--	M	
SI	Section 2.7	SI-01	CabCon	--	--	M	
		SI-02	CabCon	--	--	M	
		SI-03	CabCon	--	--	M	
		SI-04	CabCon	--	--	M	
		SI-05	CabCon	--	--	M	
		SI-06	CabCon	--	--	M	
		SI-07	CabCon	--	--	M	
		SI-08	CabCon	--	--	M	
		SI-09	CabCon	--	--	M	
MDI	Section 2.8	MDI-01	CabCon	M	M	--	--
		MDI-02	CabCon	M	M	--	--
MDP	Section 2.9	MDP-01	CabCon	M	M	--	--
PHY	Section 2.10	PHY-01	Phy	M	M	--	--
		PHY-02	Phy	M	M	--	--
		PHY-03	Phy	F	F	--	--
		PHY-04	Phy	F	F	--	--
TX	Section 2.11	TX-01	Phy	M	M	--	--
		TX-02	Phy	M	M	--	--
		TX-03	Phy	F	F	--	--
		TX-04	Phy	F	F	--	--
		TX-05	Phy	F	F	--	--
TSG	Section 2.12	TSG-01	Phy	M	M	--	--
		TSG-02	Phy	M	M	--	--
		TSG-03	Phy	M	M	--	--
		TSG-04	Phy	F	F	--	--
		TSG-05	Phy	F	F	--	--
		TSG-06	Phy	F	F	--	--
		TSG-07	Phy	O	O	--	--
		TSG-08	Phy	O	O	--	--
		TSG-09	Phy	M	M	--	--
		TSG-10	Phy	M	M	--	--
		TSG-11	Phy	F	F	--	--
		TSG-12	Phy	F	F	--	--
RX	Section 2.13	RX-01	Phy	M	M	--	--
		RX-02	Phy	M	M	--	--
		RX-03	Phy	F	F	--	--

Test Area	Document Section	Test Requirement	Classification	Device - HDD	Device - ATAPI	Cable - Interface	Cable - Power
		RX-04	Phy	F	F	--	--
		RX-05	Phy	F	F	--	--
OOB	Section 2.14	OOB-01	Phy	M	M	--	--
		OOB-02	Phy	M	M	--	--
		OOB-03	Phy	M	M	--	--
		OOB-04	Phy	M	M	--	--
		OOB-05	Phy	M	M	--	--
		OOB-06	Phy	M	M	--	--
		OOB-07	Phy	M	M	--	--

Key:
M – Test is mandatory for listed component type
F – Test is feature dependent for list component type
O – Test is optional, for informational purposes
-- – Test is not valid for listed component type

2.1. General Device Requirements

All Serial ATA devices under test shall meet the test requirements listed within this section to confirm Serial ATA interoperability relevant to the specified Expected Behavior.

2.1.1. GDR-01 – Software Reset

2.1.1.1. Device Expected Behavior

See section 11.3 of Serial ATA Revision 2.5.

Once the initial Register device-to-host FIS has been received and successfully acknowledged with no errors, a Device shall successfully respond to the setting of the SRST bit in the Device Control register at any time and perform the software reset protocol.

Measurement Requirements

- Repeat the following 5 times
    - Issue SRST to device when no command is outstanding

Pass/Fail Criteria

- Verify Register FIS receipt (after reset sequence) from device with the appropriate signature contents within an allotted 31 second timeframe (these results shall be verified for all test instances)

2.1.2. GDR-02 -- 3Gb/s Backwards Compatibility

2.1.2.1. Device Expected Behavior

See section 7.4.21.1.2 of Serial ATA Revision 2.5.

If a device claims support for Serial ATA Gen-2 signaling speed (Word 76 bit 2 set to one in IDENTIFY DEVICE or IDENTIFY PACKET DEVICE data), then it shall also support Serial ATA Gen-1 signaling speed (Word 76 bit 1 set to one in IDENTIFY DEVICE or IDENTIFY PACKET DEVICE data).

In addition to verifying the IDENTIFY DEVICE or IDENTIFY PACKET DEVICE contents, support shall be verified by ensuring compatibility and interoperability with both a Gen-1 host and Gen-2 host. Details on how this testing is done is not specified in this document.

Measurement Requirements

- Check Word 76 bit 2 in IDENTIFY DEVICE or IDENTIFY PACKET DEVICE data (set to one)
- If the above are true, then run the following test when connected to a 3Gb/s host and 1.5Gb/s host
    - Check Word 76 bit 1 in IDENTIFY DEVICE or IDENTIFY PACKET DEVICE data (set to one)
    - Complete OOB sequence at least 10 times

Pass/Fail Criteria

- Values below shall be confirmed when tested in connection with both 3Gb/s host and 1.5Gb/s host
    - Verify IDENTIFY DEVICE or IDENTIFY PACKET DEVICE contents including:
        - If Word 76 bit 2 set to one, then Word 76 bit 1 set to one
    - Verify Register FIS receipt (after each OOB sequence) from device with the appropriate signature contents (see ATA/6 reference)

2.1.3. GDR-03 – DMA Protocol Support

2.1.3.1. Device Expected Behavior

See sections 13.2.1 and 13.2.2 of Serial ATA Revision 2.5.

DMA support can be verified through Word 49 bit 8 in IDENTIFY DEVICE or IDENTIFY PACKET DEVICE data. This bit shall be set to one for all Serial ATA devices.

Measurement Requirements

- Check Word 49 bit 8 in IDENTIFY DEVICE or IDENTIFY PACKET DEVICE data (set to one)
- If the above are true, then run the appropriate tests below

There are several test scenarios that are required when testing a HDD for this test requirement, all of which shall be tested 5 times each to verify passing of the test:

- Issue IDENTIFY DEVICE to device
- Issue and complete WRITE DMA command to device with transfer size of </= 8Kbytes, followed by issue and completion of READ DMA command to device to the same disk location that the previous write was completed. The test shall verify that the contents read have the same values that were previously written.
- Issue and complete WRITE DMA command to device with transfer size of > 8Kbytes, followed by issue and completion of READ DMA command to device to the same disk location that the previous write was completed. The test shall verify that the contents read have the same values that were written initially.

There are several test scenarios that are required when testing an ATAPI read-only device for this test requirement, all of which shall be tested 5 times each to verify passing of the test. The tests below are for ATAPI devices which only support reading from media (e.g. CDROM, DVDROM, etc…).

- Issue IDENTIFY PACKET DEVICE to device
- Issue and complete a read command using the DMA protocol with transfer size of </= 8Kbytes, followed by issue and completion of another read command using the DMA protocol to the same disk location that the previous read was completed. The test shall verify that the contents read have the same values that were read initially.
- Issue and complete a read command using the DMA protocol with transfer size of > 8Kbytes, followed by issue and completion of another read command using the DMA

protocol to the same disk location that the previous read was completed. The test shall verify that the contents read have the same values that were read initially.

There are several test scenarios that are required when testing an ATAPI device for this test requirement, all of which shall be tested 5 times each to verify passing of the test. The tests below are for ATAPI devices which support writing to media.

- Issue IDENTIFY PACKET DEVICE to device
- Issue and complete a write command using the DMA protocol with transfer size of </= 8Kbytes, followed by issue and completion of a read command using the DMA protocol to the same disk location that the previous write was completed. The test shall verify that the contents read have the same values that were previously written.
- Issue and complete a write command using the DMA protocol with transfer size of > 8Kbytes, followed by issue and completion of a read command using the DMA protocol to the same disk location that the previous write was completed. The test shall verify that the contents read have the same values that were previously written.

Pass/Fail Criteria

- Verify Word 49 bit 8 set to one in IDENTIFY DEVICE or IDENTIFY PACKET DEVICE
- Verify that data read is equal to data initially written (or read in case of ATAPI read-only device)

2.1.4. GDR-04 – Word 93 Contents

2.1.4.1. Device Expected Behavior

See sections 13.2.1 and 13.2.2 of Serial ATA Revision 2.5.

For all Serial ATA devices, the entire contents of Word 93 in IDENTIFY DEVICE or IDENTIFY PACKET DEVICE data shall be cleared to zero.

Measurement Requirements

- Issue IDENTIFY DEVICE or IDENTIFY PACKET DEVICE to device

Pass/Fail Criteria

- Verify Word 93 is cleared to zero in IDENTIFY DEVICE or IDENTIFY PACKET DEVICE

2.1.5. GDR-05 : Unrecognized FIS receipt

2.1.5.1. Device Expected Behavior

See section 10.3.1.1 of Serial ATA Revision 2.5.

The receiver of an “unrecognized FIS” shall follow the link layer state machine definitions in section 9.6 of the Serial ATA Revision 2.5 specification upon receipt of an “unrecognized FIS”. The expected response is status return with an R_ERR.

Note that determination of any FIS being ‘unrecognized’ is done by the recipient of the FIS.

Measurement Requirements

- Transmit undefined FIS to device

Pass/Fail Criteria

- Verify R_ERR response from device

2.2. Native Command Queuing

The Native Command Queuing (NCQ) test requirements are determined by the requirements of the feature as defined in Serial ATA Revision 2.5.

All of the test requirements listed in this section require that support for NCQ is claimed by the component for verification of the Expected Behavior. Support for NCQ can be verified by reading Word 76 bit 8 set to one in IDENTIFY DEVICE data.

2.2.1. NCQ-01 : Forced Unit Access

2.2.1.1. Device Expected Behavior

See sections 11.14 and 13.5.4 of Serial ATA Revision 2.5.

Devices that support the NCQ commands (READ FPDMA QUEUED and WRITE FPDMA QUEUED) shall support the Force Unit Access (FUA) bit.

For WRITE FPDMA QUEUED when the FUA bit is set to one, the data shall be written to the storage media before completing the command.

Measurement Requirements

- Check Word 76 bit 8 in IDENTIFY DEVICE (set to one)
- If the above is true, then run the following test
    - Issue and complete WRITE FPDMA QUEUED with FUA bit set.
    - Issue and complete READ FPDMA QUEUED to the same disk location.

Pass/Fail Criteria

- Verify that data read is equal to data written.

2.2.2. NCQ-02 : Read Log Ext log page 10h support

2.2.2.1. Device Expected Behavior

See section 13.5.4.3.1 of Serial ATA Revision 2.5.

If a device claims support for Native Command Queuing (Word 76 bit 8 set to one in IDENTIFY DEVICE data), then it shall also support READ LOG EXT log page 10h. Support for READ LOG EXT log page 10h is reflected in the General Purpose Log Directory page (log page 0) by having the value 1 at offset 20h and the value 0 at offset 21h of that log page to indicate existence of a log page at address 10h of 1-page in length.

Measurement Requirements

- Check Word 76 bit 8 in IDENTIFY DEVICE (set to one)
- If the above is true, then run the following test
    - Issue READ LOG EXT to log page 00h

Pass/Fail Criteria

- Verify offset 20h of log page 00h contains value of 1
- Verify offset 21h of log page 00h contains value of 0

2.2.3. NCQ-03 : Intermix of Legacy and NCQ commands

2.2.3.1. Device Expected Behavior

See section 13.5.3 and 13.5.4.3 of Serial ATA Revision 2.5.

Upon receiving a legacy ATA command while a native queued command is outstanding, an error has occurred and the device shall perform necessary state cleanup to return to a state with no commands pending. Legacy ATA commands include all commands other than the READ FPDMA QUEUED and WRITE FPDMA QUEUED commands.

The device shall signal the error condition to the host by transmitting a Register FIS to the host with the ERR bit set to one and the BSY bit cleared to zero in the Status field, and the ABRT bit set to one in the Error field. Upon detecting an error when there are one or more NCQ commands outstanding, the device shall stop processing commands until a READ LOG EXT command with a specified log page of 10h or reset is issued. Upon receipt of the READ LOG EXT command, the device shall send a Set Device Bits FIS to discard all commands in the pending device queue, followed by data for the log page. The READ LOG EXT page shall reflect that the error condition was a result of a legacy ATA command having been issued by having the NQ bit set to one. The device shall not continue command processing for any of the outstanding commands following this error.

If no prior NCQ error has occurred and a device has received a READ LOG EXT command while there are NCQ commands outstanding, the device shall respond as described above as having received a legacy ATA command while one or more native queued commands are outstanding.

Measurement Requirements

- Check Word 76 bit 8 in IDENTIFY DEVICE (set to one)
- If the above is true, then run the following test
  - Check Word 75 bits 4:0 to verify maximum queue depth reported by device
  - Issue at least X random FPDMA QUEUED commands (read or write), where X is the maximum queue depth reported above
  - Issue a legacy ATA command using one of the following (NOTE that the test shall be run a total of three times to ensure each legacy ATA command listed below is used for the test):
    - IDENTIFY DEVICE
    - PIO write
    - DMA read
  - Verify Register FIS receipt with Error
    - Issue Read Log Ext to log page 10h

Pass/Fail Criteria

- Verify receipt of Register FIS with error
- Verify SDB receipt with ERR bit cleared to zero, the ‘I’ bit cleared to zero, and the SActive field set to FFFFFFFFh.
- Verify that the NQ bit is set to one in the data within log page 10h
- NOTE – there is opportunity for a device to complete all outstanding commands prior to the host being able to send the legacy ATA command. In these cases, the device may not be failed for this particular test.

2.2.4. NCQ-04 : Device response to malformed NCQ command

2.2.4.1. Device Expected Behavior

See section 13.5.2.4 and 13.5.4.3 of Serial ATA Revision 2.5.

Malformed commands could include the following situations:

- Specified LBA is out of the device supported range
- Duplicate tag value for outstanding NCQ command

- TAG value is out of the device supported range, only in the case that the device reports support for less than 32 outstanding commands

In response to a malformed READ FPDMA QUEUED or WRITE FPDMA QUEUED command due to a duplicate tag or out of range tag, the device shall transmit a Register FIS to the host with the ERR bit set to one, and the BSY bit cleared to zero in the Status register. The 'I' bit shall be set to one. The ABRT bit shall be set in the Error field. The device shall stop processing commands until a READ LOG EXT command with a specified log page of 10h or reset is issued. Upon receipt of the READ LOG EXT command, the device shall send a Set Device Bits FIS to discard all commands in the pending device queue, followed by data for the log page. The READ LOG EXT page shall have the NQ bit cleared to zero. The TAG field within the log page shall contain the tag associated with the NCQ command which failed.

In response to a malformed READ FPDMA QUEUED or WRITE FPDMA QUEUED command due to an LBA out of range, the device may report the error in one of two ways:

- Transmit a Register FIS to the host with the ERR bit set to one, and the BSY bit cleared to zero in the Status register. The 'I' bit shall be set to one. Either the ABRT bit or IDNF bit shall be set to one in the Error field. The device shall stop processing commands until a READ LOG EXT command with a specified log page of 10h or reset is issued. Upon receipt of the READ LOG EXT command, the device shall send a Set Device Bits FIS to discard all commands in the pending device queue, followed by data for the log page. The READ LOG EXT page shall have the NQ bit cleared to zero. The TAG field within the log page shall contain the tag associated with the NCQ command which failed.
- If the device accepts the command, then the device shall report the error within a subsequent Set Device Bits FIS. A Set Device Bits FIS shall be transferred with the ERR bit set to one, and the BSY bit cleared to zero in the Status register. The 'I' bit shall set to one. Either the ABRT bit or IDNF bit shall be set to one in the Error field. The device shall stop processing commands until a READ LOG EXT command with a specified log page of 10h or reset is issued. Upon receipt of the READ LOG EXT command, the device shall send a Set Device Bits FIS to discard all commands in the pending device queue, followed by data for the log page. The READ LOG EXT page shall have the NQ bit cleared to zero. The TAG field within the log page shall contain the tag associated with the NCQ command which failed.

Measurement Requirements

- Check Word 76 bit 8 in IDENTIFY DEVICE (set to one)
- If the above is true, then run the following test
    - Issue an FPDMA command with one of the following (NOTE that the test shall be run a total of three times to ensure each type of command listed below is used for the test):
        - LBA out of range (refer to Words 61:60 in IDENTIFY DEVICE data)
        - Duplicate tag for another outstanding NCQ command (will require other outstanding NCQ commands)
        - Tag value out of device supported range (refer to Word 75 bits 4:0 in IDENTIFY DEVICE data)
- Verify Register FIS receipt with Error
    - Issue Read Log Ext to log page 10h
- If a Register FIS is not received with Error, then an SDB FIS receipt posting the error should be expected
    - Issue Read Log Ext to log page 10h

Pass/Fail Criteria

- In the case of a duplicate tag or tag out of range, verify the following:
    - Verify receipt of Register FIS with error, followed by

- Verify SDB receipt with ERR bit cleared to zero, and 'I' bit cleared to zero. The SActive field shall be set to FFFFFFFFh.
- Verify that the TAG field includes the tag associated with the failed NCQ command in the data within log page 10h

- In the case of LBA out of range, verify one of the following:
  - 1) Verify receipt of Register FIS with error, followed by
    - Verify SDB receipt with ERR bit cleared to zero, the 'I' bit cleared to zero, and the SActive field set to FFFFFFFFh.
    - Verify that the TAG field includes the tag associated with the failed NCQ command in the data within log page 10h
  - 2) Verify receipt of SDB FIS with error, followed by
    - Verify SDB receipt with ERR bit cleared to zero, the 'I' bit cleared to zero, and the SActive field set to FFFFFFFFh.
    - Verify that the TAG field includes the tag associated with the failed NCQ command in the data within log page 10h

2.2.5. NCQ-05 : DMA Setup Auto-Activate

2.2.5.1. Device Expected Behavior

See section 10.3.7.3.1 of Serial ATA Revision 2.5.

To test for this test requirement, the device shall claim support for DMA Setup Auto-Activate (IDENTIFY DEVICE data, Word 78 bit 2 set to one) and have the feature enabled using the SET FEATURES command (IDENTIFY DEVICE data, Word 79 bit 2 set to one).

A device shall not transmit a DMA Activate FIS to trigger transmission of the first Data FIS from the host, if it had previously sent a DMA Setup FIS with the Auto-Activate bit ('A') set to one.

Measurement Requirements

- Check Word 76 bit 8 in IDENTIFY DEVICE (set to one)
- If the above is true, then run the following test
  - Check Word 78 bit 2 in IDENTIFY DEVICE
  - Issue SET FEATURES with Features value of 10h and Sector Count value of 02h
  - Check Word 79 bit 2 in IDENTIFY DEVICE
  - Issue WRITE DMA QUEUED with Auto-Activate bit set

Pass/Fail Criteria

- Verify Word 78 bit 2 of IDENTIFY DEVICE is set to one
- Verify Word 79 bit 2 of IDENTIFY DEVICE is set to one (following SET FEATURES)
- Verify command completion (data transferred and Register FIS received)

2.3. Asynchronous Signal Recovery

The Serial ATA Asynchronous Signal Recovery (ASR) test requirements are determined by the requirements of the feature as defined in Serial ATA Revision 2.5.

2.3.1. ASR-01 : COMINIT response interval

2.3.1.1. Device Expected Behavior

See section 15.2.2.2 of Serial ATA Revision 2.5.

In a case where the device is in an interface quiescent state in response to receipt of a COMRESET signal from the host, the device shall respond with a COMINIT signal within 10 ms of de-qualification of a received COMRESET signal.

Measurement Requirements

- Power on host & device
- Setup bus analyzer (or scope) for tracing of bus activity & begin tracing
- Initiate COMRESET sequence

Pass/Fail Criteria

- Confirm OOB sequence completion and COMINIT timing of being within 10ms of COMRESET receipt from host (use trace to analyze timings)

2.3.2. ASR-02 : COMINIT OOB Interval

2.3.2.1. Device Expected Behavior

See section 8.2 of Serial ATA Revision 2.5.

When Phy communication is not established, the device shall not initiate a new OOB (COMINIT) to the host faster than every 10 ms.

Measurement Requirements

- Power on host & device
- Setup bus analyzer (or scope) for tracing of bus activity & begin tracing
- Power off host, keeping device powered on

Pass/Fail Criteria

- Verify that once host is powered off, that device sends COMINIT repeatably and no faster than every 10ms (use trace to verify behavior and timings)

2.4. Software Settings Preservation

The Serial ATA software settings preservation (SSP) test requirements are determined by the requirements of the feature as defined in Serial ATA Revision 2.5.

All of the test requirements listed in this section require that support for Software Settings Preservation is claimed by the component for verification of the Expected Behavior. Support for Software Settings Preservation can be verified by reading Word 78 bit 6 set to one in IDENTIFY DEVICE or IDENTIFY PACKET DEVICE data.

See section 13.4 of Serial ATA Revision 2.5 for details on Software Settings Preservation.

2.4.1. SSP-01 : Initialize Device Parameters

2.4.1.1. Device Expected Behavior

This test is not applicable to ATAPI devices.

NOTE - To test the following requirement, a device must claim that the value contained in Words 58:54 are valid (Word 53 bit 0 set to one in IDENTIFY DEVICE data).

Upon receipt of a COMRESET, a device shall maintain the device settings established by the INITIALIZE DEVICE PARMATERS command. Specifically, the values contained within Words 58:54 in IDENTIFY DEVICE data shall be maintained after a COMRESET. The value contained within Word 53 bit 0 in IDENTIFY DEVICE data shall also be maintained after a COMRESET.

Measurement Requirements

- Check Word 78 bit 6 in IDENTIFY DEVICE (set to one)
- Check Word 53 bit 0 (set to one)

- If the above is false, then the test is not applicable
- Otherwise, run the following test
    - Check value of device settings (Words 58:54)
    - Issue COMRESET and complete OOB sequence
    - Check value of device settings (Words 58:54)

Pass/Fail Criteria
- Verify that IDENTIFY DEVICE Words 58:54 contain the same values following COMRESET

2.4.2. SSP-02 : Read/Write Stream Error Log

2.4.2.1. Device Expected Behavior

This test is not applicable to ATAPI devices.

NOTE - To test the following requirement, a device must claim support for Streaming (Word 84 bit 4 set to one in IDENTIFY DEVICE data).

Upon receipt of a COMRESET, a device shall maintain the Read Stream Error Log and Write Stream Error Log contents. Specifically, the values contained within log addresses 22:21 shall be maintained after a COMRESET.

Measurement Requirements
- Check Word 78 bit 6 in IDENTIFY DEVICE (set to one)
- Check Word 84 bit 4 (set to one)
- If the above is false, then the test is not applicable
- Otherwise, run the following test
    - Check value of log pages 22:21
    - Issue COMRESET and complete OOB sequence
    - Check value of log pages 22:21

Pass/Fail Criteria
- Verify that log pages 22:21 contain the same values following COMRESET

2.4.3. SSP-03 : Security Mode State

2.4.3.1. Device Expected Behavior

NOTE - To test the following requirement, a device must claim support for Security Mode (Word 82 bit 1 set to one in IDENTIFY DEVICE or IDENTIFY PACKET DEVICE data).

Upon receipt of a COMRESET, a device shall maintain the value of Security Mode. Specifically, if Security Mode is enabled (Word 85 bit 1 set to one in IDENTIFY DEVICE or IDENTIFY PACKET DEVICE data) upon receipt of a COMRESET then the mode value (Word 128 bits 3:1 in IDENTIFY DEVICE or IDENTIFY PACKET DEVICE data) shall be maintained after a COMRESET.

Measurement Requirements
- Check Word 78 bit 6 in IDENTIFY DEVICE or IDENTIFY PACKET DEVICE (set to one)
- Check Word 82 bit 1 (set to one)
- If the above is false, then the test is not applicable
- Otherwise, run the following test
    - Check value of Word 85 bit 1 (set to one)
        - If the above is not true, then the Security Mode feature set must be enabled to continue

- Check value of Word 128 bits 3:1
- Issue COMRESET and complete OOB sequence
- Check value of Word 85 bit 1 (set to one)
- Check value of Word 128 bits 3:1

Pass/Fail Criteria

- Verify that IDENTIFY DEVICE or IDENTIFY PACKET DEVICE Word 85 bit 1 contains the same value following COMRESET
- Verify that IDENTIFY DEVICE or IDENTIFY PACKET DEVICE Word 128 bits 3:1 contain the same value following COMRESET

2.4.4. SSP-04 : Set Address Max

2.4.4.1. Device Expected Behavior

This test is not applicable to ATAPI devices.

NOTE - To test the following requirement, a device must claim support for Host Protected Area (Word 82 bit 10 set to one in IDENTIFY DEVICE data).

Upon receipt of a COMRESET, a device shall maintain the max address established by the SET MAX ADDRESS or SET MAX ADDRESS EXT command. Specifically, the value contained within Words 61:60 in IDENTIFY DEVICE data shall be maintained after a COMRESET.

If 48-bit support is enabled by the device (Word 83 bit 10 set to one in IDENTIFY DEVICE data), then the values contained within Words 103:100 in IDENTIFY DEVICE data shall also be maintained after a COMRESET.

Measurement Requirements

- Check Word 78 bit 6 in IDENTIFY DEVICE (set to one)
- Check Word 82 bit 10 in IDENTIFY DEVICE (set to one)
- If the above is false, then the test is not applicable
- Otherwise, run the following test
  - Issue READ NATIVE MAX ADDRESS (or READ NATIVE MAX ADDRESS EXT) to get max user accessible address.
  - Issue SET MAX ADDRESS (or SET MAX ADDRESS EXT) with new valid max accessible address
  - Check value of Word 83 bit 10
  - Check value of Words 61:60
  - If Word 83 bit 10 is set to one, also check value of Words 103:100
  - Verify correct address is set due to SET MAX ADDRESS (EXT) command
  - Issue COMRESET and complete OOB sequence
  - Check value of Words 61:60
  - If Word 83 bit 10 is set to one, also check value of Words 103:100

Pass/Fail Criteria

- Verify that IDENTIFY DEVICE Words 61:60 contain the same values following COMRESET, additionally if Word 83 bit 10 is set to one verify that Words 103:100 contain the same values following COMRESET

2.4.5. SSP-05 : Set Features – Write Cache Enable/Disable

2.4.5.1. Device Expected Behavior

NOTE - To test the following requirement, a device must claim support for Write Cache (Word 82 bit 5 set to one in IDENTIFY DEVICE or IDENTIFY PACKET DEVICE data).

Upon receipt of a COMRESET, a device shall maintain the value of write cache enable/disable. Specifically, if write cache is enabled (Word 85 bit 5 set to one in IDENTIFY DEVICE or IDENTIFY PACKET DEVICE data) upon receipt of a COMRESET then the feature shall be enabled after the COMRESET. If write cache is disabled (Word 85 bit 5 cleared to zero in IDENTIFY DEVICE or IDENTIFY PACKET DEVICE data) upon receipt of a COMRESET then the feature shall be disabled after the COMRESET.

Measurement Requirements

- Check Word 78 bit 6 in IDENTIFY DEVICE or IDENTIFY PACKET DEVICE (set to one)
- Check value of Word 82 bit 5 (set to one)
- If the above is false, then the test is not applicable
- Otherwise, run the following test
    - Check value of Word 85 bit 5
    - Issue SET FEATURES to alter setting for Write Cache enable/disable
    - Issue COMRESET and complete OOB sequence
    - Check value of Word 85 bit 5

Pass/Fail Criteria

- Verify that IDENTIFY DEVICE or IDENTIFY PACKET DEVICE Word 85 bit 5 contains the same value following COMRESET

2.4.6. SSP-06 : Set Features – Set Transfer Mode

2.4.6.1. Device Expected Behavior

Upon receipt of a COMRESET, a device shall maintain the PIO, Multiword DMA and Ultra DMA mode settings. Specifically, the values contained within Word 63 bits 10:8 (MWDMA) and Word 88 bits 14:8 (UDMA) in IDENTIFY DEVICE or IDENTIFY PACKET DEVICE data shall be maintained after a COMRESET.

The bits in Word 88 are only valid if Word 53 bit 2 is set to one.

There is no method of verification for PIO modes regarding this requirement.

Measurement Requirements

- Check Word 78 bit 6 in IDENTIFY DEVICE or IDENTIFY PACKET DEVICE (set to one)
- If the above is false, then the test is not applicable
- Otherwise, run the following test
    - Check value of Word 63 bits 10:8
    - Check value of Word 88 bits 14:8
    - Issue COMRESET and complete OOB sequence
    - Check value of Word 63 bits 10:8
    - Check value of Word 88 bits 14:8
    - Issue a read to any valid random location on the device (using DMA transfer)
        - Note that you may need to appropriately handle the reset condition for ATAPI devices (i.e. handling of request sense)

Pass/Fail Criteria

- Verify that IDENTIFY DEVICE or IDENTIFY PACKET DEVICE Word 63 bits 10:8 contain the same values following COMRESET
- Verify that Word 88 bits 14:8 contain the same values following COMRESET
- Verify that the read command completed successfully

2.4.7. SSP-07 : Set Features – Advanced Power Management Enable/Disable

2.4.7.1. Device Expected Behavior

NOTE - To test the following requirement, a device must claim support for Advanced Power Management (Word 83 bit 3 set to one in IDENTIFY DEVICE data).

Upon receipt of a COMRESET, a device shall maintain the value of Advanced Power Management (APM) enable/disable and the advanced power management level. Specifically, if APM is enabled (Word 86 bit 3 set to one in IDENTIFY DEVICE or IDENTIFY PACKET DEVICE data) upon receipt of a COMRESET then the feature shall be enabled after the COMRESET, and Word 91 bits 7:0 in IDENTIFY DEVICE or IDENTIFY PACKET DEVICE data shall contain the value present prior to the COMRESET. If APM is disabled (Word 86 bit 3 cleared to zero in IDENTIFY DEVICE or IDENTIFY PACKET DEVICE data) upon receipt of a COMRESET then the feature shall be disabled after the COMRESET.

Measurement Requirements

- Check Word 78 bit 6 in IDENTIFY DEVICE or IDENTIFY PACKET DEVICE (set to one)
- Check Word 83 bit 3 (set to one)
- If the above is false, then the test is not applicable
- Otherwise, run the following test
    - Check Word 86 bit 3 (set to one)
    - Issue SET FEATURES to alter setting for APM enable/disable
    - If Word 86 bit 3 is set to one,
        - Check value of Word 91 bits 7:0
    - Issue COMRESET and complete OOB sequence
    - Check Word 83 bit 3,
    - If Word 86 bit 3 is set to one,
        - Check value of Word 91 bits 7:0

Pass/Fail Criteria

- Verify that IDENTIFY DEVICE or IDENTIFY PACKET DEVICE Word 86 bit 3 contains the same value following COMRESET
    - If Word 86 bit 3 was set to one, verify that IDENTIFY DEVICE or IDENTIFY PACKET DEVICE 91 bits 7:0 contains the same value following COMRESET

2.4.8. SSP-08 : Set Features – Read Look-Ahead

2.4.8.1. Device Expected Behavior

NOTE - To test the following requirement, a device must claim support for look-ahead (Word 82 bit 6 set to one in IDENTIFY DEVICE or IDENTIFY PACKET DEVICE data).

Upon receipt of a COMRESET, a device shall maintain the value of look-ahead enable/disable. Specifically, if support for look-ahead is enabled (Word 85 bit 6 set to one in IDENTIFY DEVICE or IDENTIFY PACKET DEVICE data) upon receipt of a COMRESET then the feature shall be enabled after the COMRESET. If support for look-ahead is disabled (Word 85 bit 6 cleared to zero in IDENTIFY DEVICE or IDENTIFY PACKET DEVICE data) upon receipt of a COMRESET then the feature shall be disabled after the COMRESET.

Measurement Requirements

- Check Word 78 bit 6 in IDENTIFY DEVICE or IDENTIFY PACKET DEVICE (set to one)
- Check Word 82 bit 6 (set to one)
- If the above is false, then the test is not applicable
- Otherwise, run the following test

- Check value of Word 85 bit 6
- Issue SET FEATURES to alter setting for read look-ahead enable/disable
- Issue COMRESET and complete OOB sequence
- Check value of Word 85 bit 6

Pass/Fail Criteria

- Verify that IDENTIFY DEVICE or IDENTIFY PACKET DEVICE Word 85 bit 6 contains the same value following COMRESET

2.4.9. SSP-09 : Set Features – Release Interrupt

2.4.9.1. Device Expected Behavior

NOTE - To test the following requirement, a device must claim support for release interrupt (Word 82 bit 7 set to one in IDENTIFY DEVICE or IDENTIFY PACKET DEVICE data).

Upon receipt of a COMRESET, a device shall maintain the value of release interrupt enable/disable. Specifically, if support for release interrupt is enabled (Word 85 bit 7 set to one in IDENTIFY DEVICE or IDENTIFY PACKET DEVICE data) upon receipt of a COMRESET then the feature shall be enabled after the COMRESET. If support for release interrupt is disabled (Word 85 bit 7 cleared to zero in IDENTIFY DEVICE or IDENTIFY PACKET DEVICE data) upon receipt of a COMRESET then the feature shall be disabled after the COMRESET.

Measurement Requirements

- Check Word 78 bit 6 in IDENTIFY DEVICE or IDENTIFY PACKET DEVICE (set to one)
- Check Word 82 bit 7 (set to one)
- If the above is false, then the test is not applicable
- Otherwise, run the following test
  - Check value of Word 85 bit 7
  - Issue SET FEATURES to alter setting for release interrupt enable/disable
  - Issue COMRESET and complete OOB sequence
  - Check value of Word 85 bit 7

Pass/Fail Criteria

- Verify that IDENTIFY DEVICE or IDENTIFY PACKET DEVICE Word 85 bit 7 contains the same value following COMRESET

2.4.10. SSP-10 : Set Features – Service Interrupt

2.4.10.1. Device Expected Behavior

NOTE - To test the following requirement, a device must claim support for service interrupt (Word 82 bit 8 set to one in IDENTIFY DEVICE or IDENTIFY PACKET DEVICE data).

Upon receipt of a COMRESET, a device shall maintain the value of service interrupt enable/disable. Specifically, if support for service interrupt is enabled (Word 85 bit 8 set to one in IDENTIFY DEVICE or IDENTIFY PACKET DEVICE data) upon receipt of a COMRESET then the feature shall be enabled after the COMRESET. If support for service interrupt is disabled (Word 85 bit 8 cleared to zero in IDENTIFY DEVICE or IDENTIFY PACKET DEVICE data) upon receipt of a COMRESET then the feature shall be disabled after the COMRESET.

Measurement Requirements

- Check Word 78 bit 6 in IDENTIFY DEVICE or IDENTIFY PACKET DEVICE (set to one)
- Check Word 82 bit 8 (set to one)
- If the above is false, then the test is not applicable

- Otherwise, run the following test
    - Check value of Word 85 bit 8
    - Issue SET FEATURES to alter setting for service interrupt enable/disable
    - Issue COMRESET and complete OOB sequence
    - Check value of Word 85 bit 8

Pass/Fail Criteria

- Verify that IDENTIFY DEVICE or IDENTIFY PACKET DEVICE Word 85 bit 8 contains the same value following COMRESET

2.4.11. SSP-11 : Set Multiple Mode

2.4.11.1. Device Expected Behavior

This test is not applicable to ATAPI devices.

NOTE - To test the following requirement, a device must claim that the multiple sector setting is valid (Word 59 bit 8 set to one in IDENTIFY DEVICE data).

Upon receipt of a COMRESET, a device shall maintain the block size established by the Set Multiple Mode command. Specifically, the value contained within Word 59 bits 8:0 in IDENTIFY DEVICE data shall be maintained after a COMRESET.

Measurement Requirements

- Check Word 78 bit 6 in IDENTIFY DEVICE (set to one)
- Check Word 59 bit 8 (set to one)
- If the above is false, then the test is not applicable
- Otherwise, run the following test
    - Check value of Word 47 bits 7:0
    - Issue Set Multiple command to change the block size from the value reported in Word 48 bits 7:0
    - Check value of Word 59 bits 8:0
    - Verify correct block size is set due to Set Multiple command
    - Issue COMRESET and complete OOB sequence
    - Check value of Word 59 bits 8:0

Pass/Fail Criteria

- Verify that IDENTIFY DEVICE Word 59 bits 8:0 contains the same value following COMRESET

2.5. Interface Power Management

The Serial ATA Interface Power Management (IPM) test requirements are determined by the requirements of the feature as defined in Serial ATA Revision 2.5.

Some of the test requirements listed in this section require that support for device initiating interface power management and/or host initiating interface power management is claimed by the component for verification of the Expected Behavior. Support for device initiating interface power management can be verified by reading Word 78 bit 3 set to one in IDENTIFY DEVICE or IDENTIFY PACKET DEVICE data. Support for host initiating interface power management can be verified by reading Word 76 bit 9 set to one in IDENTIFY DEVICE or IDENTIFY PACKET DEVICE data. For each test requirement, there will be a note outlining whether support for device initiating interface power management and/or host initiating interface power management is a requirement for testing said test requirement.

A component may claim support for both device initiating interface power management (DIPM) requests and receipt of host initiating power management (HIPM) requests. It is not required to support both types of requests.

The test requirements shall be specified in one of the following ways to determine what type of IPM support is required to test the specified Expected behavior:

- YES (test requirement shall be tested only if the capability is supported as listed in IDENTIFY DEVICE or IDENTIFY PACKET DEVICE data)
- NO (test requirement shall be tested only if the capability is NOT supported as listed in IDENTIFY DEVICE or IDENTIFY PACKET DEVICE data)
- N/A (test requirement shall be tested whether or not the capability is supported as listed in IDENTIFY DEVICE or IDENTIFY PACKET DEVICE data)

2.5.1. IPM-01 : Partial State exit latency

2.5.1.1. Device Expected Behavior

Device or Host IPM Support Required: YES

See section 8.1 of Serial ATA Revision 2.5.

The device exit latency (i.e. COMWAKE response) from the partial state shall start within 10 microseconds of COMWAKE receipt from the host.

Measurement Requirements

- Setup bus analyzer (or scope) for tracing of bus activity & begin tracing
- Check Word 76 bit 9 in IDENTIFY DEVICE or IDENTIFY PACKET DEVICE (set to one)
    - If the above is true, then run the following test (HIPM)
        - Issue PMREQ_P and receive device response
        - Issue COMWAKE and wait for complete wake of device
    - If the above is not true, then check Word 78 bit 3 in IDENTIFY DEVICE or IDENTIFY PACKET DEVICE (set to one)
        - If the above is true, then run the following test (DIPM)
            - Wait for a Partial IPM request from the device
                - NOTE – there is no guaranteed method for causing the device to send a request, some common methods which may cause a request from the device are:
                    - Leave the disk idle (up to 10 seconds)
                    - Issue STANDBY IMMEDIATE command to device
            - Issue COMWAKE and wait for complete wake of device

Pass/Fail Criteria

- Confirm Partial wake sequence completion and COMWAKE timing of being within 10us of COMWAKE receipt from host (use trace to analyze timings)

2.5.2. IPM-02 : Slumber State exit latency

2.5.2.1. Device Expected Behavior

Device or Host IPM Support Required: YES

See section 8.1 of Serial ATA Revision 2.5.

The device exit latency (i.e. COMWAKE response) from the slumber state shall start within 10 milliseconds of COMWAKE receipt from the host.

A method for testing the exit latency is for host software to initiate a COMWAKE on the interface. After initiating the request, the host would record the time until the W bit is set to one within the DIAG field of the SError register.

Measurement Requirements

- Setup bus analyzer (or scope) for tracing of bus activity & begin tracing
- Check Word 76 bit 9 in IDENTIFY DEVICE or IDENTIFY PACKET DEVICE (set to one)
    - If the above is true, then run the following test (HIPM)
        - Issue PMREQ_S and receive device response
        - Issue COMWAKE and wait for complete wake of device
    - If the above is not true, then check Word 78 bit 3 in IDENTIFY DEVICE or IDENTIFY PACKET DEVICE (set to one)
        - If the above is true, then run the following test (DIPM)
            - Wait for a Slumber IPM request from the device
                - NOTE – there is no guaranteed method for causing the device to send a request, some common methods which may cause a request from the device are:
                    - Leave the disk idle (up to 10 seconds)
                    - Issue STANDBY IMMEDIATE command to device
            - Issue COMWAKE and wait for complete wake of device

Pass/Fail Criteria

- Confirm Slumber wake sequence completion and COMWAKE timing of being within 10ms of COMWAKE receipt from host (use trace to analyze timings)

2.5.3. IPM-03 : Speed matching upon resume

2.5.3.1. Device Expected Behavior

Device or Host IPM Support Required: YES

See section 8.3.3.2 of Serial ATA Revision 2.5.

The device signaling speed upon returning from a partial or slumber state shall match the speed prior to entering the partial or slumber state.

Measurement Requirements

- Check Word 76 bit 9 in IDENTIFY DEVICE or IDENTIFY PACKET DEVICE (set to one)
    - If the above is true, then run the following test (HIPM)
        - Check the SPD field (bits 7:4) of the SStatus register
        - Issue PMREQ_P or PMREQ_S and receive device response
        - Issue COMWAKE and wait for complete wake of device
        - Check the SPD field (bits 7:4) of the SStatus register
    - If the above is not true, then check Word 78 bit 3 in IDENTIFY DEVICE or IDENTIFY PACKET DEVICE (set to one)
        - If the above is true, then run the following test (DIPM)
            - Check the SPD field (bits 7:4) of the SStatus register
            - Wait for an IPM request from the device
                - NOTE – there is no guaranteed method for causing the device to send a request, some common methods which may cause a request from the device are:
                    - Leave the disk idle (up to 10 seconds)
                    - Issue STANDBY IMMEDIATE command to device
            - Issue COMWAKE and wait for complete wake of device

- Check the SPD field (bits 7:4) of the SStatus register

Pass/Fail Criteria

- Verify that the SPD field contains the same value before and after the power management sequence (HIPM support required)
- NOTE – if the device does not support HIPM but does support DIPM and no request was issued by the device, then the device shall not be failed for this test requirement.

2.5.4. IPM-04 : Lack of IPM support

2.5.4.1. Device Expected Behavior

Device IPM Support Required: N/A
Host IPM Support Required: NO

See section 9.6 of Serial ATA Revision 2.5.

If a device does not support host interface power management (Word 76 bit 9 cleared to zero in IDENTIFY DEVICE or IDENTIFY PACKET DEVICE data), upon receipt of a PMREQ_P or PMREQ_S the device shall respond with a PMNAK.

Measurement Requirements

- Setup bus analyzer (or scope) for tracing of bus activity & begin tracing
- Check Word 76 bit 9 in IDENTIFY DEVICE or IDENTIFY PACKET DEVICE (cleared to zero)
- If the above is true, then run the following test
    - Issue PMREQ_P or PMREQ_S and receive device response

Pass/Fail Criteria

- Verify that PMNAK is received (use trace to verify PMNAK receipt)

2.5.5. IPM-05 : Device response to PMREQ_P

2.5.5.1. Device Expected Behavior

Device IPM Support Required: N/A
Host IPM Support Required: YES

See section 9.6 of Serial ATA Revision 2.5.

If a device claims support for host interface power management (Word 76 bit 9 set to one in IDENTIFY DEVICE or IDENTIFY PACKET DEVICE data), upon receipt of a PMREQ_P the following are valid device responses:

- respond with four PMACK primitives and place the device Phy layer into the partial state
- respond with PMNAK until SYNC is received from the host, no device Phy layer power transition shall occur.

Measurement Requirements

- Setup bus analyzer (or scope) for tracing of bus activity & begin tracing
- Check Word 76 bit 9 in IDENTIFY DEVICE or IDENTIFY PACKET DEVICE (set to one)
- If the above is true, then run the following test
    - Issue PMREQ_P and receive device response

Pass/Fail Criteria

- Verify that PMNAK or at least 4 total PMACKs are received (use trace to verify device response)

2.5.6. IPM-06 : Device response to PMREQ_S

2.5.6.1. Device Expected Behavior

Device IPM Support Required: N/A
Host IPM Support Required: YES

See section 9.6 of Serial ATA Revision 2.5.

If a device claims support host interface power management (Word 76 bit 9 set to one in IDENTIFY DEVICE or IDENTIFY PACKET DEVICE data), upon receipt of a PMREQ_S the following are valid device responses:

- respond with four PMACK primitives and place the device Phy layer into the slumber state
- respond with PMNAK until SYNC is received from the host, no device Phy layer power transition shall occur.

Measurement Requirements

- Setup bus analyzer (or scope) for tracing of bus activity & begin tracing
- Check Word 76 bit 9 in IDENTIFY DEVICE or IDENTIFY PACKET DEVICE (set to one)
- If the above is true, then run the following test
    - Issue PMREQ_S and receive device response

Pass/Fail Criteria

- Verify that PMNAK or at least 4 total PMACKs are received (use trace to verify device response)

2.5.7. IPM-07 : Default setting for device initiated requests

2.5.7.1. Device Expected Behavior

Device Initiated IPM Support Required: YES
Host IPM Support Required: N/A

See section 13.2.4.3 of Serial ATA Revision 2.5.

Support for device power management shall be disabled (Word 79 bit 3 cleared to zero in IDENTIFY DEVICE or IDENTIFY PACKET DEVICE data) by default. A device shall not issue Partial/Slumber requests unless this feature has been enabled by the host as a result of a SET FEATURES command.

Measurement Requirements

- Power on device
- Check Word 78 bit 3 in IDENTIFY DEVICE or IDENTIFY PACKET DEVICE (set to one)
- Check Word 79 bit 3 in IDENTIFY DEVICE or IDENTIFY PACKET DEVICE (cleared to zero)
- Issue SET FEATURES (Sector Count = 03h) to enable device support for initiating power management
- Issue COMRESET and complete OOB sequence
- Check Word 79 bit 3 in IDENTIFY DEVICE or IDENTIFY PACKET DEVICE

Pass/Fail Criteria

- Verify that Word 79 bit 3 in IDENTIFY DEVICE or IDENTIFY PACKET DEVICE is cleared to zero in both instances above

2.6. Mechanical - Cable Assembly - Standard Internal

If both ends of a cable have identical connector types, then the mechanical tests will only need to be verified on one end of the cable.

The tester shall ensure that the cable assemblies are clearly labeled so that each line in a cable assembly can be uniquely identified. For a standard internal cable assembly, a suggested labeling method is:

- Each of the cables is labeled
- The two ends of the cable are also labeled, e.g. Recept_A, Recept_B
- The signal lines use the pin names provided in the specification. For standard internal connectors table 2 and Figure 29 of section 6.1.3.2, in the Serial ATA Revision 2.5 specification labels the individual signal lines as S1, S2, S3, …S6, S7. It also defines Pair A as being the combination of signal lines S2 and S3, while Pair B is defined as the combination of signal lines S5 and S6.

If a family of cables is being tested, all tests shall be performed on only one of the cables (longest or shortest).

2.6.1. MCI-01 : Visual and Dimensional Inspections

2.6.1.1. Cable Assembly Expected Behavior

See section 6.1.10.2, Table 5 of the Serial ATA Revision 2.5 specification.

Measurement Requirements

See section 6.1.10.2, Table 5 and section 6.1.4, Figures 30 and 31 of the Serial ATA Revision 2.5 specification.

Pass/Fail Criteria

- The height of the slot (for the device plug tongue) shall be 1.40 +- 0.08 mm (Figure 30, section A-A).
- The width of the slot (for the device plug tongue) shall be 10.57 +- 0.08 mm (Figure 30).
- The height of the slot for the device plug key shall be 2.40 +- 0.08 mm (Figure 30).
- The width of the slot for the device plug key shall be 1.31 +- 0.05 mm (Figure 30).
- For a non-latching cable the width of the cable retention feature (bump) shall be 1.50 +- 0.20 mm (Figure 30).
- For a latching cable there shall be no cable retention feature (bump), as shown in Figure 31.
- For a latching cable the distance from the slot to the top surface of the receptacle shall be 1.45 +- 0.05 mm (Figure 31).
- For a latching cable the latch engagement feature shall be able to deflect below 1.45 mm (Figure 31).

2.6.2. MCI-02 : Insertion Force (Latching and Non-Latching)

2.6.2.1. Cable Assembly Expected Behavior

See section 6.1.10.2, Table 5 of the Serial ATA Revision 2.5 specification.

Measurement Requirements

See section 6.1.10.2, Table 5 of the Serial ATA Revision 2.5 specification.

For Serial ATA Interoperability Program testing a total of 20 insertion/removal force cycles shall be used for this measurement.

Pass/Fail Criteria

- 45 N Max.

2.6.3. MCI-03 : Removal Force (Non-Latching)

2.6.3.1. Cable Assembly Expected Behavior

See section 6.1.10.2, Table 5 of the Serial ATA Revision 2.5 specification.

Measurement Requirements
See section 6.1.10.2, Table 5 of the Serial ATA Revision 2.5 specification.

For Serial ATA Interoperability Program testing a total of 20 insertion/removal force cycles shall be used for this measurement.

Pass/Fail Criteria
- 10 N Min. through 20 cycles

2.6.4. MCI-04 : Removal Force (Latching)

2.6.4.1. Cable Assembly Expected Behavior

See section 6.1.10.2, Table 5 of the Serial ATA Revision 2.5 specification.

Measurement Requirements
See section 6.1.10.2, Table 5 of the Serial ATA Revision 2.5 specification.

For Serial ATA Interoperability Program testing a total of 20 insertion/removal force cycles shall be used for this measurement.

Pass/Fail Criteria
- No damage and no disconnect through 20 mating cycles

2.6.5. MCI-05 : Cable Pull-out

2.6.5.1. Cable Assembly Expected Behavior

See section 6.1.10.2, Table 5 of the Serial ATA Revision 2.5 specification.

Measurement Requirements
See section 6.1.10.2, Table 5 of the Serial ATA Revision 2.5 specification.

Pass/Fail Criteria
- No physical damage

2.7. Electrical - Cable Assembly – Standard Internal

The Serial ATA specification currently specifies a 20-80% rise time for the test pulse. However, test equipment rise time filters are usually programmed with 10-90% values. Thus, some conversion is needed. An example conversion for a 70ps 20-80% would be to set up the rise time filter for a 105ps 10-90% rise time.

The tester shall ensure that the cable assemblies are clearly labeled so that each line in a cable assembly can be uniquely identified. For a standard internal cable assembly, a suggested labeling method is:
- Each of the cables is labeled
- The two ends of the cable are also labeled, e.g. Recept_A, Recept_B
- The signal lines use the pin names provided in the specification. For standard internal connectors table 2 and Figure 29 of section 6.1.3.2, in the Serial ATA Revision 2.5

specification labels the individual signal lines as S1, S2, S3, …S6, S7. It also defines Pair A as being the combination of signal lines S2 and S3, while Pair B is defined as the combination of signal lines S5 and S6.

If a family of cables is being tested, all tests shall be performed on both the longest and shortest lengths unless otherwise noted in a specific test.

Tester must save all the calibration data (i.e. screen shot) that is done daily at a minimum, if not every cable evaluation. Valid calibration data must be available per product for review, even if the same calibration data (i.e. daily) is used for multiple products. It is required that calibration be completed for this area of testing to ensure consistent measurements and environment impacts.

2.7.1. SI-01 : Mated Connector Impedance

2.7.1.1. Cable Assembly Expected Behavior

See section 6.3.1.1, Table 10 of the Serial ATA Revision 2.5 specification.

The test shall be performed on both ends of the cable assembly, for each differential pair of the assembly.

Measurement Requirements
See section 6.3.2.4, Table 14, Procedure P1 of the Serial ATA Revision 2.5 specification.

After completing the common procedures (and before doing the measurement) the instrument rise time shall be set or the results filtered for a minimum of 55 ps to a maximum of 70 ps (20-80%) system rise time. The system rise time shall be set as close to 70 ps (20-80%) as practical.

Pass/Fail Criteria
- Mated Connector Differential Impedance 100 Ohms ±15%

2.7.2. SI-02 : Cable Absolute Impedance

2.7.2.1. Cable Assembly Expected Behavior

See section 6.3.1.1, Table 10 of the Serial ATA Revision 2.5 specification.

The test shall be performed on one end of the cable assembly, for each differential pair of the assembly.

Measurement Requirements
See section 6.3.2.4, Table 14, Procedure P2 of the Serial ATA Revision 2.5 specification.

After completing the common procedures (and before doing the measurement) the instrument rise time shall be set or the results filtered for a minimum of 55 ps to a maximum of 70 ps (20-80%) system rise time. The system rise time shall be set as close to 70 ps (20-80%) as practical.

Pass/Fail Criteria
- Cable Absolute Differential Impedance 100 Ohms ±10%

2.7.3. SI-03 : Cable Pair Matching

2.7.3.1. Cable Assembly Expected Behavior

See section 6.3.1.1, Table 10 of the Serial ATA Revision 2.5 specification.

The test shall be performed on one end of the cable assembly, for each differential pair of the assembly.

Measurement Requirements
See section 6.3.2.4, Table 14, Procedure P3 of the Serial ATA Revision 2.5 specification.

After completing the common procedures (and before doing the measurement) the instrument rise time shall be set or the results filtered for a minimum of 55 ps to a maximum of 70 ps (20-80%) system rise time. The system rise time shall be set as close to 70 ps (20-80%) as practical.

Pass/Fail Criteria
- Cable Pair Matching Impedance ±5 Ohms

2.7.4. SI-04 : Common Mode Impedance

2.7.4.1. Cable Assembly Expected Behavior

See section 6.3.1.1, Table 10 of the Serial ATA Revision 2.5 specification.

Measurement Requirements
See section 6.3.2.4, Table 14, Procedure P4 of the Serial ATA Revision 2.5 specification.

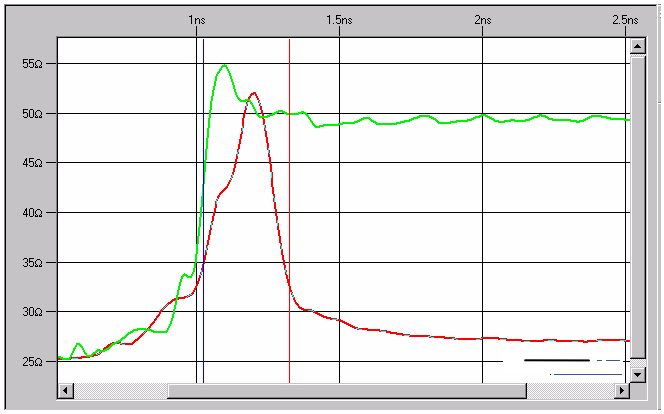

Figure – 1 Example result showing the last vestige of the connector response (at 1.8 ns)

The test shall be performed on one end of the cable assembly, for each differential pair of the assembly.

After completing the common procedures (and before doing the measurement) the instrument rise time shall be set or the results filtered for a minimum of 55 ps to a maximum of 70 ps (20-80%) system rise time. The system rise time shall be set as close to 70 ps (20-80%) as practical.

Pass/Fail Criteria
- Common Mode Impedance 25 - 40 ohms

2.7.5. SI-05 : Differential Rise Time

2.7.5.1. Cable Assembly Expected Behavior

See section 6.3.1.1, Table 10 of the Serial ATA Revision 2.5 specification.

Measurement Requirements
See section 6.3.2.4, Table 14, Procedure P8 of the Serial ATA Revision 2.5 specification.

The test shall be performed in one direction on the cable assembly, for each differential pair of the assembly.

Pass/Fail Criteria

- Maximum Rise Time 85 ps (20-80%)

2.7.6. SI-06 : Intra-Pair Skew

2.7.6.1. Cable Assembly Expected Behavior

See section 6.3.1.1, Table 10 of the Serial ATA Revision 2.5 specification.

The test shall be performed in one direction on the cable assembly, for each differential pair of the assembly.

Measurement Requirements

See section 6.3.2.4, Table 14, Procedure P10 of the Serial ATA Revision 2.5 specification.

All cables and all adapters must be de-skewed just prior to performing the measurement. Note that the inclusion of the adapters in calibrations for other tests may not be correct.

Pass/Fail Criteria

- Maximum Intra-Pair Skew 10 ps

2.7.7. SI-07 : Insertion Loss

2.7.7.1. Cable Assembly Expected Behavior

See section 6.3.1.1, Table 10 of the Serial ATA Revision 2.5 specification.

The test shall be performed in one direction on the cable assembly, for each differential pair of the assembly.

If a family of cables is being tested, only the longest length is tested for this requirement.

Measurement Requirements

See section 6.3.2.4, Table 14, Procedure P5 of the Serial ATA Revision 2.5 specification.

Pass/Fail Criteria

- Maximum Insertion Loss of Cable (10-4500 MHz) 6 dB

2.7.8. SI-08 : Differential to Differential Crosstalk: NEXT

2.7.8.1. Cable Assembly Expected Behavior

See section 6.3.1.1, Table 10 of the Serial ATA Revision 2.5 specification.

The test shall be performed on both ends of the cable assembly, but only needs to be measured in one direction on each end (for example, with the Tx pair as the aggressor, and the Rx pair as the receiver).

Measurement Requirements

See section 6.3.2.4, Table 14, Procedure P6 of the Serial ATA Revision 2.5 specification.

If a time-based test equipment is used to measure the NEXT, it must use a acquisition window that is at least 4 times the propagation delay of the cable (electrical length).

For test adapters comprising of 2 plugs to SMA and 1 receptacle to SMA adapters, each combination of plug / receptacle shall have a NEXT performance better than -36dB. The performance measurement of this adapter combination must be made and saved on a daily basis, or each time the setup is restored. In the event of a component failure, re-confirm that the adapter performance meets this requirement. For this measurement, the tester must continue to follow the same procedure for making a NEXT measurement on a component (see Procedure P6).

Pass/Fail Criteria

- Maximum Crosstalk: NEXT (10-4500 MHz) -26 dB

2.7.9. SI-09 : Inter-Symbol Interference

2.7.9.1. Cable Assembly Expected Behavior

See section 6.3.1.1, Table 10 of the Serial ATA Revision 2.5 specification.

The test shall be performed in one direction on the cable assembly, for each differential pair of the assembly.

If a family of cables is being tested, only the longest length is tested for this requirement.

Measurement Requirements

See section 6.3.2.4, Table 14, Procedure P9 of the Serial ATA Revision 2.5 specification.

Pass/Fail Criteria

- Maximum Inter-Symbol Interference 50 ps

2.8. Mechanical – Device - Standard Internal Connector

2.8.1. MDI-01 : Connector Location

2.8.1.1. Device Expected Behavior

See section 6.1.2 of the Serial ATA Revision 2.5 specification.

Measurement Requirements

- For a 5.25” optical device see section 6.1.2, Figure 18 of the Serial ATA Revision 2.5 specification.
- For a 5.25” non-optical device see either section 6.1.2, Figure 18 or section 6.1.2, Figure 19 of the Serial ATA Revision 2.5 specification.
- For a 3.5” side mounted device see section 6.1.2, Figure 20 of the Serial ATA Revision 2.5 specification.
- For a 3.5” bottom mounted device see section 6.1.2, Figure 21 of the Serial ATA Revision 2.5 specification.
- For a 2.5” side mounted device see section 6.1.2, Figure 22 of the Serial ATA Revision 2.5 specification.
- For a 2.5” bottom mounted device see section 6.1.2, Figure 23 of the Serial ATA Revision 2.5 specification.

Pass/Fail Criteria

- For a 5.25” optical device:
    - From the bottom surface of the drive to the top of the tongue of the SATA plug.
      10.00 +- 0.38 mm

- Parallelism of the top of the tongue of the SATA plug vs. the bottom surface of the drive.
  0.40 mm
- From the centerline of the drive to the centerline of the SATA plug.
  25.00 +- 0.38 mm
- From the back surface of the drive (i.e. the “end of the device factor”) to the base of the tongue of the SATA plug.
  4.90 +- 0.50 mm

- For a 5.25” non-optical device: If the device follows section 6.1.2, Figure 18 then use the Pass/Fail criteria for a “*5.25” optical drive*”. If the device does not follow section 6.1.2, Figure 18 then:
  - From the bottom surface of the drive to the top of the tongue of the SATA plug.
    3.50 +- 0.38 mm
  - Parallelism of the top of the tongue of the SATA plug vs. the bottom surface of the drive.
    0.40 mm
  - From the centerline of the drive to the centerline of the SATA plug.
    42.90 +- 0.38 mm
  - From the back surface of the drive (i.e. the “end of the device factor”) to the base of the tongue of the SATA plug.
    4.90 +- 0.50 mm
- For a 3.5” side mounted device:
  - From the centerline of the mounting holes to the top of the tongue of the SATA plug.
    2.85 +- 0.38 mm
  - Parallelism of the top of the tongue of the SATA plug vs. the bottom surface of the drive.
    0.25 mm
  - From the centerline of the drive to the centerline of the SATA plug.
    20.68 +- 0.38 mm
  - From the centerline of the mounting holes to the base of the tongue of the SATA plug.
    23.60 +- 0.50 mm
- For a 3.5” bottom mounted device:
  - From the bottom surface of the drive to the top of the tongue of the SATA plug.
    3.50 +- 0.38 mm
  - Parallelism of the top of the tongue of the SATA plug vs. the bottom surface of the drive.
    0.25 mm
  - From the centerline of the drive to the centerline of the SATA plug.
    20.68 +- 0.38 mm
  - From the centerline of the mounting holes to the base of the tongue of the SATA plug.
    36.38 +- 0.50 mm
- For a 2.5” side mounted device:
  - From the centerline of the mounting holes to the top of the tongue of the SATA plug.
    0.50 +- 0.38 mm
  - Parallelism of the top of the tongue of the SATA plug vs. the bottom surface of the drive.
    0.25 mm
  - From the centerline of the drive to the centerline of the SATA plug.
    4.80 +- 0.38 mm
  - From the centerline of the mounting holes to the base of the tongue of the SATA plug.
    9.40 +- 0.50 mm

- For a 2.5” bottom mounted device:
    - From the bottom surface of the drive to the top of the tongue of the SATA plug.
      3.50 +- 0.38 mm
    - Parallelism of the top of the tongue of the SATA plug vs. the bottom surface of the drive.
      0.25 mm
    - From the centerline of the drive to the centerline of the SATA plug.
      4.80 +- 0.38 mm
    - From the centerline of the mounting holes to the base of the tongue of the SATA plug.
      9.40 +- 0.50 mm

2.8.2. MDI-02 : Visual and Dimensional Inspections

2.8.2.1. Device Expected Behavior

See section 6.1.10.2, Table 5 of the Serial ATA Revision 2.5 specification.

Measurement Requirements
See section 6.1.10.2, Table 5; section 6.1.2, Figure 26; and section 6.1.3.1, Figures 27 and 28 of the Serial ATA Revision 2.5 specification.

Pass/Fail Criteria
- The thickness of the device plug tongue shall be 1.23 +- 0.05 mm (Figure 28, section C-C).
- If the “Optional Wall” of Figure 28 is present then the distance from the device plug tongue to the wall shall be 1.58 +- 0.08 mm (Figure 28, section B-B).
- If the “Optional Wall” of Figure 28 is not present then there shall be a minimum of a 1.5 mm keep out zone from Datum A of Figure 26 to the nearest obstruction.
- The combined width of the power and signal segments shall be 33.39 +- 0.08 mm (Figure 27).
- The separation between the power and signal segments shall be 2.41 +- 0.05 mm (Figure 27).

2.9. Mechanical – Device - Power Connector

2.9.1. MDP-01 : Visual and Dimensional Inspections

2.9.1.1. Device Expected Behavior

See section 6.1.10.2, Table 5 of the Serial ATA Revision 2.5 specification.

Measurement Requirements
See section 6.1.10.2, Table 5; section 6.1.2, Figure 26; and section 6.1.3.1, Figures 27 and 28 of the Serial ATA Revision 2.5 specification.

Pass/Fail Criteria
- The thickness of the device plug tongue shall be 1.23 +- 0.05 mm (Figure 28, section C-C).
- If the “Optional Wall” of Figure 28 is present then the distance from the device plug tongue to the wall shall be 1.58 +- 0.08 mm (Figure 28, section B-B).
- If the “Optional Wall” of Figure 28 is not present then there shall be a minimum of a 1.5 mm keep out zone from Datum A of Figure 26 to the nearest obstruction.

2.10. Phy General Requirements

2.10.1. PHY-01 : Unit Interval

2.10.1.1. Device Expected Behavior

See section 7.2.2.1.3 of Serial ATA Revision 2.5.

Measurement Requirements
See section 7.4.11 of Serial ATA Revision 2.5.

For components which support 3Gb/s, this requirement must be tested at both interface rates (1.5Gb/s and 3Gb/s).

Pass/Fail Criteria

- Mean Unit Interval measured between 666.4333ps (min) to 670.2333ps (max) (for components running at 1.5Gb/s)
- Mean Unit Interval measured between 333.2167ps (min) to 335.1167ps (max) (for components running at 3Gb/s)
- The values above shall be based on at least 100,000 UIs (covers at least one SSC profile)

2.10.2. PHY-02 : Frequency Long Term Stability

2.10.2.1. Device Expected Behavior

See section 7.2.2.1.4 of Serial ATA Revision 2.5.

Measurement Requirements
See section 7.4.6 of Serial ATA Revision 2.5.

This test is only run once at the maximum interface rate of the component (1.5Gb/s or 3Gb/s).

The execution of this test must include use of the low pass filter defined within section 7.4.11 of Serial ATA Revision 2.5, whether SSC is supported or not by the component.

If support of SSC is claimed by the device, the reported result must be the maximum value from the range of SSC modulation deviation.

Pass/Fail Criteria

- f_{tol} measured between -350ppm and 350ppm

2.10.3. PHY-03 : Spread-Spectrum Modulation Frequency

2.10.3.1. Device Expected Behavior

See sections 7.2.2.1.5 and 7.3.3 of Serial ATA Revision 2.5.

This test requires support for Spread Spectrum Clocking (SSC), which is optional.

Measurement Requirements
See section 7.4.11 of Serial ATA Revision 2.5.

This test is only run once at the maximum interface rate of the component (1.5Gb/s or 3Gb/s).
Pass/Fail Criteria

- f_{SSC} measured between 30kHz and 33kHz
- The value above shall be based on at least 10 complete SSC cycles

2.10.4. PHY-04 : Spread-Spectrum Modulation Deviation

2.10.4.1. Device Expected Behavior

See sections 7.2.2.1.6 and 7.3.3 of Serial ATA Revision 2.5.

This test requires support for Spread Spectrum Clocking (SSC), which is optional.

Measurement Requirements
See section 7.4.11 of Serial ATA Revision 2.5.

This test is only run once at the maximum interface rate of the component (1.5Gb/s or 3Gb/s).

The value reported as the result must be the single total range value (i.e. max to min) of the SSC modulation deviation.

Pass/Fail Criteria

- SSC_{tol} measured between -5000ppm and +0ppm

2.11. Phy Transmitter Requirements

During the testing execution for all TX test requirements, it is essential that the device under test be able to complete an initial OOB sequence through the device COMWAKE. This is to allow device calibration to occur prior to and/or during the initial power on and detect sequences.

2.11.1. TX-01 : Pair Differential Impedance

2.11.1.1. Device Expected Behavior

See section 7.2.2.2.1 of Serial ATA Revision 2.5.

Measurement Requirements
See section 7.4.22 of Serial ATA Revision 2.5.

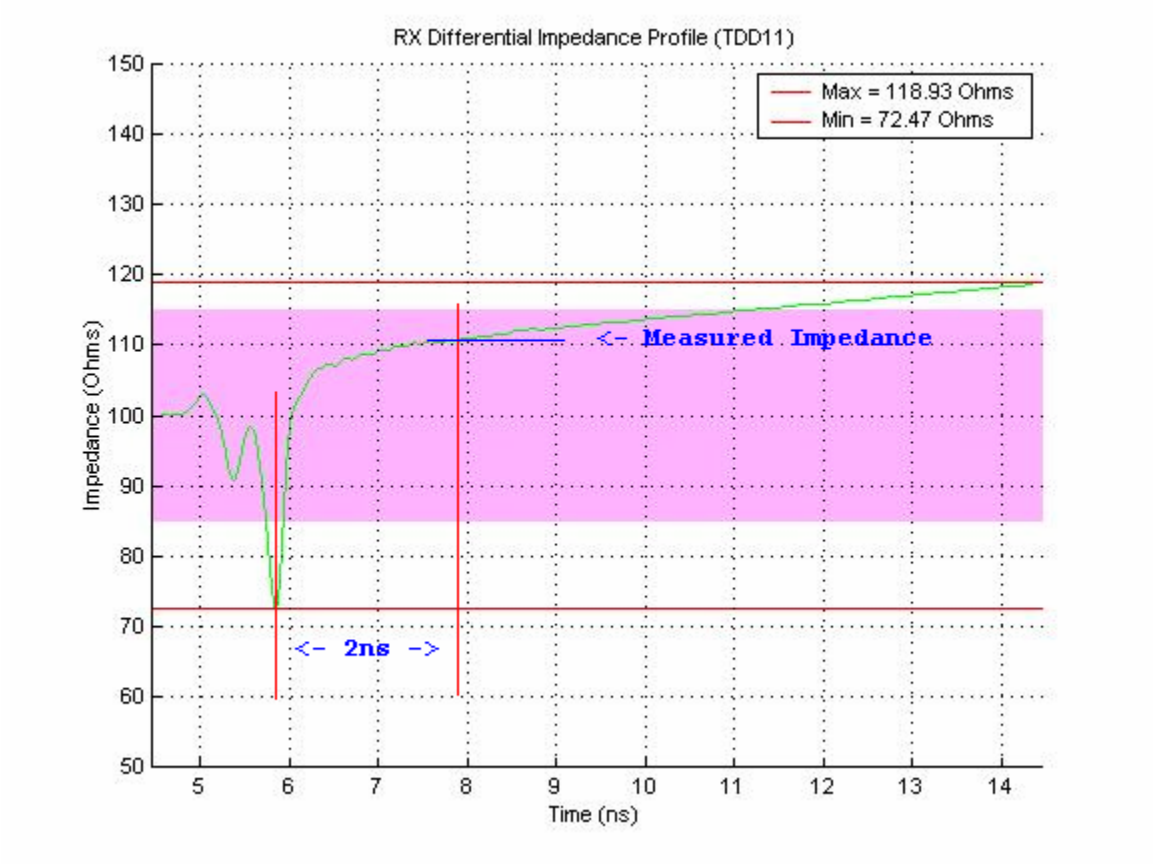

Figure 2 – Example impedance measurement point

While making the measurement, only consider the impedance at a point 2ns past the bottom of the last major capacitive excursion (i.e. dip) that is known to be inside the ASIC device. See Figure 2 above for an example.

For components which support 3Gb/s, this requirement must be tested at 1.5Gb/s.

Pass/Fail Criteria

- Pair differential impedance measured between 85 ohms and 115 ohms (for components running at 1.5Gb/s)

2.11.2. TX-02 : Single-Ended Impedance

2.11.2.1. Device Expected Behavior

See section 7.2.2.2.2 of Serial ATA Revision 2.5.

Measurement Requirements

See section 7.4.23 of Serial ATA Revision 2.5.

For components which support 3Gb/s, this requirement must be tested at 1.5Gb/s.

Pass/Fail Criteria

- $Z_{s\text{-}eTX}$ measured to be at least 40 ohms (for components running at 1.5Gb/s)

2.11.3. TX-03 : Differential Mode Return Loss

2.11.3.1. Device Expected Behavior

See section 7.2.2.2.3 of Serial ATA Revision 2.5.

Measurement Requirements
See section 7.4.10 of Serial ATA Revision 2.5.

Calibrate to the end of the SMA cables, but do NOT include (de-embedd) the SMA to SATA PCB and the SATA connector, so the board and the SATA connector are INCLUDED with the device measurement.

This test requirement is only applicable to components running at 3Gb/s.

Pass/Fail Criteria

- $RL_{DD11,TX}$ measured per the values in Table 2 (for components running at 3Gb/s)

Table 2 - TX Differential Mode Return Loss

Frequency	Minimum (dB)
150MHz-300MHz	14
300MHz-600MHz	8
600MHz-1.2GHz	6
1.2GHz-2.4GHz	6
2.4GHz-3.0GHz	3
3.0GHz-5.0GHz	1

2.11.4. TX-04 : Common Mode Return Loss

2.11.4.1. Device Expected Behavior

See section 7.2.2.2.4 of Serial ATA Revision 2.5.

Measurement Requirements
See section 7.4.10 of Serial ATA Revision 2.5.

Calibrate to the end of the SMA cables, but do NOT include (de-embedd) the SMA to SATA PCB and the SATA connector, so the board and the SATA connector are INCLUDED with the device measurement.

This test requirement is only applicable to components running at 3Gb/s.

Pass/Fail Criteria

- $RL_{CC11,TX}$ measured per the values in Table 3 (for components running at 3Gb/s)

Table 3 - TX Common Mode Return Loss

Frequency	Minimum (dB)
150MHz-300MHz	8
300MHz-600MHz	5
600MHz-1.2GHz	2
1.2GHz-2.4GHz	2
2.4GHz-3.0GHz	2
3.0GHz-5.0GHz	1

2.11.5. TX-05 : Impedance Balance

2.11.5.1. Device Expected Behavior

See section 7.2.2.2.5 of Serial ATA Revision 2.5.

Measurement Requirements
See section 7.4.10 of Serial ATA Revision 2.5.

This test requirement is only applicable to components running at 3Gb/s.

Pass/Fail Criteria

- $RL_{DC11,TX}$ measured per the values in Table 4 (for components running at 3Gb/s)

Table 4 - TX Impedance Balance

Frequency	Minimum (dB)
150MHz-300MHz	30
300MHz-600MHz	20
600MHz-1.2GHz	10
1.2GHz-2.4GHz	10
2.4GHz-3.0GHz	4
3.0GHz-5.0GHz	4

2.12. Phy Transmitted Signal Requirements

During the testing execution for all TSG test requirements, it is essential that the device under test be able to complete an initial OOB sequence through the device COMWAKE prior to transmission of a BIST FIS or initiation of the BIST mode sequence. This is to allow device calibration to occur prior to and/or during the initial power on and detect sequences.

Tester must save all the calibration data (i.e. screen shot) that is done daily at a minimum, if not every device evaluation. Valid calibration data must be available per product for review, even if the same calibration data (i.e. daily) is used for multiple products. It is required that calibration be completed for this area of testing to ensure consistent measurements and environment impacts.

2.12.1. TSG-01 : Differential Output Voltage

2.12.1.1. Device Expected Behavior

See section 7.2.2.3.1 of Serial ATA Revision 2.5.

Measurement Requirements
See section 7.4.4 and section 7.4.2.1 of Serial ATA Revision 2.5.

For components which support 3Gb/s, this requirement must be tested at both interface rates (1.5Gb/s and 3Gb/s).

For the interests of the Interoperability Program, the measurements will only be taken to verify this requirement at the minimum limit. Within the specification, there are two options for measuring the minimum:

- Vtest = min(DH, DM, VtestLBP)
- Vtest = min(DH, DM, VtestAPP)

Note that gathering a minimum result from either of the options above is acceptable. It is not required to report a result for both.

In the interest of ensuring products to meet some metric for system interoperability at the maximum limit, the maximum value received out of the minimum measurement will be verified to not exceed 800mV using the formulas below, where DH, DM, VtestLBP, and VtestAPP are the same values used for the above minimum measurement.

- Vtest(max) = max(DH, DM, VtestLBP)
- Vtest(max) = max(DH, DM, VtestAPP)

Pass/Fail Criteria

- V_{diffTX} (min) measured to be (for devices running at 1.5Gb/s):
  - Minimum : VTest at least 400 mVppd
  - The maximum result (Vtest(max)) of the minimum measurement must not exceed 800mV

- V_{diffTX} (min) measured to be (for devices running at 3Gb/s):
  - Minimum : VTest at least 400 mVppd
  - The maximum result (Vtest(max)) of the minimum measurement must not exceed 800mV

2.12.2. TSG-02 : Rise/Fall Time

2.12.2.1. Device Expected Behavior

See section 7.2.2.3.3 of Serial ATA Revision 2.5.

Measurement Requirements
See section 7.4.3 of Serial ATA Revision 2.5.

For components which support 3Gb/s, this requirement must be tested at both interface rates (1.5Gb/s and 3Gb/s).

There are several different patterns defined within the specification and are intended to be used to verify this requirement. In order to ensure efficient test time of products within the Interoperability Testing, testing of this requirement will be limited to the High Frequency Test Pattern (HFTP) as defined in the SATA Revision 2.5 specification.

Pass/Fail Criteria

- $t_{20\text{-}80TX}$ measured per the Max values in Table 5
- Note: Failures at minimum rate have not been shown to affect interoperability and will not be included in determining pass/fail for Interop testing

Table 5 - TX Rise/Fall Time

Limit	Time @ 1.5Gb/s (ps (UI))	Time @ 3Gb/s (ps (UI))
Min 20-80%	100 (0.15)	67 (0.20)
Max 20-80%	273 (0.41)	136 (0.41)

2.12.3. TSG-03 : Differential Skew

2.12.3.1. Device Expected Behavior

See section 7.2.2.3.4 of Serial ATA Revision 2.5.

Measurement Requirements
See section 7.4.12 of Serial ATA Revision 2.5.

This test is only run once at the maximum interface rate of the component (1.5Gb/s or 3Gb/s).

Please note that this requires measuring the mean skew of TX+ rise to TX- fall and the mean skew of TX+ fall to TX- rise, as stated in 7.2.2.3.4, and then computing the Differential Skew = average of the magnitude (absolute value) of the two mean skews. This removes the effect of rise-fall imbalance from the skew measurement.

Pass/Fail Criteria

- t_{skewTX} measured at a maximum of 20 ps

2.12.4. TSG-04 : AC Common Mode Voltage

2.12.4.1. Device Expected Behavior

See section 7.2.2.3.5 of Serial ATA Revision 2.5.

Measurement Requirements
See section 7.4.17 of Serial ATA Revision 2.5.

This test requirement is only applicable to components running at 3Gb/s.

Pass/Fail Criteria

- $V_{cm,acTX}$ measured at a maximum of 50 mVp-p (for components running at 3Gb/s)

2.12.5. TSG-05 : Rise/Fall Imbalance

2.12.5.1. Device Expected Behavior

See section 7.2.2.3.9 of Serial ATA Revision 2.5.

Measurement Requirements
See section 7.4.16 of Serial ATA Revision 2.5.

This test requirement is only applicable to components running at 3Gb/s.

Pass/Fail Criteria

- Mean R/F_{bal} measured at a maximum of 20% (for components running at 3Gb/s)
- The value above shall be based on at least 10,000 UIs

2.12.6. TSG-06 : Amplitude Imbalance

2.12.6.1. Device Expected Behavior

See section 7.2.2.3.10 of Serial ATA Revision 2.5.

Measurement Requirements
See section 7.4.15 of Serial ATA Revision 2.5.

This test requirement is only applicable to components running at 3Gb/s.

Pass/Fail Criteria

- Mean Amp_{bal} measured at a maximum of 10% (for components running at 3Gb/s)
- The value above shall be based on at least 10,000 UIs

2.12.7. TSG-07 : TJ at Connector, Data, 5UI

2.12.7.1. Device Expected Behavior

See sections 7.2.2.3.11 and 7.3 of Serial ATA Revision 2.5.

Measurement Requirements
See section 7.4.8 of Serial ATA Revision 2.5.

This test is optional for all components. For components which support 3Gb/s, this requirement would be tested at 1.5Gb/s.

The loop damping factor for the reference PLLs is required to be 0.707.

There are several different patterns defined within the specification and are intended to be used to verify this requirement. In order to ensure efficient test time of products within the Interoperability Testing, testing of this requirement will be limited to the following patterns as defined in the SATA Revision 2.5 specification: High Frequency Test Pattern (HFTP), and Lone Bit Pattern (LBP). It is optional to additionally test using the Simultaneous Switching Outputs Pattern (SSOP) as a third pattern.

For this test, the methodology of obtaining the result must follow a filtered TIE based method, similar to that for obtaining 3Gb/s results for TSG-11 and TSG-12. In the past, an N-cycle method was used but is no longer preferred for the use of the interoperability testing.

Pass/Fail Criteria
- TJ measured at a maximum of 0.355 UI when measured at 5UI (for components running at 1.5Gb/s)

2.12.8. TSG-08 : DJ at Connector, Data, 5UI

2.12.8.1. Device Expected Behavior

See sections 7.2.2.3.11 and 7.3 of Serial ATA Revision 2.5.

Measurement Requirements
See section 7.4.8 of Serial ATA Revision 2.5.

This test is optional for all components. For components which support 3Gb/s, this requirement would be tested at 1.5Gb/s.

The loop damping factor for the reference PLLs is required to be 0.707.

There are several different patterns defined within the specification and are intended to be used to verify this requirement. In order to ensure efficient test time of products within the Interoperability Testing, testing of this requirement will be limited to the following patterns as defined in the SATA Revision 2.5 specification: High Frequency Test Pattern (HFTP), and Lone Bit Pattern (LBP). It is optional to additionally test using the Simultaneous Switching Outputs Pattern (SSOP) as a third pattern.

For this test, the methodology of obtaining the result must follow a filtered TIE based method, similar to that for obtaining results for TSG-11 and TSG-12. In the past, an N-cycle method was used but is no longer preferred for the use of the interoperability testing.

Pass/Fail Criteria
- DJ measured at a maximum of 0.175 UI when measured at 5UI (for components running at 1.5Gb/s)

2.12.9. TSG-09 : TJ at Connector, Data, 250UI

2.12.9.1. Device Expected Behavior

See sections 7.2.2.3.11 and 7.3 of Serial ATA Revision 2.5.

Measurement Requirements
See section 7.4.8 of Serial ATA Revision 2.5.

For components which support 3Gb/s, this requirement must be tested at 1.5Gb/s.

For this test, the methodology of obtaining the result must follow a filtered TIE based method, similar to that for obtaining results for TSG-11 and TSG-12. In the past, an N-cycle method was used but is no longer preferred for the use of the interoperability testing.

The loop damping factor for the reference PLLs is required to be 0.707.

There are several different patterns defined within the specification and are intended to be used to verify this requirement. In order to ensure efficient test time of products within the Interoperability Testing, testing of this requirement will be limited to the following patterns as defined in the SATA Revision 2.5 specification: High Frequency Test Pattern (HFTP), and Lone Bit Pattern (LBP). It is optional to additionally test using the Simultaneous Switching Outputs Pattern (SSOP) as a third pattern.

Pass/Fail Criteria

- TJ measured at a maximum of 0.47 UI when measured at 250UI (for components running at 1.5Gb/s)

2.12.10. TSG-10 : DJ at Connector, Data, 250UI

2.12.10.1. Device Expected Behavior

See sections 7.2.2.3.11 and 7.3 of Serial ATA Revision 2.5.

Measurement Requirements
See section 7.4.8 of Serial ATA Revision 2.5.

For components which support 3Gb/s, this requirement must be tested at 1.5Gb/s.

For this test, the methodology of obtaining the result must follow a filtered TIE based method, similar to that for obtaining results for TSG-11 and TSG-12. In the past, an N-cycle method was used but is no longer preferred for the use of the interoperability testing.

The loop damping factor for the reference PLLs is required to be 0.707.

There are several different patterns defined within the specification and are intended to be used to verify this requirement. In order to ensure efficient test time of products within the Interoperability Testing, testing of this requirement will be limited to the following patterns as defined in the SATA Revision 2.5 specification: High Frequency Test Pattern (HFTP), and Lone Bit Pattern (LBP). It is optional to additionally test using the Simultaneous Switching Outputs Pattern (SSOP) as a third pattern.

Pass/Fail Criteria

- DJ measured at a maximum of 0.22 UI when measured at 250UI (for components running at 1.5Gb/s)

2.12.11. TSG-11 : TJ at Connector, Clock, 500

2.12.11.1. Device Expected Behavior

See sections 7.2.2.3.12 and 7.3 of Serial ATA Revision 2.5.

Measurement Requirements
See sections 7.4.6 and 7.4.8 of Serial ATA Revision 2.5.

This test requirement is only applicable to components running at 3Gb/s.

The loop damping factor for the reference PLLs is required to be 0.707.

There are several different patterns defined within the specification and are intended to be used to verify this requirement. In order to ensure efficient test time of products within the Interoperability Testing, testing of this requirement will be limited to the following patterns as defined in the SATA Revision 2.5 specification: High Frequency Test Pattern (HFTP), and Lone Bit Pattern (LBP). It is optional to additionally test using the Simultaneous Switching Outputs Pattern (SSOP) as a third pattern.

Pass/Fail Criteria

- TJ measured at a maximum of 0.37 UI when measured at $f_{BAUD}/500$ (for components running at 3Gb/s)

2.12.12. TSG-12 : DJ at Connector, Clock, 500

2.12.12.1. Device Expected Behavior

See sections 7.2.2.3.12 and 7.3 of Serial ATA Revision 2.5.

Measurement Requirements
See sections 7.4.6 and 7.4.8 of Serial ATA Revision 2.5.

This test requirement is only applicable to components running at 3Gb/s.

The loop damping factor for the reference PLLs is required to be 0.707.

There are several different patterns defined within the specification and are intended to be used to verify this requirement. In order to ensure efficient test time of products within the Interoperability Testing, testing of this requirement will be limited to the following patterns as defined in the SATA Revision 2.5 specification: High Frequency Test Pattern (HFTP), and Lone Bit Pattern (LBP). It is optional to additionally test using the Simultaneous Switching Outputs Pattern (SSOP) as a third pattern.

Pass/Fail Criteria

- DJ measured at a maximum of 0.19 UI when measured at $f_{BAUD}/500$ (for components running at 3Gb/s)

2.13. Phy Receiver Requirements

During the testing execution for all RX test requirements, it is essential that the device under test be able to complete an initial OOB sequence through the device COMWAKE. This is to allow device calibration to occur prior to and/or during the initial power on and detect sequences.

2.13.1. RX-01 : Pair Differential Impedance

2.13.1.1. Device Expected Behavior

See section 7.2.2.4.1 of Serial ATA Revision 2.5.

Measurement Requirements
See section 7.4.22 of Serial ATA Revision 2.5.

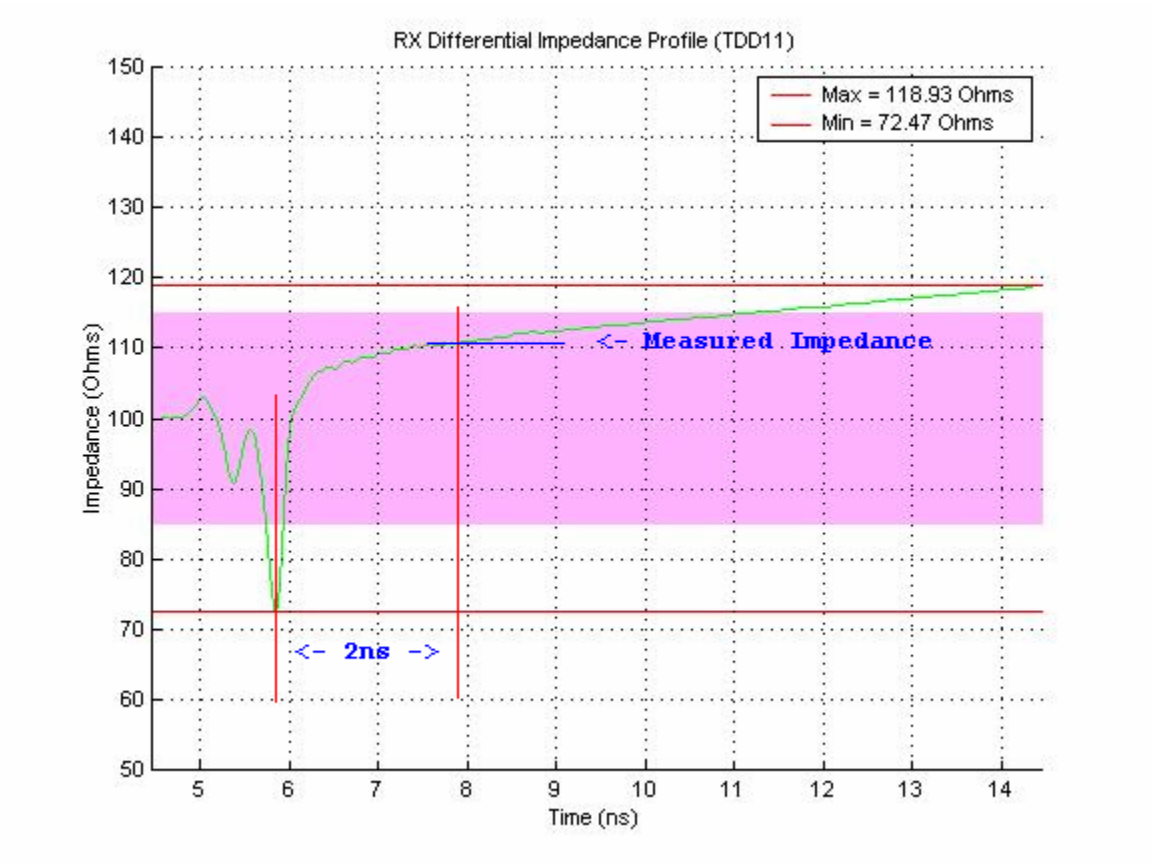

Figure 3 – Example impedance measurement point

While making the measurement, only consider the impedance at a point 2ns past the bottom of the last major capacitive excursion (i.e., dip) that is known to be inside the ASIC device. See Figure 3 above for an example.

For components which support 3Gb/s, this requirement must be tested at 1.5Gb/s.

Pass/Fail Criteria

- Pair differential impedance measured between 85 ohms and 115 ohms (for components running at 1.5Gb/s)

2.13.2. RX-02 : Single-Ended Impedance

2.13.2.1. Device Expected Behavior

See section 7.2.2.4.2 of Serial ATA Revision 2.5.

Measurement Requirements
See section 7.4.23 of Serial ATA Revision 2.5.

For components which support 3Gb/s, this requirement must be tested at 1.5Gb/s.

Pass/Fail Criteria

- $Z_{s\text{-}eRX}$ measured to be at least 40 ohms (for components running at 1.5Gb/s)

2.13.3. RX-03 : Differential Mode Return Loss

2.13.3.1. Device Expected Behavior

See section 7.2.2.4.3 of Serial ATA Revision 2.5.

Measurement Requirements
See section 7.4.10 of Serial ATA Revision 2.5.

Calibrate to the end of the SMA cables, but do NOT include (i.e. de-embedd) the SMA to SATA PCB and the SATA connector, so the board and the SATA connector are INCLUDED with the device measurement.

This test requirement is only applicable to components running at 3Gb/s.

Pass/Fail Criteria

- $RL_{DD11,RX}$ measured per the values in Table 6 (for components running at 3Gb/s)

Table 6 - RX Differential Mode Return Loss

Frequency	Minimum (dB)
150MHz-300MHz	18
300MHz-600MHz	14
600MHz-1.2GHz	10
1.2GHz-2.4GHz	8
2.4GHz-3.0GHz	3
3.0GHz-5.0GHz	1

2.13.4. RX-04 : Common Mode Return Loss

2.13.4.1. Device Expected Behavior

See section 7.2.2.4.4 of Serial ATA Revision 2.5.

Measurement Requirements
See section 7.4.10 of Serial ATA Revision 2.5.

Calibrate to the end of the SMA cables, but do NOT include (de-embedd) the SMA to SATA PCB and the SATA connector, so the board and the SATA connector are INCLUDED with the device measurement.

This test requirement is only applicable to components running at 3Gb/s.

Pass/Fail Criteria

- $RL_{CC11,RX}$ measured per the values in Table 7 (for components running at 3Gb/s)

Table 7 - RX Common Mode Return Loss

Frequency	Minimum (dB)
150MHz-300MHz	5

300MHz-600MHz	5
600MHz-1.2GHz	2
1.2GHz-2.4GHz	2
2.4GHz-3.0GHz	2
3.0GHz-5.0GHz	1

2.13.5. RX-05 : Impedance Balance

2.13.5.1. Device Expected Behavior

See section 7.2.2.4.5 of Serial ATA Revision 2.5.

Measurement Requirements
See section 7.4.10 of Serial ATA Revision 2.5.

This test requirement is only applicable to components running at 3Gb/s.

Pass/Fail Criteria

- $RL_{DC11,RX}$ measured per the values in Table 8 (for components running at 3Gb/s)

Table 8 - RX Impedance Balance

Frequency	Minimum (dB)
150MHz-300MHz	30
300MHz-600MHz	30
600MHz-1.2GHz	20
1.2GHz-2.4GHz	10
2.4GHz-3.0GHz	4
3.0GHz-5.0GHz	4

2.14. Phy OOB Requirements

2.14.1. OOB-01 : OOB Signal Detection Threshold

2.14.1.1. Device Expected Behavior

See section 7.2.2.7.1 of Serial ATA Revision 2.5.

Measurement Requirements
See section 7.4.20 of Serial ATA Revision 2.5.

For components which support 3Gb/s, this requirement must be tested at both interface rates (1.5Gb/s and 3Gb/s).

Note that the specification stipulates a Detection Threshold with value of V_{thresh}, where V_{thresh} is $50 \le V_{thresh} \le 200$ in millivolts (mV) for 1.5Gb/s devices, and where V_{thresh} is $75 \le V_{thresh} \le 200$ in millivolts (mV) for 3Gb/s devices. For the interests of the Interoperability Program, the measurements will only be taken to verify this requirement at the lower and upper limits.

To execute this test on a device which supports 1.5Gb/s, an OOB burst is issued to the device at the following voltage threshold limits:

- 40mV (at this limit, the device is expected to NOT detect the OOB signaling)
- 210mV (at this limit, the device is expected to detect the OOB signaling)

To execute this test on a device which supports 3Gb/s, an OOB burst is issued to the device at the following voltage threshold limits:

- 60mV (at this limit, the device is expected to NOT detect the OOB signaling)
  - NOTE : Tool resolution preference is even values, as opposed to 75mV
- 210mV (at this limit, the device is expected to detect the OOB signaling)

Pass/Fail Criteria

- For devices running at 1.5Gb/s:
  - Verification of no device OOB detection at 40mV
  - Verification of device OOB detection at 210mV
  - If any of the above cases fails, this is considered a failure by the device.
- For devices running at 3Gb/s:
  - Verification of no device OOB detection at 60mV
  - Verification of device OOB detection at 210mV
  - If any of the above cases fails, this is considered a failure by the device.

2.14.2. OOB-02 : UI During OOB Signaling

2.14.2.1. Device Expected Behavior

See section 7.2.2.7.2 of Serial ATA Revision 2.5.

Measurement Requirements
See section 7.4.11 of Serial ATA Revision 2.5.

This test is only run once at the maximum interface rate of the component (1.5Gb/s or 3Gb/s).

Pass/Fail Criteria

- Mean UI_{OOB} measured to be between 646.67 ps and 686.67 ps over entire OOB burst

2.14.3. OOB-03 : COMINIT/RESET and COMWAKE Transmit Burst Length

2.14.3.1. Device Expected Behavior

See section 7.2.2.7.3 of Serial ATA Revision 2.5.

Measurement Requirements
See section 7.4.21 of Serial ATA Revision 2.5.

This test is only run once at the maximum interface rate of the component (1.5Gb/s or 3Gb/s).

Note that the requirement within the specification is called out in UI. For the interests of the Interoperability Program, the measured value (T) will be compared against th minimum and maximum values of a multiple of UI_{OOB} in nanoseconds, where $103.5 \leq T \leq 109.9$. The values above are obtained from the following formulas:

- Min (160) = 646.67ps (Min UIoob) x 160 = 103.5ns
- Max (160) = 686.67ps (Max UIoob) x 160 = 109.9ns

Pass/Fail Criteria

- Burst Length measured to be between minimum and maximum values of UI_{OOB} multiplied by 160 (in nanoseconds)

2.14.4. OOB-04 : COMINIT/RESET Transmit Gap Length

2.14.4.1. Device Expected Behavior

See section 7.2.2.7.4 of Serial ATA Revision 2.5.

Measurement Requirements
See section 7.4.21 of Serial ATA Revision 2.5.

This test is only run once at the maximum interface rate of the component (1.5Gb/s or 3Gb/s).

Note that the requirement within the specification is called out in UI. For the interests of the Interoperability Program, the measured value (T) will be compared against the minimum and maximum values of a multiple of UI_{OOB} in nanoseconds, where 310.4 ≤ T ≤ 329.6. The values above are obtained from the following formulas:

- Min (480) = 646.67ps (Min UIoob) x 480 = 310.4ns
- Max (480) = 686.67ps (Max UIoob) x 480 = 329.6ns

Pass/Fail Criteria

- Gap Length measured to be between minimum and maximum values of UI_{OOB} multiplied by 480 (in nanoseconds)

2.14.5. OOB-05 : COMWAKE Transmit Gap Length

2.14.5.1. Device Expected Behavior

See section 7.2.2.7.5 of Serial ATA Revision 2.5.

Measurement Requirements
See section 7.4.21 of Serial ATA Revision 2.5.

This test is only run once at the maximum interface rate of the component (1.5Gb/s or 3Gb/s).

Note that the requirement within the specification is called out in UI. For the interests of the Interoperability Program, the measured value (T) will be compared against th minimum and maximum values of a multiple of UI_{OOB} in nanoseconds, where 103.5 ≤ T ≤ 109.9. The values above are obtained from the following formulas:

- Min (160) = 646.67ps (Min UIoob) x 160 = 103.5ns
- Max (160) = 686.67ps (Max UIoob) x 160 = 109.9ns

Pass/Fail Criteria

- Gap Length measured to be between minimum and maximum values of UI_{OOB} multiplied by 160 (in nanoseconds)

2.14.6. OOB-06 : COMWAKE Gap Detection Windows

2.14.6.1. Device Expected Behavior

See section 7.2.2.7.6 of Serial ATA Revision 2.5.

Measurement Requirements
See section 7.4.21 of Serial ATA Revision 2.5.

This test is only run once at the maximum interface rate of the component (1.5Gb/s or 3Gb/s).

Note that the specification stipulates a Detection Window with value of T, where T is 55 ≤ T < 175 in nanoseconds. For the interests of the Interoperability Program, the measurements will only be

taken to verify this requirement at the lower and upper limits. At the time of the approval of this documentation, an errata was under review which proposed changing the minimum limit above to 35 nanoseconds. The testing of this requirement takes the new value into account (i.e. no response at 30ns) and is still within the current specification range of no response.

To execute this test, a COMWAKE is issued to the device at the following limits:

- 103ns (at this limit, the device is expected to respond with COMWAKE)
- 110ns (at this limit, the device is expected to respond with COMWAKE)
- 30ns (at this limit, the device is expected to NOT respond with COMWAKE)
- 177ns (at this limit, the device is expected to NOT respond with COMWAKE)

NOTE : There is no timing requirement for how soon following a host COMWAKE which the device must respond with a device COMWAKE. For test efficiency purposes, a tester is only required to wait for verification of device COMWAKE up to 100ms following de-qualification of host COMWAKE.

Pass/Fail Criteria

- Verification of device COMWAKE response at 103ns
- Verification of device COMWAKE response at 110ns
- Verification of no device COMWAKE response at 30ns
- Verification of no device COMWAKE response at 177ns
- If any of the above cases fails, this is considered a failure by the device.

2.14.7. OOB-07 : COMINIT Gap Detection Windows

2.14.7.1. Device Expected Behavior

See section 7.2.2.7.7 of Serial ATA Revision 2.5.

Measurement Requirements

See section 7.4.21 of Serial ATA Revision 2.5.

This test is only run once at the maximum interface rate of the component (1.5Gb/s or 3Gb/s).

Note that the specification stipulates a Detection Window with value of T, where T is $175 \leq T < 525$ in nanoseconds. For the interests of the Interoperability Program, the measurements will only be taken to verify this requirement at the lower and upper limits.

To execute this test, a COMRESET is issued to the device at the following limits:

- 306ns (at this limit, the device is expected to respond with COMINIT)
- 334ns (at this limit, the device is expected to respond with COMINIT)
- 173ns (at this limit, the device is expected to NOT respond with COMINIT)
- 527ns (at this limit, the device is expected to NOT respond with COMINIT)

NOTE : A device must respond by transmitting COMINIT within 10ms of de-qualification of a received COMRESET signal (see section 8.3.2 of Serial ATA Revision 2.5). With this in mind, a test only needs to wait up to 11ms following de-qualification of COMRESET to ensure that the device is responding. If no COMINIT is received in this timeframe, this is considered a failure by the device to this test.

NOTE : In a case where a device supports Asynchronous Signal Recovery, it is possible that a device may transmit COMINIT pro-actively and not in direct response to a COMRESET. In verification of this test requirement, it is essential that the tester be able to extract any COMINIT response which may be as a result of Asynchronous Signal Recovery, and simply verify COMINIT responses as a result of COMRESET receipt from the host.

Pass/Fail Criteria

- Verification of device COMINIT response at 306ns
- Verification of device COMINIT response at 334ns
- Verification of no device COMINIT response at 173ns
- Verification of no device COMINIT response at 527ns
- If any of the above cases fails, this is considered a failure by the device.

3. System Interoperability Tests

The system interoperability tests are required tests above and beyond the tests described in the preceding sections of the document. This testing is required for the Device component type. No System Interoperability testing is required for Cable components.

3.1. System Description

The test systems used for the system interoperability testing must be configured in such a way to confidently provide test capabilities to ensure interoperability of a Serial ATA component within that platform. The components and configuration information for the test platforms are defined in the following sections.

3.1.1. System Component Selection

Determination of components for inclusion in the platforms used for the system interoperability testing will be completed by the SATA-IO. The SATA-IO will deliver the approved list of components which are sufficient for usage in the systems. This will be applicable to testing completed at both Interop Workshops and independent test labs.

For the current set of system interoperability testing, the following components will be defined for usage by the SATA-IO:

- Motherboard/chipset for SATA host usage
- SATA cables

A total of 5 different platform configurations (including appropriate components) will be defined for usage in the system interoperability testing. It is required that all 5 configurations are used in verification of all SATA components under test (i.e. cables, devices). The approved platform configurations are specified in section 3.1.2.

Only the components approved by the SATA-IO may be used in the platform configurations for system interoperability testing.

3.1.2. Platform Configurations

The following platform configurations will be used for all component testing with regards to system interoperability testing.

- Configuration 1 : Intel ICH7 based system:
  - Dell 9150 or HP DC7600 CMT – Internal graphics, no add-in cards
- Configuration 2 : Intel ICH6 base system
  - HP DC5100 or DX6120 micro Tower
- Configuration 3 : ATI SB400
  - HP DX5150 micro tower or SFF (same system board), internal graphics, no add-in cards
- Configuration 4 : Nvidia nForce4
  - HP xw9300 workstation
- Configuration 5 : Silicon Image 3132-based PCIe SATA
  - Host system with a PCIe slot and either a LyCOM PE-103R5 or Addonics AD2SA3GPX1 host controller

For device component testing, the cables used in the platform configurations must be selected from the Integrators List as already approved products and are limited to non-latching straight-straight solutions which are 1 meter in length.

The configurations are based on requirements around SATA specific capabilities and combinations (e.g. 3Gb/s, 1.5Gb/s, different host controllers, etc…). It is also required that the motherboards or hosts considered for this testing support INT 13h mechanisms.

The SATA-IO will consider updating the approved platform configurations approximately every 12-18 months, depending on necessity.

3.2. Test Description

There are several key components when working to understand the interoperability of a component in a specified system, including data transfer and error rates. The system interoperability tests are defined in a way such that the components are validated in a repeatable and consistent manner.

3.2.1. Test Details

It is required that the test(s) defined in this section are run on all 5 platform configurations outlined by this document.

The data used for the testing is pre-defined and developed from the specification defined COMP pattern. The data has been organized in such a way that different transfer sizes will be used to verify different data transfer behavior of the component. The data is organized in the following transfer sizes: 8KB, 64KB, 256KB, 1MB, and 16MB (all binary exact values [NOT decimal]). Errors will be tracked by the tool with verification of 128-bit CRC calculations on the data transferred through the component. This will be done using industry standard MD5 signatures based on the specified data and transfer sizes.

It is required that the test executes for 9 minutes in transferring of data on each platform configuration, with the appropriate CRC calculations for error tracking.

Note that for ATAPI device tests, only read transfers must be used for the system interoperability testing. For hard disk drives and cables, both read and write transfers must be used in the testing.

For implementation specific details, please see the System Interoperability MOI. The MS-DOS version is available at the time of the publication of this document.

3.2.2. Pass/Fail Criteria

To be considered passing on the system interoperability tests, a component must execute the test(s) successfully on at least 4 of the 5 platform configurations with no errors reported.