SyntheSys Research, Inc.

Serial ATA International Organization

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Serial ATA Interoperability Program Revision 1.1

SyntheSys Research, Inc. MOI, Method of Implementation, for PHY and TSG Electrical Tests

using the BERTScope

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MODIFICATION RECORD

First draft, January 25, 2006

Version 0.8, February 6, 2006

Version 0.93RC, March 14, 2006

Version 0.94RC, March 22, 2006: “using either the BIST T,S,A mode or other suitable method” inserted in the initiating step in PHY-01 through TSG-12. TSG01 section inserted. “Possible Issues” inserted in TSG-02. TSG04 removed one cable to improve the setup and corrected labels in step 4. TSG05 and TSG06 corrected to: “at least 10,000 samples” and “mean” Amplitude Imbalance. Inserted: “When initiating via BIST; there is 50% “in Possible Issues in TSG-09 through TSG-12. “This test requirement is only applicable to components claiming to be capable of running at 3Gb/s” inserted in TSG-11 and TSG-12. Appendix C step-by-step bullets filled in.

Version 0.96RC, March 23, 2006: Completed step 4 through 9 and observable results paragraphs of TSG01 and added “When calibrating the BERTScope clock need to be used. By clicking on “Synthesizer” the Clock frequency is set to either 1.5 Gbps or 3.0 Gbps. Clock and Data Outputs are enabled by clicking on the “Outputs On/Off” button. “to TSG-02.

Version 0.97RC, April 19, 2006: “SATAI (3.0)” corrected to “SATAI (6.0) in PHY-01 through TSG-02 and in TSG-09 and TSG-10. TSG-01 changed to minimum and maximum measured using the same method and TSG-02 merely using HFTP as described in Serial ATA Interoperability Program Unified Test Document, LogoTF_ILunified_v1_0RC2f.doc.

Version 0.98RC, June, 2006: Changed from “(6.0)” to “(1.98)” settings on the CR 12500A in PHY-01 through PHY-04. Updated TSG-01 and Appendix E. Updated PHY-01, PHY-04 and TSG-01 through TSG-03 with explicit requirements to save calibration screen shots. Updated TSG-09 and TSG-10 with TIE based methodology requirements of Unified Test Document, LogoTF_ILunified_v1_0RC2i.doc.

Version 0.99RC, June 7, 2006: Updated index to show TSG-01. Added reference to Comax H303000204 or equivalent in all sections. Detailed the scope measurements in PHY-03 and PHY-04.

Version 1.0RC, June 19, 2006: Modified SSC equations in PHY-04 to record SSC relative to $f_{nominal}$.

Version 1.05RC, September 14, 2006: Modified PHY-02 and PHY-04 to in clued the words “average over” ten SSC cycles for the measurement of frequency deviation. Added the Host Worst Case Port Identification test. Changed “device” to “product” and “DUT” to “PUT”. Inserted note of LBP pattern being per ECN 018 and therefore disparity agnostic. Removed disparity verification of the LBP pattern from TSG-01 and TSG-09 through TSG-12. Allowing multiple choices of Stimulus Tools in Appendix A for initiation of the product and generation of BIST Active.

Version 1.07RC, September 20, 2006: Added calibration procedure to TSG-04.

Revision 1.1 Version 0.90, October 30, 2006: Revised title, revision and version according to new workgroup naming conventions. Updated the TJ and DJ limits for Gen1 1.5 Gb/s to follow the limits for other clock to data jitter measurements, namely 0.37 and 0.19 UI respectively.

Revision 1.1 Version 0.91, November 6, 2006 and Revision 1.1 Version 1.0RC, November 16, 2006: Changed “Revision 0.90” to “Version 0.91” and moved “Revision 1.1” on cover page, Merged PHY-02, PHY-03 and PHY-04 to share one diagram and simplify the formula for conversion from measured value to ppm. Merge TSG-09 and TSG-10 as well as TSG-11 and TSG-12 in pairs to share procedure and images.

Revision 1.1 Version 1.0RC, July 26, 2007: Added Appendix G : Setup return loss verification and measurement data. “RC” removed after approval, November 13, 2008.

INTRODUCTION

These Methods of Implementations describe the step by step procedures to perform the required PHY-01 through PHY-04 and TSG-01 through TSG-12 (except TSG-07 and TSG-08, which are optional for all components) tests of the Serial ATA Interoperability Program using the BERTScope by SyntheSys Research, Inc. in order to qualify a product for listing on the SATA Integrators List.

The test setup is illustrated in Appendix B.

The Lone Bit Pattern (LBP) used for Interoperability Testing is that which is defined per ECN 018 against SATA Revision 2.5.

The tests may be performed in the sequence shown in Appendix D or automated using software shown in Test Title: Serial ATA Interop Test Suite. Please contact SyntheSys Research, Inc. at +1 (650) 364-1853 or info@bertscope.com for the availability of software and accessories.

REFERENCES

The following document is referenced in this text:

[1] Serial ATA version 2.5, SerialATA_Revision_2_5.pdf
[2] Serial ATA Interoperability Program Unified Test Document, Interop_UnifiedTest_Rev1_1_v092.doc
[3] Serial ATA Interoperability Program Policy Document, Interop_Policy_Rev1_1_v091.doc
[4] ECN 018 against Serial ATA version 2.5.

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Test Title: Host Worst Port Identification

Purpose: Prior to execution of any testing on a host, a "worst port" must be identified.

Resource Requirements:

- One BERTScope 7500 or BERTScope 12500 with software version 7.3 or later
- One clock recovery instrument BERTScope CR 12500A with software version SW 0.9.6 FPGA 2.8 or later
- One iSATA receptacle to SMA Female Adapter, Comax H303000202, H303000204 or equivalent
- One short SMA Male to SMA Male Cable less than or equal to 12" length, Sucoflex 104 or equivalent
- A pair of matched length short SMA Male to SMA Male Cables, Suhner Sucoflex 104 or equivalent
- A pair of matched length low loss SMA Male to SMA Male Cables of approximately 2 meters length, Suhner Sucoflex 106 or equivalent.

Last Modification: September 19, 2006

Discussion: The intent of identifying a worst port is not to validate each port to the specification, but to simply identify the worst port based on a single relative measurement across all ports within a host. The Interoperability Tests must then be executed on the worst port identified per the procedure below.

Test Setup as shown in Appendix B: Connect the CR 12500A sub-rate clock output to the BERTScope clock input using the short SMA Male to SMA Male Cable. Connect the Data Output + and - ports of the CR 12500A to the Data Input + and – ports of the BERTScope using the matched pair of cables. Connect both of the B+ and B- ports of iSATA receptacle, these are the pins marked 6 and 5 respectively, to SMA Adapter via the short matched pair of SMA Male to Male Cables to the respective CR 12500A Data Input + and - ports.

Test Procedure:

1. Power-on host and ensure test ports are enabled & functional. Run the following on each individual port.
2. Connect a 3.0 Gb/s device, i.e. HDD or ODD or device emulator, and complete OOB sequence
3. Connect the host to the iSATA receptacle
4. Execute TSG-09 while the host is in NRZ idle following OOB and record results for the Total Jitter (TJ) for each port

Observable Results:

- The "worse port" is identified as that which has the highest TJ value recorded on the measurement above

Test Title: Serial ATA Interop Test Suite Automation

Purpose: The Revision 1.1 Unified Listing tests for PHY and TSG have been automated to provide a repetitive and fast execution, namely less than 15 minutes for the Serial ATA Interop Test Suite.

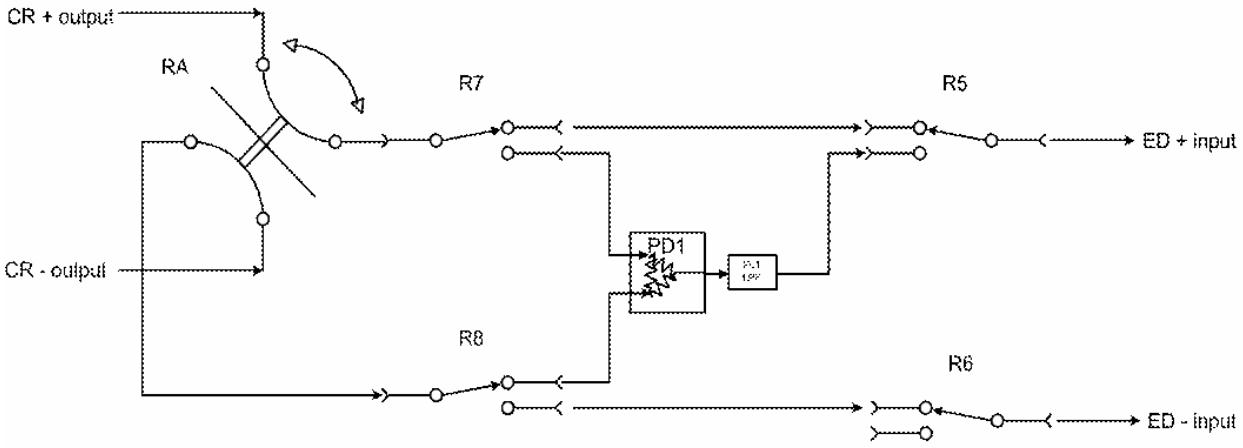
Resource Requirements:

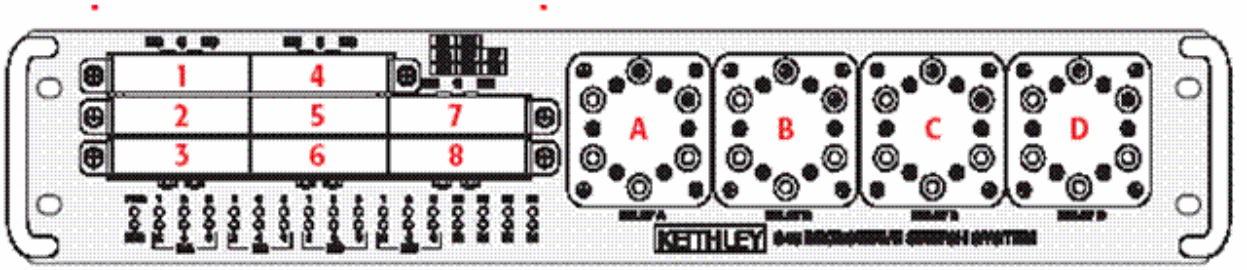
- One BERTScope 7500 or BERTScope 12500 with software version 7.3 or later
- One clock recovery instrument BERTScope CR 12500A with software version SW 0.9.6 FPGA 2.8 or later
- One iSATA receptacle to SMA Female Adapter, Comax H303000202, H303000204 or equivalent
- One short SMA Male to SMA Male Cable less than or equal to 12" length, Sucoflex 104 or equivalent
- A pair of matched length short SMA Male to SMA Male Cables, Suhner Sucoflex 104 or equivalent
- A pair of matched length low loss SMA Male to SMA Male Cables of approximately 2 meters length, Suhner Sucoflex 106 or equivalent.
- One 50 ohms termination, SUHNER 65SMA-50-0-1 or equivalent
- One passive power combiner, Weinschel 1515 or equivalent
- One first order low pass filter having a cutoff equal to the bitrate/2, namely 1.5 GHz.
- Switch, Keithley S46TX0000000TTTA
- Ethernet to GPIB interface for Keithley switch
- 7 Cables 6" each for switch: 32081-2-29094C-6
- BERTScope Serial ATA Test Fixture for support of non-disconnect PUTs.
- BERTScope Serial ATA Interop Test Suite software, revision 0.7.1

Last Modification: October 30, 2006

Discussion: Automation speeds up the measurements and assures repeatability by elimination human interactions. The tests are executed by use of the PC controller as they are individually described in the following Test Titles. All tests may therefore be executed manually in absence of a suitable controller. Although BIST "L" loop back is the preferred mode for the automated Test Suite, the Test Suite does allow for BIST "T,A,S" mode testing as well, The BERTScope Serial ATA Test Fixture additionally allows for testing of PUTs that do not support disconnect.

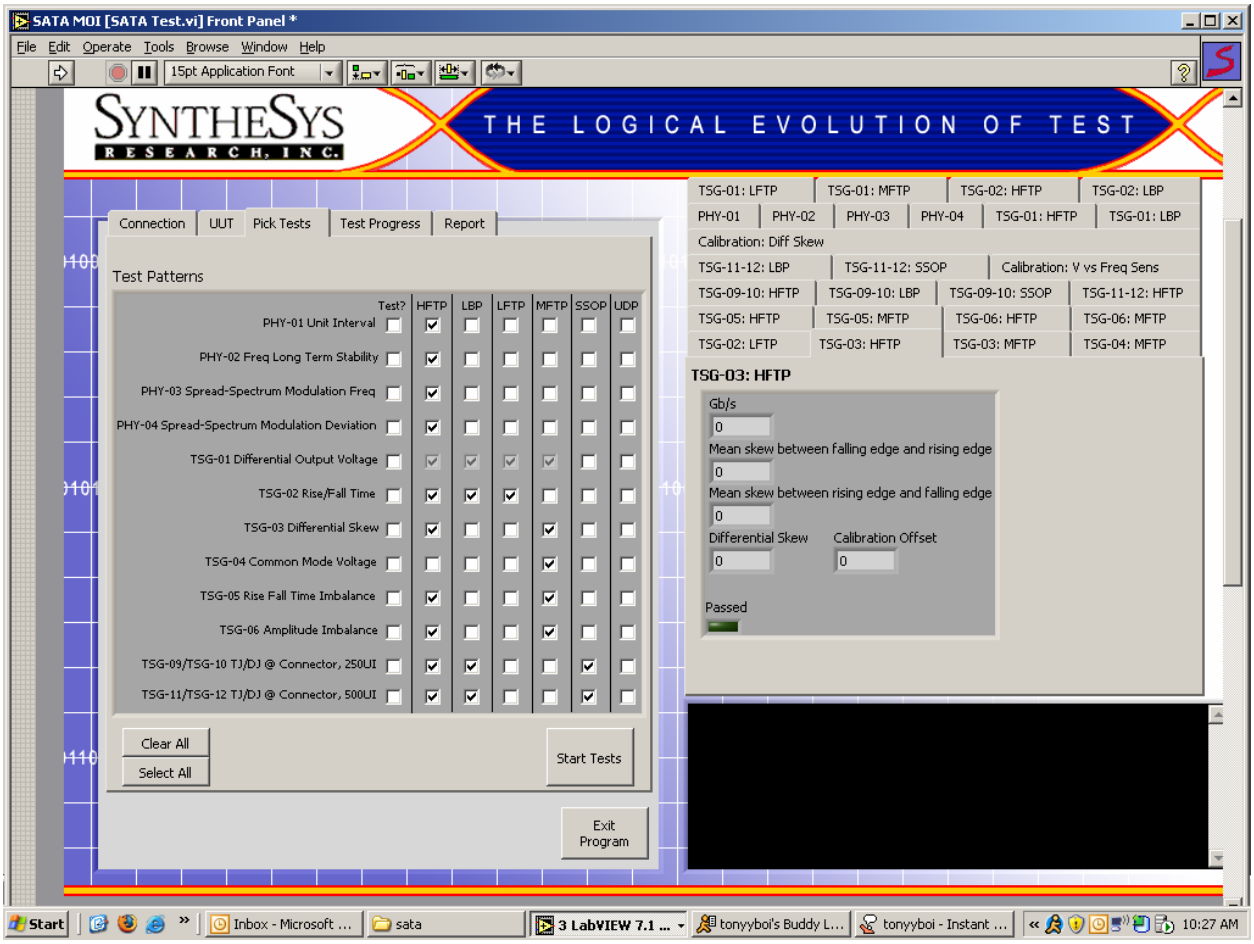
Test Setup as shown in Appendix B: Connect the CR 12500A sub-rate clock output to the BERTScope clock input using the short SMA Male to SMA Male Cable. Connect the Data Output + and - ports of the CR 12500A to the Data Input + and – ports of the BERTScope using the matched pair of cables. Connect both of the B+ and B- ports of iSATA receptacle, these are the pins marked 6 and 5 respectively, to SMA Adapter via the short matched pair of SMA Male to Male Cables to the respective CR 12500A Data Input + and - ports. Connect the USB cable between the CR12500A and the BERTScope and connect the controller PC to the BERTScope via the Ethernet connection. The Keithley switch is further connected to the controller PC via the Ethernet to GBIP converter and between the CR 12500A and the BERTScope as per the following Figure.





Test Procedure:

1. Connect controller to the set-up and follow the Serial ATA Interop Test Suite on-screen instructions.



Observable Results:

- The observable results are recorded in an Interop spread sheet compatible format and compared against Interop test limits for pass/fail indication.

Test Title: PHY-01 : Unit Interval

Purpose: Verify that the Product Under Test, PUT, meets the Unit Interval specification of section 7.2.2.1.3 of Serial ATA revision 2.5 at both 1.5 Gb/s and 3 Gb/s if the PUT claims to support both rates.

Resource Requirements:

- One BERTScope 7500 or BERTScope 12500 with software version 7.3 or later
- One clock recovery instrument BERTScope CR 12500A with software version SW 0.9.6 FPGA 2.8 or later
- One iSATA receptacle to SMA Female Adapter, Comax H303000202, H303000204 or equivalent
- One short SMA Male to SMA Male Cable less than or equal to 12" length, Sucoflex 104 or equivalent
- A pair of matched length short SMA Male to SMA Male Cables, Suhner Sucoflex 104 or equivalent
- A pair of matched length low loss SMA Male to SMA Male Cables of approximately 2 meters length, Suhner Sucoflex 106 or equivalent.

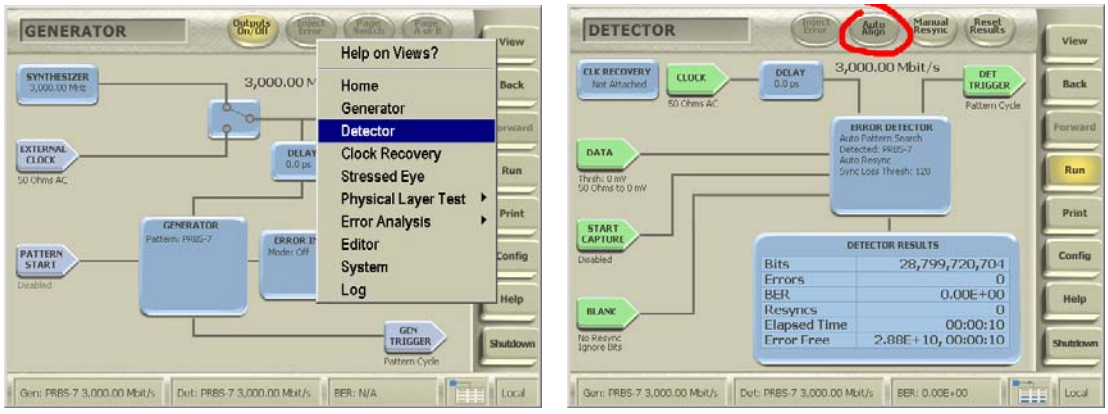
Last Modification: September 14, 2006

Discussion: For components which claim to support 3Gb/s, this requirement must be tested at both interface rates (1.5Gb/s and 3Gb/s). The BERTScope automatically perform the Unit Interval measurement according to section 7.2.2.1.3 of the Serial ATA revision 2.5 based on more than 100,000 UIs.

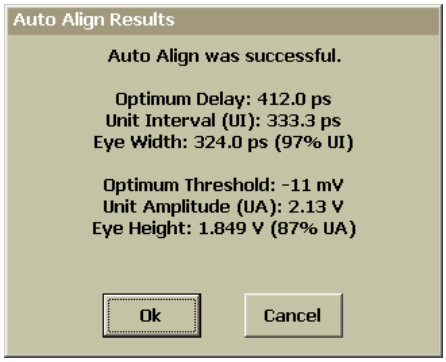
Test Setup as shown in Appendix B: Connect the CR 12500A sub-rate clock output to the BERTScope clock input using the short SMA Male to SMA Male Cable. Connect the Data Output + and - ports of the CR 12500A to the Data Input + and – ports of the BERTScope using the matched pair of cables. Connect both of the B+ and B- ports of iSATA receptacle, these are the pins marked 6 and 5 respectively, to SMA Adapter via the short matched pair of SMA Male to Male Cables to the respective CR 12500A Data Input + and - ports.

Test Procedure:

2. Initiate the PUT transmitting the HFTP pattern (D10.2) using either the BIST T,S,A mode or other suitable method as described in Appendix A.
3. Connect the PUT to the iSATA receptacle
4. On CR 12500A, choose the appropriate pre-stored selection: "SATA1 (1.98)" for 1.5 Gb/s or "SATA2 (1.98)" for 3 Gb/s; by pressing "Enter", scroll to the desired setting and press "Enter" again. On the CR 12500A also set the sub-rate clock divider to 1 by scrolling to "SubDiv: 4" press "Enter" select "1" and press "Enter" again.
5. On the BERTScope, Select "View" then "Detector" and click on "Auto Align".



A pop-up window will appear with the Unit Interval measurement result.



6. Record the measured Unit Interval.
7. If the PUT claim to be capable of running at 3 Gb/s then repeat 1 through 5 of above to get both 1.5 Gb/s and 3 Gb/s measurements.

Observable Results: The pass/fail criteria are:

- Mean Unit Interval measured shall be between 666.4333ps (min) and 670.2333ps (max) (for components when running at 1.5Gb/s)
- Mean Unit Interval measured shall be between 333.2167ps (min) and 335.1167ps (max) (for components claiming to be capable of running at 3Gb/s)

Time Base Stability: <1 ppm per year plus +/-2.5 ppm temperature stability -30 ^{o}C to +70 ^{o}C

Test Title: PHY-02 : Frequency Long Term Stability
Test Title: PHY-03 : Spread-Spectrum Modulation Frequency
Test Title: PHY-04 : Spread-Spectrum Modulation Deviation

Purpose: Verify that the Product Under Test, PUT, meets the Frequency Long Term Stability specification of section 7.2.2.1.4; the Spread-Spectrum Modulation Frequency specification of section 7.2.2.1.5; and the Spread-Spectrum Modulation Deviation specification of section 7.2.2.1.6 and 7.3.3 of Serial ATA revision 2.5.

Resource Requirements:

- One BERTScope 7500 or BERTScope 12500 with software version 9.51 or later
- One clock recovery instrument BERTScope CR 12500A with software version SW 0.9.6 FPGA 2.8or later
- One iSATA receptacle to SMA Female Adapter, Comax H303000202, H303000204 or equivalent
- One short SMA Male to SMA Male Cable less than or equal to 12" length, Sucoflex 104 or equivalent
- A pair of matched length short SMA Male to SMA Male Cables, Suhner Sucoflex 104 or equivalent
- A pair of matched length low loss SMA Male to SMA Male Cables of approximately 2 meters length, Suhner Sucoflex 106 or equivalent.

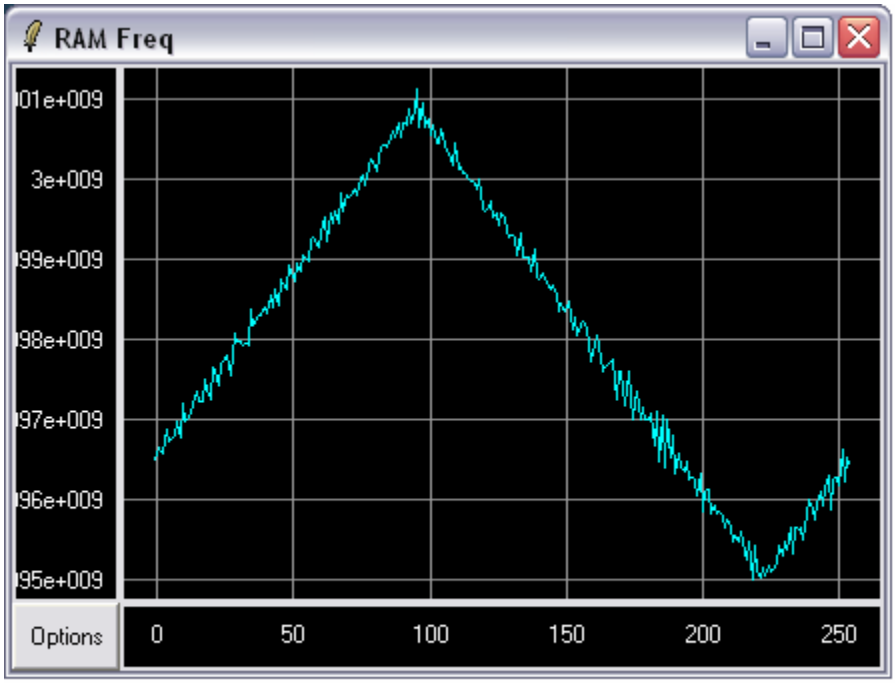
Last Modification: November 6, 2006

Discussion: These tests are only run once at the maximum interface rate claimed by the component (1.5Gb/s or 3Gb/s). PHY-03 and PHY-04 are only run on a PUT claiming SSC. The BERTScope CR12500A has a built-in frequency counter that automatically performs the frequency measurement according to section 7.4.6 of the Serial ATA revision 2.5. The BERTScope CR 12500A further automatically demodulates the incoming data signal and displays the spread-spectrum modulation waveform and measures the Spread-Spectrum Repetition and Modulation Frequency over at least 10 cycles using the internal precision frequency counter according to section 7.4.11 of the Serial ATA revision 2.5. If support of SSC is claimed by the product, the reported PHY-02 result must be the average maximum value from the range of SSC modulation deviation, which is obtained by using the following formula: $f_{tol} = (RawMax - f_{nominal})/f_{nominal}$. RawMax and RawMin are respectively the maximum and minimum frequencies in the SSC waveform averaged over the number, N, of cycles displayed as "Using N Cycles". $f_{nominal}$ is 1.5 GHz for PUTs running at 1.5 Gb/s and 3 GHz for PUTs claiming to be capable of running at 3 Gb/s.

Test Setup as shown in Appendix B: Connect the CR 12500A sub-rate clock output to the BERTScope clock input using the short SMA Male to SMA Male Cable. Connect the Data Output + and - ports of the CR12500A to the Data Input + and – ports of the BERTScope using the matched pair of cables. Connect both of the B+ and B- ports of iSATA receptacle, these are the pins marked 6 and 5 respectively, to SMA Adapter via the short matched pair of SMA Male to Male Cables to the respective CR 12500A Data Input + and - ports.

Test Procedure:

1. Initiate the PUT transmitting the HFTP pattern (D10.2) at the highest of the 1.5 Gb/s or 3 Gb/s that the PUT claims to capable of using either the BIST T,S,A mode or other suitable method as described in Appendix A.
2. Connect the PUT to the iSATA receptacle
3. On CR 12500A, choose the appropriate pre-stored selection: "SATA1 (1.98)" for 1.5 Gb/s or "SATA2 (1.98)" for 3 Gb/s; by pressing Enter, scroll to the desired setting and press "Enter" again. On the CR 12500A also set the sub-rate clock divider to 1 by scrolling to "SubDiv: 4" press "Enter" select "1" and press "Enter" again.
4. Record the measured frequency from the CR 12500A display.
5. From the SSC Analysis display record the measured average repetition frequency, "MFreq", average maximum, "RawMax", and average minimum, "RawMin" frequencies of the spread-spectrum-modulation.



MFreq = 29.9746 KHz (Using 311 Cycles)

RawMax = 3.001096 GHz
RawMin = 2.994971 GHz

6. "MFreq" is the Spread-Spectrum Modulation Frequency for PHY-03.
7. Convert the measured CR 12500A frequency counter, RawMax and RawMin measurements to ppm using the following formula: $ppm_{counter} = (f_{counter} - f_{nominal})/f_{nominal}$,; $ppm_{max} = (RawMax - f_{nominal})/f_{nominal}$: $ppm_{min} = (RawMin - f_{nominal})/f_{nominal}$ $f_{nominal}$ is 1.5 GHz for PUTs running at 1.5 Gb/s and 3 GHz for PUTs claiming to be capable of running at 3 Gb/s. Record $ppm_{counter}$ as the measured Frequency Long Term Stability for PHY-02 if the PUT is not claimed to be SSC capable. Record ppm_{max} as the measured Frequency Long Term Stability for PHY-02 and ppm_{min} as the measured Spread Spectrum Modulation Deviation for PHY-04 if the PUT is claimed to be SSC capable.

Observable Results: The pass/fail criteria are:

- PHY-02: The measured Frequency Long Term Stability, $ppm_{counter}$ (or ppm_{max} for PUT claiming to be SSC capable) shall be between -350 ppm and 350 ppm.
- PHY-03:The measured Spread-Spectrum Modulation Frequency, MFreq, shall be between 30 kHz and 33 kHz.
- PHY-04: The measured Spread-Spectrum Modulation Deviation, ppm_{min}, shall be between -5000 ppm and +350 ppm.

Time Base Stability: <1 ppm per year plus +/-2.5 ppm temperature stability -30 ^{o}C to +70 ^{o}C.
Display Resolution: 1 kHz (equivalent to 0.33 ppm at 3 Gb/s and 0.66 ppm at 1.5 Gb/s) for PHY-02 and PHY-04. 0.1 Hz for PHY-03.
Averaging: 311 cycles of SSC as per above example provides 189 ppm of resolution for the PHY-02 and PHY-04 SSC average maximum and average minimum frequency measurements. The resolution improves proportional to the square root of the number of 311 cycle measurements that are averaged. For example averaging 100 measurements of 311 cycles each will yield 18.9 ppm resolution.

Test Title: TSG-01 : Differential Output Voltage

Purpose: Verify that the Product Under Test, PUT, meets the Differential Output Voltage specification of section 7.2.2.3.3 of Serial ATA revision 2.5 while transmitting various specified patterns, namely HFTP, LFTP and LBP at both 1.5 Gb/s and 3 Gb/s if the PUT claims to support both rates.

Resource Requirements:

- One BERTScope 7500 or BERTScope 12500 with software version 7.3 or later
- One clock recovery instrument BERTScope CR 12500A with software version SW 0.9.6 FPGA 2.8or later
- One iSATA receptacle to SMA Female Adapter, Comax H303000202, H303000204 or equivalent
- One short SMA Male to SMA Male Cable less than or equal to 12" length, Sucoflex 104 or equivalent
- A pair of matched length short SMA Male to SMA Male Cables, Suhner Sucoflex 104 or equivalent
- A pair of matched length low loss SMA Male to SMA Male Cables of approximately 2 meters length, Suhner Sucoflex 106 or equivalent.

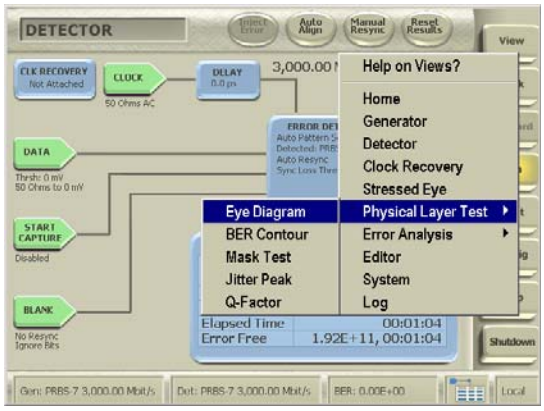
Last Modification: September 14, 2006

Discussion: For components which claim to support 3Gb/s, this requirement must be tested at both interface rates (1.5Gb/s and 3Gb/s). The BERTScope simultaneously captures the amplitudes for various bits in described set-up according to section 7.4.2 of the Serial ATA revision 2.5.

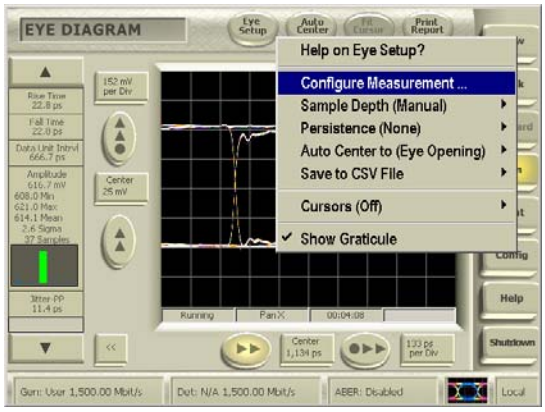
Test Setup as shown in Appendix B: Connect the CR 12500A sub-rate clock output to the BERTScope clock input using the short SMA Male to SMA Male Cable. Connect the Data Output + and - ports of the CR 12500A to the Data Input + and – ports of the BERTScope using the matched pair of cables. Connect both of the B+ and B- ports of iSATA receptacle, these are the pins marked 6 and 5 respectively, to SMA Adapter via the short matched pair of SMA Male to Male Cables to the respective CR 12500A Data Input + and - ports.

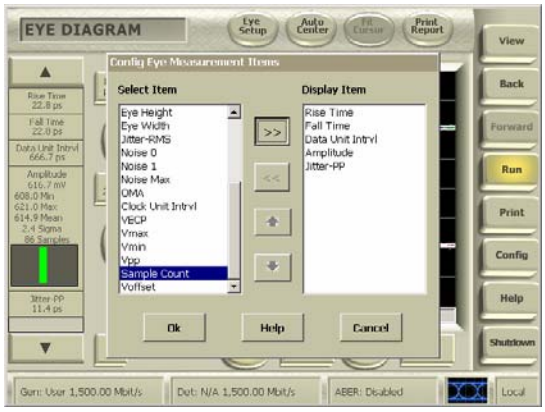
Test Procedure:

1. On CR 12500A, choose the appropriate pre-stored selection: "SATA1 (6.0)" for 1.5 Gb/s or "SATA2 (6.0)" for 3 Gb/s; by pressing "Enter", scroll to the desired setting and press "Enter" again. On the CR 12500A also set the sub-rate clock divider to 1 by scrolling to "SubDiv: 4" press "Enter" select "1" and press "Enter" again.
2. Initiate the PUT transmitting the HFTP pattern using either the BIST T,S,A mode or other suitable method as described in Appendix A.
3. Connect the PUT to the iSATA receptacle
4. On the BERTScope, select "View" then "Physical Layer Test" and "Eye Diagram" and click on "Auto Center".

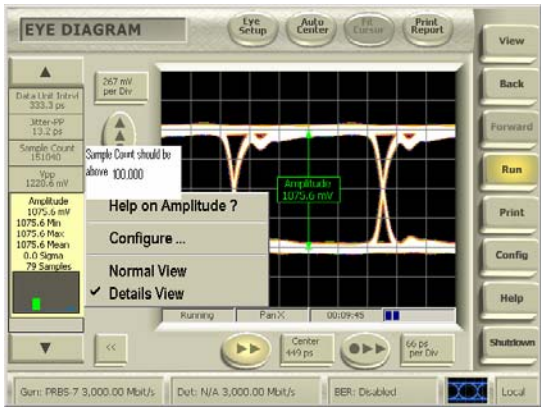


Click "Yes" to perform delay line calibrations if prompted by a pop-up window. Check that the sample size is set for 10,000 or higher by clicking on "Eye Setup" then "Configure Measurement…" select "Sample Count" and click on ">>" and "OK".





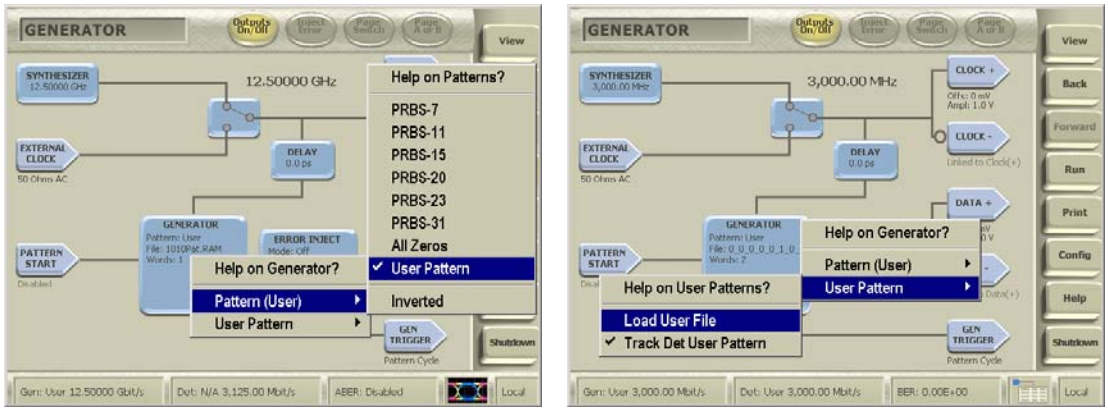
5. Click on the "Amplitude" measurement field on the left side bar and select "Detailed View".

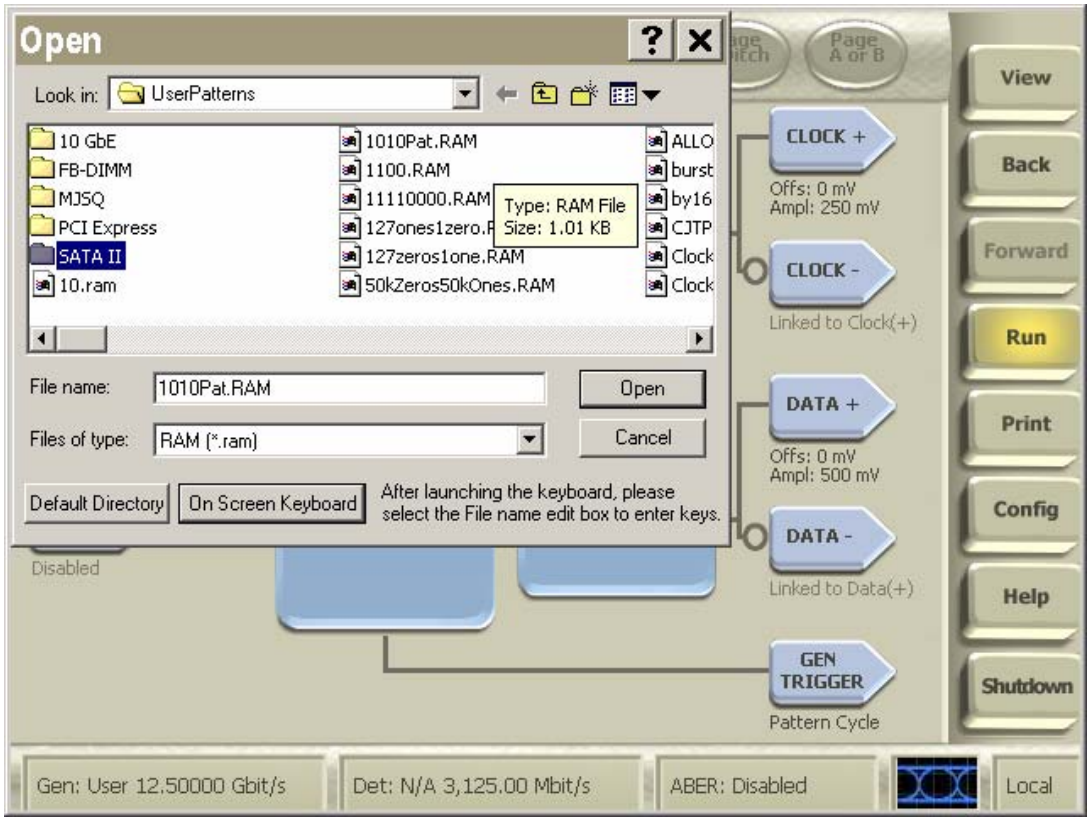


Wait until the sample counter has reach 10,000 then record the mean amplitude x, the standard deviation, s, the sample counter value, n, verify that 1537 $(s/x)^2 \leq n$ and compute the value DH = [x – (1.96 s /√ n)].

6. On the CR12500A scroll down to "SubDiv: 1", press "Enter" and scroll to select "2" and click "Enter
7. Repeat 2 through 4 with the PUT initiated transmitting the MFTP pattern and using the cursor to measure the amplitude at the second "1" and "0" which is 0.5 UI from the center of the MFTP "1100" eye. Wait until the sample counter has reach 10,000 then record the mean amplitude x, the standard deviation, s, the sample counter value, n, verify that 1537 $(s/x)^2 \leq n$ and compute the value DM = [x – (1.96 s /√ n)].
8. On the CR12500A scroll down to "SubDiv; 2", press "Enter" and scroll to select "10" and click "Enter".
9. Repeat 2 through 4 with the PUT initiated transmitting the LBP pattern this time measuring the amplitude of the lone bit. Measure the amplitude on the lone "1" bit in the "00001000" sequence. Wait until the sample counter has reach 10,000 then record the mean amplitude x, the standard deviation, s, the sample counter value, n, verify that 1537 $(s/x)^2 \leq n$ and compute the value VTestLBP = [x – (1.96 s /√ n)].
10. Record the smallest value of DM and VTestLBP as the minimum differential voltage, VdiffTX(Min) and the largest value of DM and VTestLBP as the maximum voltage, VdiffTX(Max).
11. If the PUT claims to be capable of running at 3 Gb/s then repeat 1 through 10 of above to get both 1.5 Gb/s and 3 Gb/s measurements.
12. Calibrate the test set up by repeating 1 through 11 above using the same patterns, but generated by the pattern generator of the BERTScope connected via the short matched pair of cables first in place of the iSATA receptacle to SMA Female Adapter and the PUT and then compare these measured values to a set measured with the BERTScope Data Output ports directly to the Data Input ports of the BERTScope. All calibration screen shots need to be saved. This is done by clicking on "Print" and select "Print to file" then create a unique file name for each calibration data including the serial number

of the equipment. The ratio of amplitude measured through the CR 12500A and cables compared to the amplitude measured directly is the amplitude calibration factor,, which accounts for the cable and CR 12500A insertion loss. The patterns are pre-loaded on the BERTScope in "View", then "Generator", click on "Pattern", "User Pattern", "Load User File" then "SATA II" to select a pattern.





When calibrating; the BERTScope clock need to be used. By clicking on "Synthesizer" the Clock frequency is set to either 1.5 Gbps or 3.0 Gbps. Clock and Data Outputs are enabled by clicking on the "Outputs On/Off" button. The calibrated measurement values are the amplitudes measured from the PUT divided by the amplitude calibration factors.

Observable Results: The pass/fail criteria are:

- The measured minimum differential voltages, VdiffTX(Min), shall both be larger than 400 mV (at 1.5 Gb/s as well as at 3.0 Gb/s for components claiming to be capable of running at 3Gb/s)
- Each of the measured maximum differential voltages, VdiffTX(Max), shall be less than 800 mV (at 1.5 Gb/s as well as at 3.0 Gb/s for components claiming to be capable of running at 3Gb/s)

Test Title: TSG-02 : Rise/Fall Time

Purpose: Verify that the Product Under Test, PUT, meets the Rise and Fall Time specification of section 7.2.2.3.3 of Serial ATA revision 2.5 while transmitting various specified patterns, namely HFTP (D10.2) at both 1.5 Gb/s and 3 Gb/s if the PUT claims to support both rates.

Resource Requirements:

- One BERTScope 7500 or BERTScope 12500 with software version 7.3 or later
- One clock recovery instrument BERTScope CR 12500A with software version SW 0.9.6 FPGA 2.8or later
- One iSATA receptacle to SMA Female Adapter, Comax H303000202, H303000204 or equivalent
- One short SMA Male to SMA Male Cable less than or equal to 12" length, Sucoflex 104 or equivalent
- A pair of matched length short SMA Male to SMA Male Cables, Suhner Sucoflex 104 or equivalent
- A pair of matched length low loss SMA Male to SMA Male Cables of approximately 2 meters length, Suhner Sucoflex 106 or equivalent.

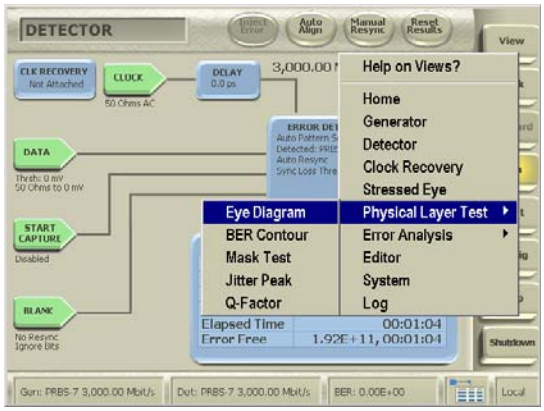
Last Modification: September 14, 2006

Discussion: For components which claim to support 3Gb/s, this requirement must be tested at both interface rates (1.5Gb/s and 3Gb/s). The BERTScope simultaneously measures the 20% to 80% Rise and 80% to 20% Fall times by default according to section 7.4.3 of the Serial ATA revision 2.5.

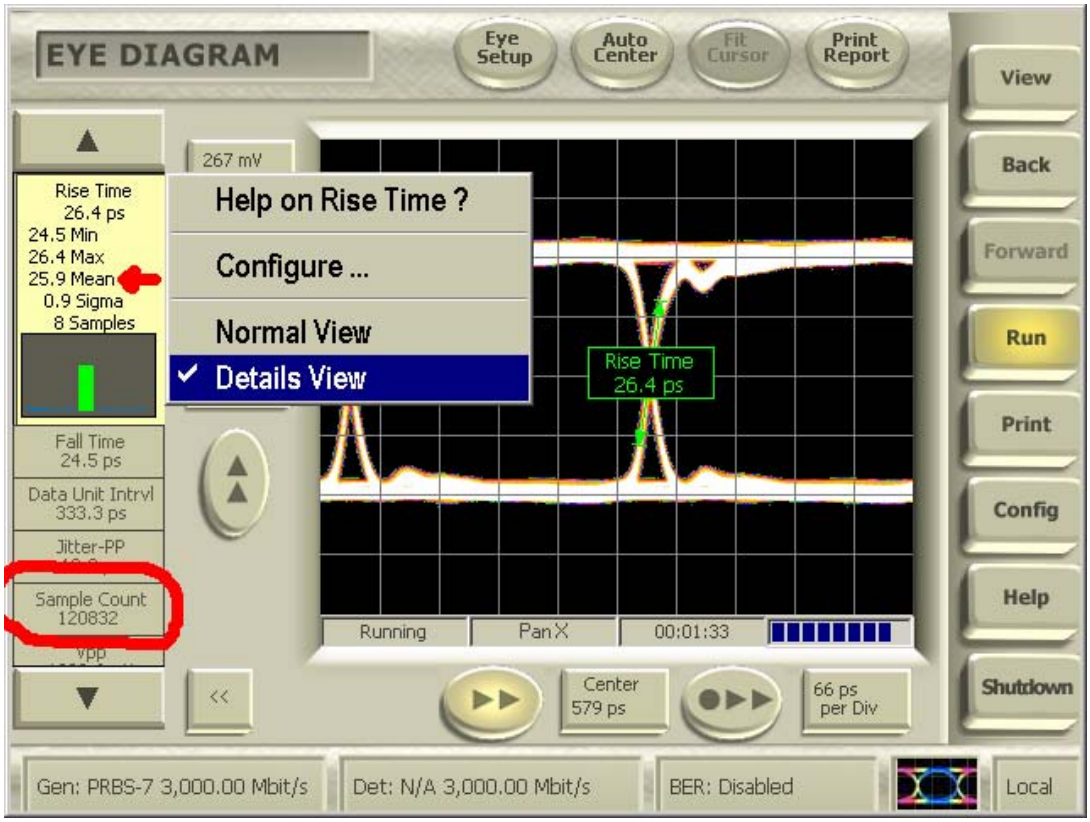
Test Setup as shown in Appendix B: Connect the CR 12500A sub-rate clock output to the BERTScope clock input using the short SMA Male to SMA Male Cable. Connect the Data Output + and - ports of the CR 12500A to the Data Input + and – ports of the BERTScope using the matched pair of cables. Connect both of the B+ and B- ports of iSATA receptacle, these are the pins marked 6 and 5 respectively, to SMA Adapter via the short matched pair of SMA Male to Male Cables to the respective CR 12500A Data Input + and - ports.

Test Procedure:

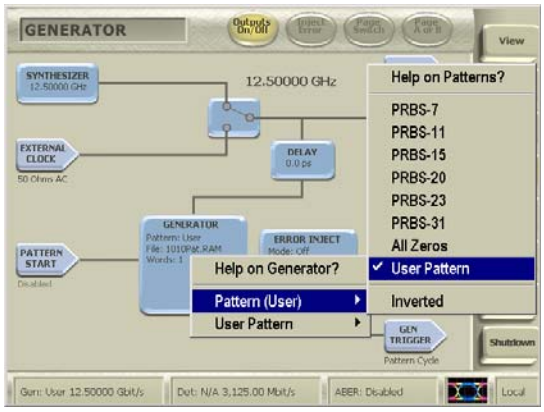
1. On CR 12500A, choose the appropriate pre-stored selection: "SATA1 (6.0)" for 1.5 Gb/s or "SATA2 (6.0)" for 3 Gb/s; by pressing "Enter", scroll to the desired setting and press "Enter" again. On the CR 12500A also set the sub-rate clock divider to 1 by scrolling to "SubDiv: 4" press "Enter" select "1" and press "Enter" again.
2. Initiate the PUT transmitting the HFTP pattern (D10.2) using either the BIST T,S,A mode or other suitable method as described in Appendix A.
3. Connect the PUT to the iSATA receptacle
4. On the BERTScope, select "View" then "Physical Layer Test" and "Eye Diagram" and click on "Auto Center".

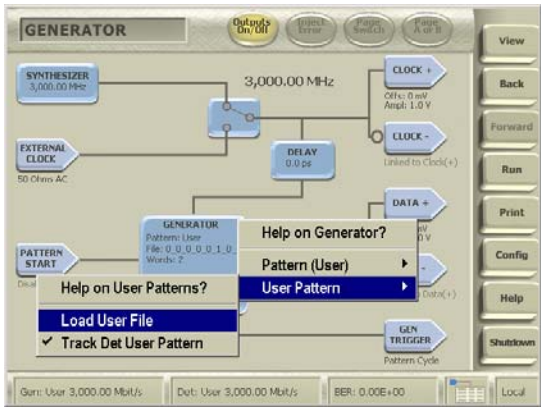


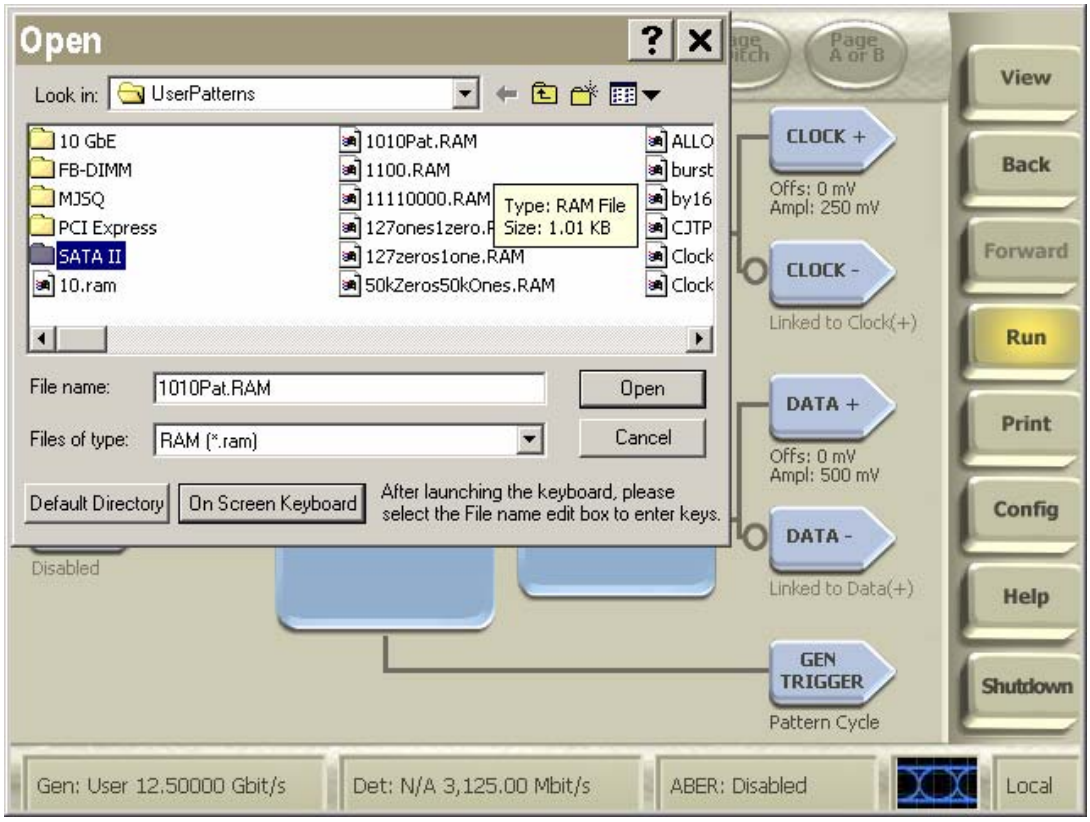
Click "Yes" to perform delay line calibrations if prompted by a pop-up window. Click on the "Rise Time" measurement field on the left side bar and select "Detailed View". Wait until the sample counter has reach 100,000 and record the mean Rise Time value.



5. Click on the "Fall Time" measurement field on the left side bar on the BERTScope and select "Detailed View". Record the mean Fall Time value (no need to wait since the fall time measurements were done simultaneously with the rise time measurements).
6. If the PUT claims to be capable of running at 3 Gb/s then repeat 1 through 5 of above to get both 1.5 Gb/s and 3 Gb/s measurements.
7. Calibrate the test set up by repeating 1 through 6 above using the same patterns, but generated by the pattern generator of the BERTScope connected via the short matched pair of cables in place of the iSATA receptacle to SMA Female Adapter and the PUT. All calibration screen shots need to be saved. This is done by clicking on "Print" and select "Print to file" then create a unique file name for each calibration data including the serial number of the equipment. The patterns are pre-loaded on the BERTScope in "View", then "Generator", click on the blue "Generator" box, "User Pattern", "Load User File" then "SATA II" to select a pattern.







When calibrating the BERTScope clock need to be used. By clicking on "Synthesizer" the Clock frequency is set to either 1.5 Gbps or 3.0 Gbps. Clock and Data Outputs are enabled by clicking on the "Outputs On/Off" button. The calibrated measurement values are the square root of the difference between the square of recorded time and the square of the calibration time measurements; t_{rise} = square root of ($t_{rise\_measured}^2 - t_{rise\_cal}^2$) and t_{fall} = square root of ($t_{fall\_measured}^2 - t_{fall\_cal}^2$).

Observable Results: The pass/fail criteria are:

- Each of the three measured Rise Time and three measured Fall Time values shall be less than 273 ps (0.41 UI) (for components when running at 1.5Gb/s)
- Each of the three measured Rise Time and three measured Fall Time values shall be less than 136 ps (0.41 UI) (for components claiming to be capable of running at 3Gb/s)

Resolution: Two measurements of +/-0.1 ps each.

Test Title: TSG-03 : Differential Skew

Purpose: Verify that the Product Under Test, PUT, meets the Differential Skew specification of section 7.2.2.3.4 of Serial ATA revision 2.5 while transmitting various specified patterns, namely HFTP (D10.2) and MFTP.

Resource Requirements:

- One BERTScope 7500 or BERTScope 12500 with software version 8.21 or later
- One clock recovery instrument BERTScope CR 12500A with software version SW 0.9.6 FPGA 2.8or later
- One iSATA receptacle to SMA Female Adapter, Comax H303000202, H303000204 or equivalent
- One short SMA Male to SMA Male Cable less than or equal to 12" length, Sucoflex 104 or equivalent
- A pair of matched length short SMA Male to SMA Male Cables, Suhner Sucoflex 104 or equivalent
- A pair of matched length low loss SMA Male to SMA Male Cables of approximately 2 meters length, Suhner Sucoflex 106 or equivalent
- One 50 ohms termination, SUHNER 65SMA-50-0-1 or equivalent.

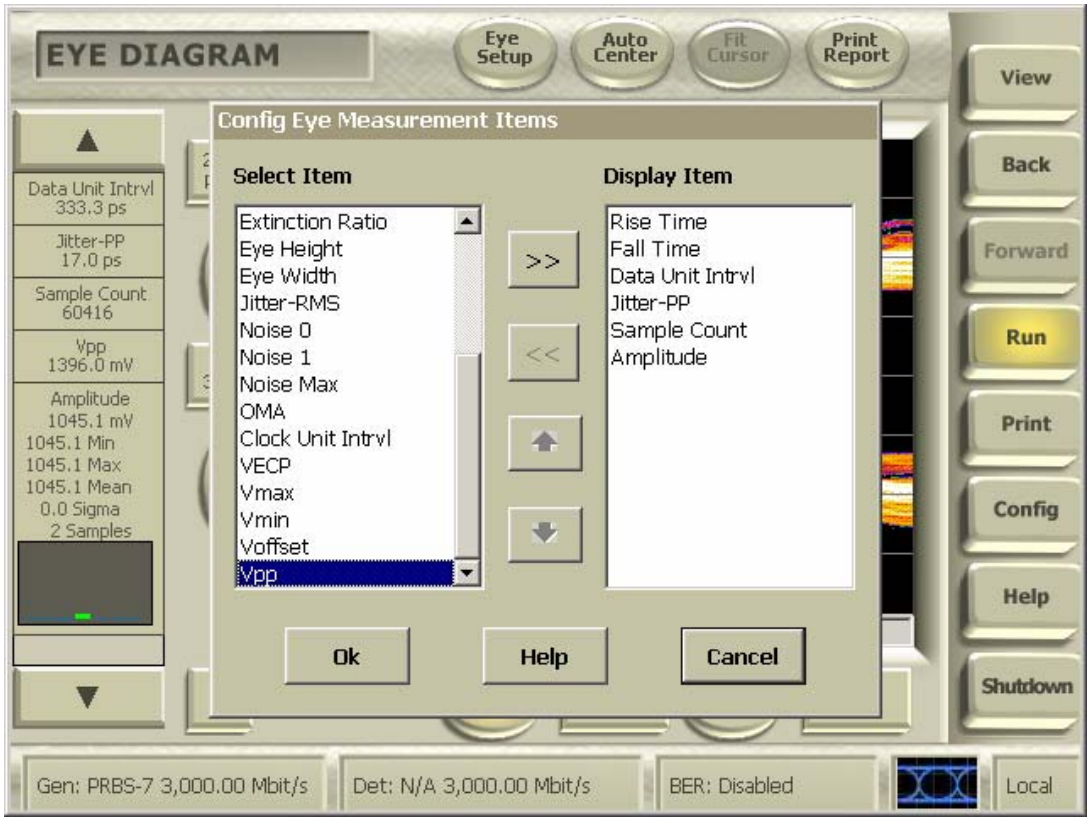
Last Modification: October 30, 2006

Discussion: This test is only run once at the maximum interface rate claimed by the component (1.5Gb/s or 3Gb/s). Differential skew is measured as the difference between the mean of the rising edge in a single-ended eye diagrams of TX+ and the mean of the falling edge in a single-ended eye diagram of TX–, repeat the measurement this time measuring the difference between the mean of the rising edge in a single-ended eye diagrams of TX- and the mean of the falling edge in a single-ended eye diagram of TX+, finally compute the Differential Skew = average of the magnitude (absolute value) of the two mean skews. This removes the effect of rise-fall imbalance from the skew measurement in accordance with section 7.4.12 of the Serial ATA revision 2.5.

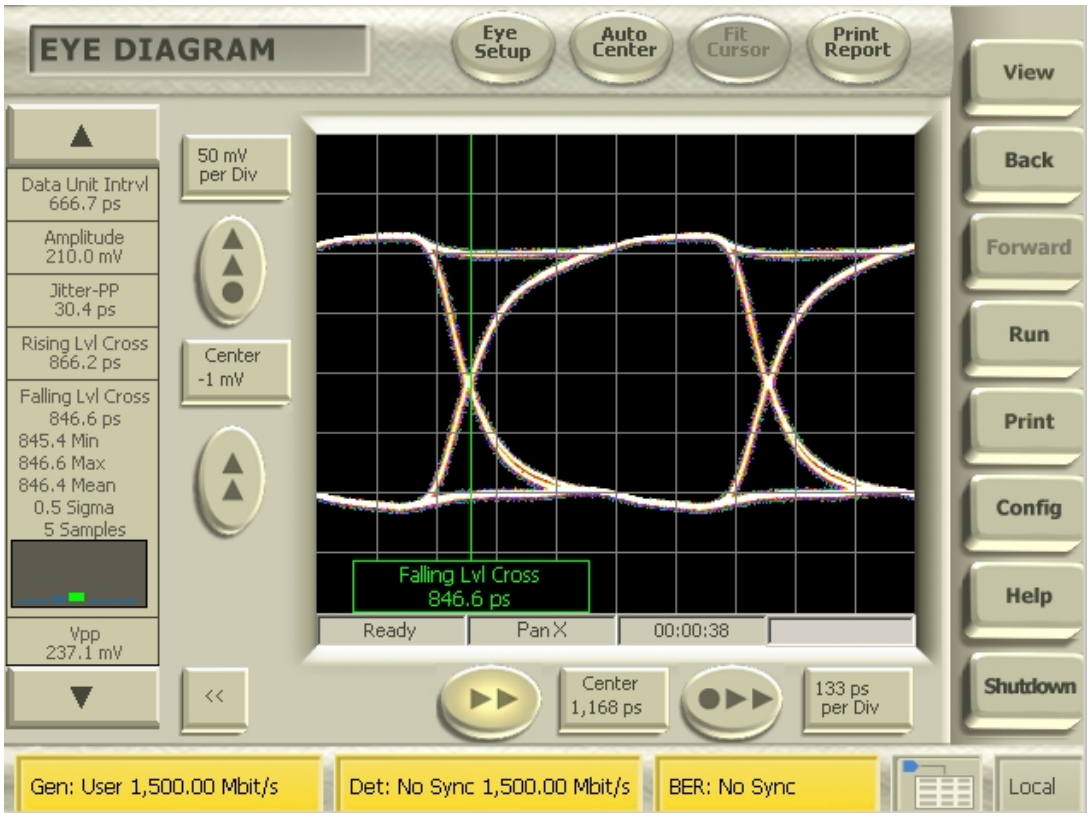
Test Setup as shown in Appendix B: Connect the CR 12500A sub-rate clock output to the BERTScope clock input using the short SMA Male to SMA Male Cable. Connect only the Data Output + port of the CR 12500A to the Data Input + port of the BERTScope using one of the matched pair of cables. Remember to terminate the other CR 12500A Data Output port with the 50 ohms Termination. Connect both of the B+ and B- ports of iSATA receptacle, these are the pins marked 6 and 5 respectively, to SMA Adapter via the short matched pair of SMA Male to Male Cables to the respective CR 12500A Data Input + and - ports.

Test Procedure:

1. On CR 12500A, choose the pre-stored selection: "SATA2 (6.0)"; by pressing "Enter", scroll to the desired setting and press "Enter" again. On the CR 12500A also set the sub-rate clock divider to 1 by scrolling to "SubDiv: 4" press "Enter" select "1" and press "Enter" again.
2. Initiate the PUT transmitting the HFTP pattern (D10.2) at the highest of the 1.5 Gb/s or 3 Gb/s that the PUT claims to be capable of using either the BIST T,S,A mode or other suitable method as described in Appendix A.
3. Connect the PUT to the iSATA receptacle.
4. On the BERTScope, select "View" then "Physical Layer Test" and "Eye Diagram" and click on "Auto Center". Click "Yes" to perform delay line calibrations if prompted by a pop-up window. Select "Eye Setup" then "Configure Measurement" and add "Rising_Edge_Level_Crossing" to the list by highlighting "Rising_Edge_Level_Crossing" click on ">>" and add "Rising_Edge_Level_Crossing" to the list by highlighting "Rising_Edge_Level_Crossing" then click on ">>" and "OK"



5. Record the rising edge level crossing and falling edge level crossing times in ps from the left side bar..



6. Move the cable from the CR 12500A Data Output + port to the CR 12500A Data Output - port. Remember to terminate the Data Output + port with the 50 ohms Termination.
7. Record the rising edge level crossing and falling edge level crossing times of the Data Output – port in ps from the left side bar..
8. The absolute difference between the falling level crossing of the Data Output + port and rising level crossing of the Data Output - port is the mean skew between the falling edge of Data + and the rising edge of Data -.
9. The absolute difference between the rising level crossing of the Data Output + port and falling level crossing of the Data Output - port is the mean skew between the rising edge of Data + to the falling edge of Data -.
10. Compute the Differential Skew = average of the magnitude (absolute value) of the two mean skews.
11. The skew of the matched pair of short SMA Male to SMA Male cables combined with the CR 12500A Data Input to Data Output paths can be calibrated in any of two simple ways: One way is to switch the connections to the pins marked 6 and 5 of the iSATA receptacle and repeat above measurements 5 through 9, the calibrated value is then the average of the two computed differential skews; the other method is to calibrate per procedure in Appendix C and subtract the calibrated setup skew from the measured differential skew. All calibration screen shots need to be saved. This is done by clicking on "Print" and select "Print to file" then create a unique file name for each calibration data including the serial number of the equipment. Additionally the skew of the iSATA receptacle to SMA Female adapter, which is stated on the calibration sheet that comes with the adapter, should also be subtracted.
12. Repeat 2 through 10 with the PUT initiated transmitting the MFTP pattern.

Observable Results: The pass/fail criterion is:

- t_{skewTX} measured shall be less than 20 ps for both HFTP and MFTP measurements.

Resolution: Four measurements of +/-0.1 ps each.

Test Title: TSG-04: AC Common Mode Voltage

Purpose: Verify that the Product Under Test, PUT, meets the AC Common Mode Voltage specification of section 7.2.2.3.5 of Serial ATA revision 2.5 while transmitting a specified patterns, namely MFTP.

Resource Requirements:

- One BERTScope 7500 or BERTScope 12500 with software version 7.3 or later
- One clock recovery instrument BERTScope CR 12500A with software version SW 0.9.6 FPGA 2.8or later
- One iSATA receptacle to SMA Female Adapter, Comax H303000202, H303000204 or equivalent
- One short SMA Male to SMA Male Cable less than or equal to 12" length, Sucoflex 104 or equivalent
- A pair of matched length short SMA Male to SMA Male Cables, Suhner Sucoflex 104 or equivalent
- A pair of matched length low loss SMA Male to SMA Male Cables of approximately 2 meters length, Suhner Sucoflex 106 or equivalent
- One 50 ohms termination, SUHNER 65SMA-50-0-1 or equivalent
- One passive power combiner, Weinschel 1515 or equivalent
- One first order low pass filter having a cutoff equal to the bitrate/2, namely 1.5 GHz.

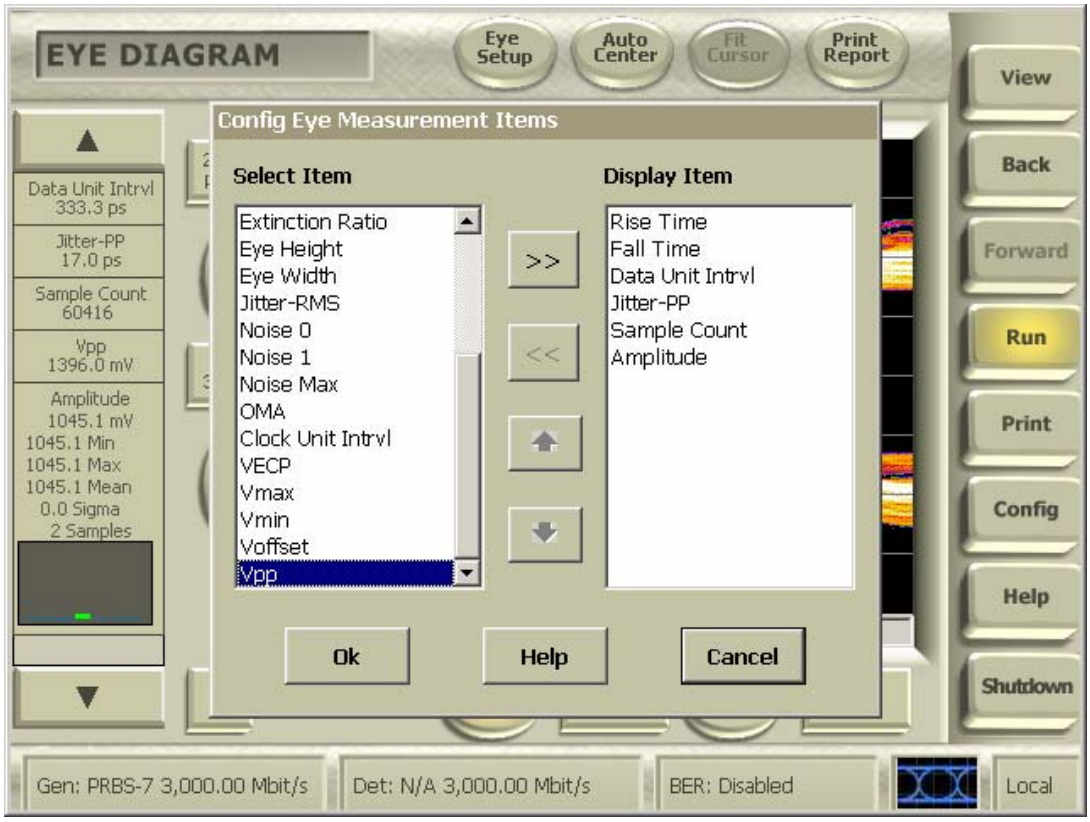
Last Modification: September 14, 2006

Discussion: This test requirement is only applicable to components claiming to be capable of running at 3Gb/s. The AC Common Mode Voltage is a measure of common mode noise other than the CM spikes during transitions due to TX+/TX- mismatch and skews which are limited by the rise/fall mismatch and other requirements. Separate channels are used for TX+ and TX- through the CR 12500A where after they are terminated in a power combiner generating common mode (TX+ + TX-) / 2. This raw common mode shall be filtered with a first order filter having a cutoff equal to the bitrate / 2 to remove the noise contribution from the edge mismatches. The peak-to-peak voltage of the filter output is the AC Common Mode Voltage and shall remain below the specified limit in accordance with section 7.4.17 of the Serial ATA revision 2.5.

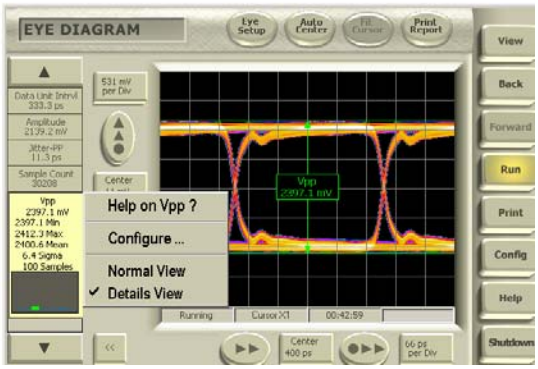
Test Setup as shown in Appendix B: Connect the CR 12500A sub-rate clock output to the BERTScope clock input using the short SMA Male to SMA Male Cable. Connect the Data Output + and - ports of the CR 12500A to the symmetrical input ports of the power combiner using the matched pair of cables. Connect the output of the power combiner to the low pass filter and connect the other end of the low pass filter to the Data Input + port on the BERTScope. Terminate the Data Input – port on the BERTScope with the 50 ohms termination. Connect both of the B+ and B- ports of iSATA receptacle, these are the pins marked 6 and 5 respectively, to SMA Adapter via the short matched pair of SMA Male to Male Cables to the respective CR 12500A Data Input + and - ports.

Test Procedure:

1. On CR 12500A, choose the pre-stored selection: "SATA2 (6.0)"; by pressing "Enter", scroll to the desired setting and press "Enter" again. On the CR 12500A also set the sub-rate clock divider to 1 by scrolling to "SubDiv: 4" press "Enter" select "1" and press "Enter" again.
2. Initiate the PUT transmitting the MFTP pattern at 3 Gb/s using either the BIST T,S,A mode or other suitable method as described in Appendix A.
3. Connect the PUT to the iSATA receptacle.
4. On the BERTScope, select "View" then "Physical Layer Test" and "Eye Diagram". Select "Eye Setup" then "Configure Measurement" and add "Vpp" to the list by highlighting "Vpp" then click on ">>" and "OK"



5. On the BERTScope, select "View" then "Physical Layer Test" and "Eye Diagram". Select "Vpp" and "Detailed View"



6. Record the peak-to-peak voltage, which is the AC Common Mode Voltage.
7. The common mode insertion loss can be calibrated by simply applying a MFTP pattern from the BERTScope Data Outputs with 100 mV of common mode sinusoidal interference turned on to test setup; namely through the matched pair of short SMA Male to SMA Male cables combined with the CR 12500A Data Input to Data Output paths ways, power combiner and low pass filter. The ratio of the 100 mV to the measured calibration signal on the BERTScope is the inverse of the insertion loss. The measured data are then scaled with this factor to obtain the actual values. All calibration screen shots need to be saved. This is done by clicking on "Print" and select "Print to file" then create a unique file name for each calibration data including the serial number of the equipment.

Observable Results: The pass/fail criterion is:

- The measured AC Common Mode Voltage shall be less than 50 mVp-p.

Test Title: TSG-05 : Rise/Fall Time Imbalance

Purpose: Verify that the Product Under Test, PUT, meets the Rise/Fall Imbalance specification of section 7.2.2.3.9 of Serial ATA revision 2.5 while transmitting various specified patterns, namely HFTP (D10.2) and MFTP.

Resource Requirements:

- One BERTScope 7500 or BERTScope 12500 with software version 7.3 or later
- One clock recovery instrument BERTScope CR 12500A with software version SW 0.9.6 FPGA 2.8or later
- One iSATA receptacle to SMA Female Adapter, Comax H303000202, H303000204 or equivalent
- One short SMA Male to SMA Male Cable less than or equal to 12" length, Sucoflex 104 or equivalent
- A pair of matched length short SMA Male to SMA Male Cables, Suhner Sucoflex 104 or equivalent
- A pair of matched length low loss SMA Male to SMA Male Cables of approximately 2 meters length, Suhner Sucoflex 106 or equivalent
- One 50 ohms termination, SUHNER 65SMA-50-0-1 or equivalent.

Last Modification: September 14, 2006

Discussion: This test requirement is only applicable to components claiming to be capable of running at 3Gb/s. In order to determine the imbalance, the single ended 20-80% rise and fall times of both TX+ and TX- shall be determined for a given pattern. Two imbalance values for that pattern are then determined by the two equations:

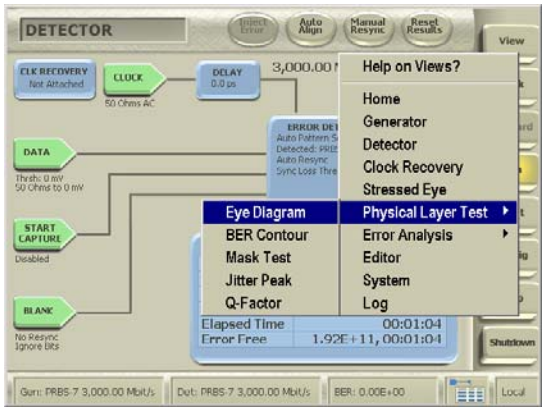
absolute value(TX+,rise – TX-,fall)/average, where average is (TX+,rise + TX-,fall)/2
absolute value(TX+,fall – TX-,rise)/average, where average is (TX+,fall + TX-,rise)/2

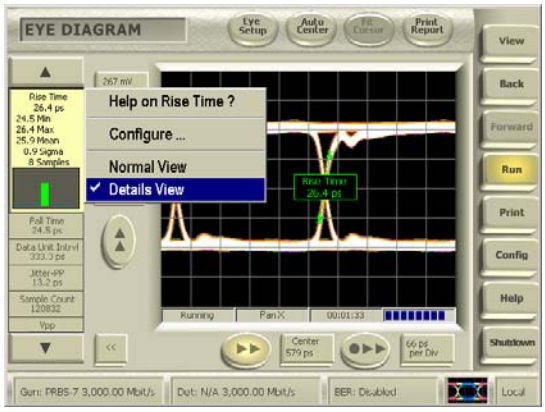
according to section 7.4.16 of the Serial ATA revision 2.5.

Test Setup as shown in Appendix B: Connect the CR 12500A clock output to the BERTScope clock input using the short SMA Male to SMA Male Cable. Connect only the Data Output + port of the CR12500A to the Data Input + port of the BERTScope using one of the matched pair of cables. Remember to terminate the other CR 12500A Data Output port with the 50 ohms Termination. Connect both of the B+ and B- ports of iSATA receptacle, these are the pins marked 6 and 5 respectively, to SMA Adapter via the short matched pair SMA Male to Male Cables to the respective CR 12500A Data Input + and - ports.

Test Procedure:

1. On CR12500A, choose the pre-stored selection: "SATAII (6.0)"; by pressing "Enter", scroll to the desired setting and press "Enter" again.
2. Initiate the PUT transmitting the HFTP pattern (D10.2) at 3 Gb/s using either the BIST T,S,A mode or other suitable method as described in Appendix A.
3. Connect the PUT to the iSATA receptacle.
4. On the BERTScope, select "View" then "Physical Layer Test" and "Eye Diagram" and click on "Auto Center". Click "Yes" to perform delay line calibrations if prompted by a pop-up window. Right click on the "Rise Time" measurement field on the left side bar and select "Detailed View". Wait until the sample counter has reach at least 10,000 and record the mean Rise Time value of TX+.





5. Right click on the "Fall Time" measurement field on the left side bar on the BERTScope and select "Detailed View". Record the mean Fall Time value of the TX+ (no need to wait since the fall time measurements were done simultaneously with the rise time measurements).
6. Move the cable from the CR 12500A Data Output + port to the CR 12500A Data Output - port. Remember to terminate the Data Output + port with the 50 ohms Termination.
7. Repeat 4 through 5.measuring the Rise and Fall times of TX–.
8. Compute the two imbalance values for the pattern determined by the two equations:

   absolute value(TX+,rise – TX-,fall)/average, where average is (TX+,rise + TX-,fall)/2
   absolute value(TX+,fall – TX-,rise)/average, where average is (TX+,fall + TX-,rise)/2.

9. Repeat 2 through 8 with the PUT initiated transmitting the MFTP pattern.

Observable Results: The pass/fail criterion is:

- Each pair of the two Rise/Fall Time Imbalances measured shall be less than 20% for both HFTP and MFTP measurements.

Resolution: <0.6%

Test Title: TSG-06 : Amplitude Imbalance

Purpose: Verify that the Product Under Test, PUT, meets the Amplitude Imbalance specification of section 7.2.2.3.10 of Serial ATA revision 2.5 while transmitting various specified patterns, namely HFTP (D10.2) and MFTP.

Resource Requirements:

- One BERTScope 7500 or BERTScope 12500 with software version 7.3 or later
- One clock recovery instrument BERTScope CR 12500A with software version SW 0.9.6 FPGA 2.8or later
- One iSATA receptacle to SMA Female Adapter, Comax H303000202, H303000204 or equivalent
- One short SMA Male to SMA Male Cable less than or equal to 12" length, Sucoflex 104 or equivalent
- A pair of matched length short SMA Male to SMA Male Cables, Suhner Sucoflex 104 or equivalent
- A pair of matched length low loss SMA Male to SMA Male Cables of approximately 2 meters length, Suhner Sucoflex 106 or equivalent
- One 50 ohms termination, SUHNER 65SMA-50-0-1 or equivalent.

Last Modification: September 14, 2006

Discussion: This test requirement is only applicable to components claiming to be capable of running at 3Gb/s. In order to determine the imbalance, the single ended amplitudes of both TX+ and TX- shall be determined for a given pattern. The imbalance value for that pattern is then calculated by the equation:

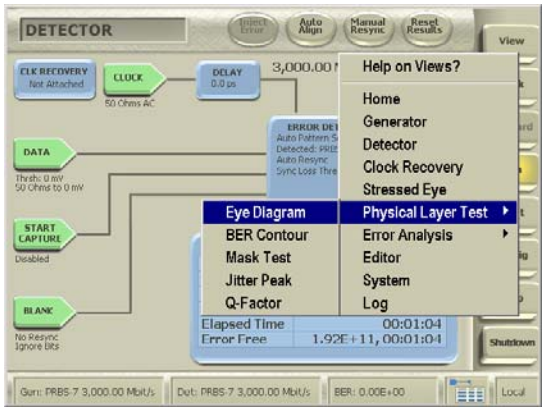
absolute value (TX+amplitude – TX-amplitude)/average, where average is (TX+amplitude + TX-amplitude)/2

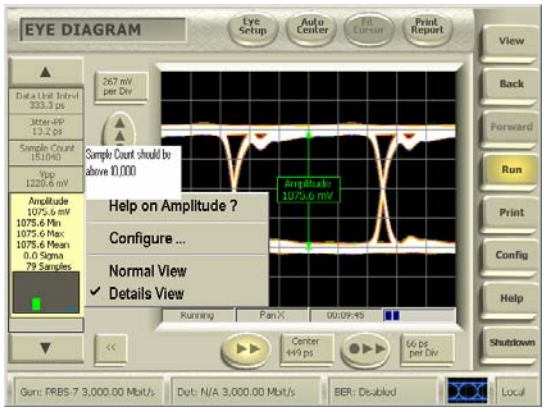
where all amplitudes are determined according to section 7.4.15 of the Serial ATA revision 2.5.

Test Setup as shown in Appendix B: Connect the CR 12500A sub-rate clock output to the BERTScope clock input using the short SMA Male to SMA Male Cable. Connect only the Data Output + port of the CR 12500A to the Data Input + port of the BERTScope using one of the matched pair of cables. Remember to terminate the other CR 12500A Data Output port with the 50 ohms Termination. Connect both of the B+ and B- ports of iSATA receptacle, these are the pins marked 6 and 5 respectively, to SMA Adapter via the short matched pair of SMA Male to Male Cables to the respective CR 12500A Data Input + and - ports.

Test Procedure:

1. On CR 12500A, choose the pre-stored selection: "SATA2 (6.0)"; by pressing "Enter", scroll to the desired setting and press "Enter" again. On the CR 12500A also set the sub-rate clock divider to 1 by scrolling to "SubDiv: 4" press "Enter" select "1" and press "Enter" again.
2. Initiate the PUT in BIST T,S,A mode transmitting the HFTP pattern (D10.2) at 3 Gb/s using either the BIST T,S,A mode or other suitable method as described in Appendix A.
3. Connect the PUT to the iSATA receptacle.
4. On the BERTScope, select "View" then "Physical Layer Test" and "Eye Diagram" and click on "Auto Center". Click "Yes" to perform delay line calibrations if prompted by a pop-up window. Right click on the "Amplitude" measurement field on the left side bar and select "Detailed View". Wait until the sample counter has reached at least 10,000 and record the mode amplitude value of TX+.





5. Move the cable from the CR 12500A Data Output + port to the CR 12500A Data Output - port. Remember to terminate the Data Output + port with the 50 ohms Termination.
6. Repeat 4 through 5.measuring the Amplitude of TX–.
7. Compute the imbalance value for the pattern determined by the equation: absolute value of (TX+amplitude – TX-amplitude)/average, where average is (TX+amplitude + TX-amplitude)/2
8. Repeat 2 through 7 with the PUT initiated transmitting the MFTP pattern.

Observable Results: The pass/fail criterion is:

- The mean Amplitude Imbalances measured shall be less than 10% for both HFTP and MFTP measurements.

Test Title: TSG-09: TJ at Connector, Data, 250 UI
Test Title: TSG-10: DJ at Connector, Data, 250 UI

Purpose: Verify that the Product Under Test, PUT, meets the TJ specification of section 7.2.2.3.11 and 7.3 of Serial ATA revision 2.5 while transmitting various specified patterns, namely HFTP (D10.2), LBP and optionally if test time permits SSOP at 1.5 Gb/s.

Resource Requirements:

- One BERTScope 7500 or BERTScope 12500 with software version 7.3 or later
- One clock recovery instrument BERTScope CR 12500A with software version SW 0.9.6 FPGA 2.8or later
- One iSATA receptacle to SMA Female Adapter, Comax H303000202, H303000204 or equivalent
- One short SMA Male to SMA Male Cable less than or equal to 12" length, Sucoflex 104 or equivalent
- A pair of matched length short SMA Male to SMA Male Cables, Suhner Sucoflex 104 or equivalent
- A pair of matched length low loss SMA Male to SMA Male Cables of approximately 2 meters length, Suhner Sucoflex 106 or equivalent.

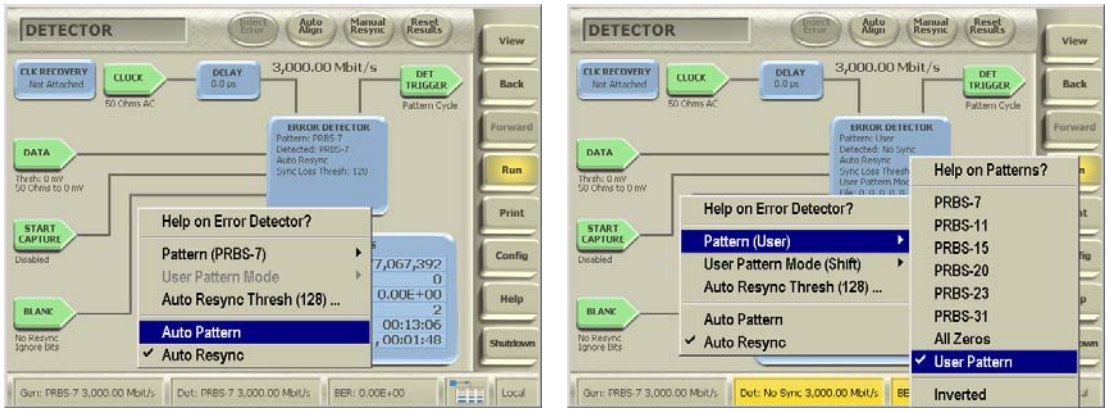
Last Modification: November 6, 2006

Discussion: For components which claim to support 3Gb/s, this requirement must be tested at 1.5Gb/s. The BERTScope simultaneously measures the TJ and DJ for TSG-09 and TSG-10 using the BERT method according to section 7.4.8 of the Serial ATA revision 2.5 using the methodology required by the following text of the Serial ATA Interoperability Program Unified Test Document, LogoTF_ILunified_v1_0RC2f.doc: "For this test, the methodology of obtaining the results must follow a filtered TIE based method, similar to that for obtaining results for TSG-11 and TSG-12. In the past, an N-cycle method was used but is no longer preferred for the use of the interoperability testing."

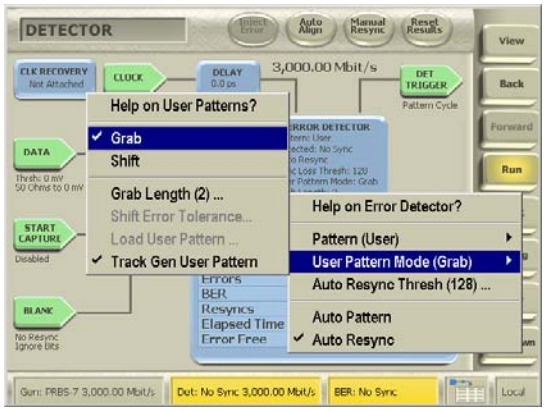
Test Setup as shown in Appendix B: Connect the CR 12500A sub-rate clock output to the BERTScope clock input using the short SMA Male to SMA Male Cable. Connect the Data Output + and - ports of the CR 12500A to the Data Input + and – ports of the BERTScope using the matched pair of cables. Connect both of the B+ and B- ports of iSATA receptacle, these are the pins marked 6 and 5 respectively, to SMA Adapter via the short matched pair of SMA Male to Male Cables to the respective CR 12500A Data Input + and - ports.

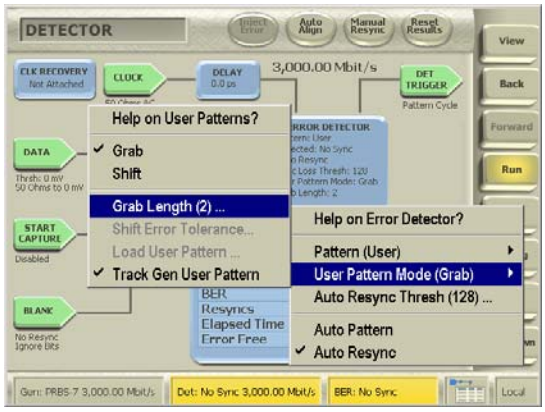
Test Procedure:

1. On CR 12500A, choose the pre-stored selection: "SATA1 (6.0)"; by pressing "Enter", scroll to the desired setting and press "Enter" again. On the CR 12500A also set the sub-rate clock divider to 1 by scrolling to "SubDiv: 4" press "Enter" select "1" and press "Enter" again.
2. On the BERTScope, select "View" then "Detector". Click on "Error Detector", deselect "Auto Pattern". Click on "Error Detector" again, select "Pattern" and click on "User Pattern".

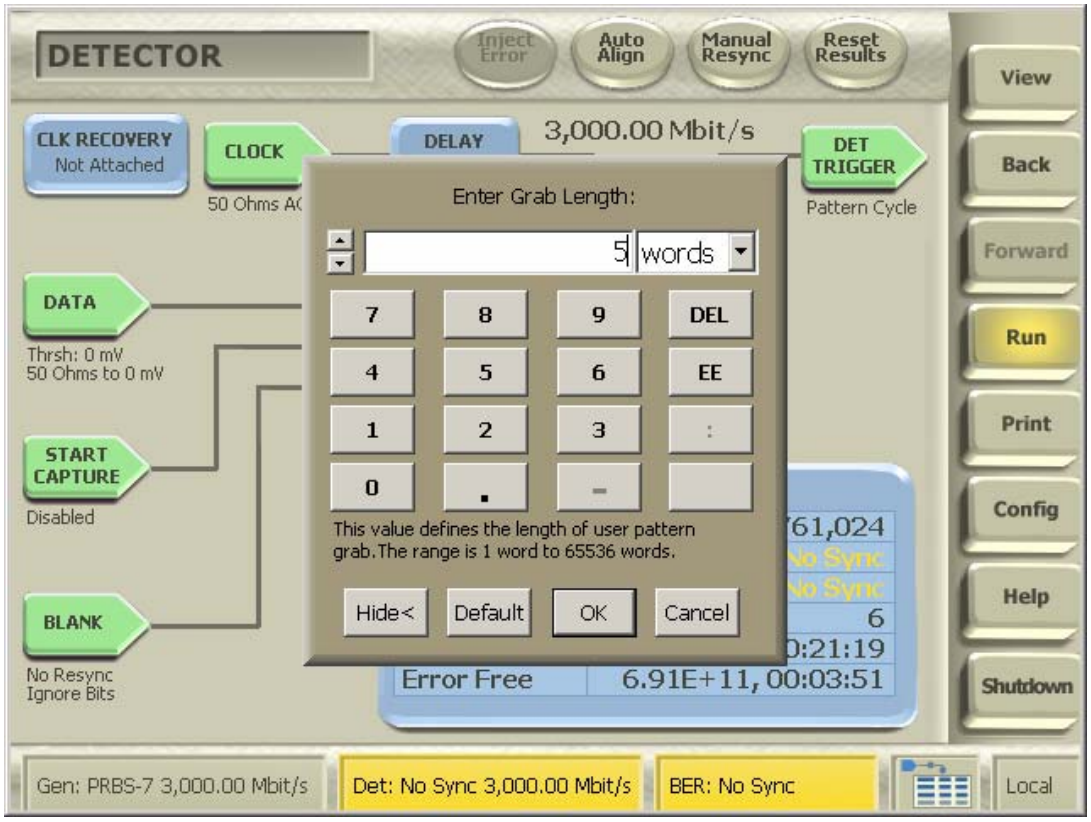


3. Click on "Error Detector" a third time, select "User Pattern Mode" and click on "Grab". Click a fourth time on "Error Detector", select "User Pattern Mode" again and click on "Grab Length".

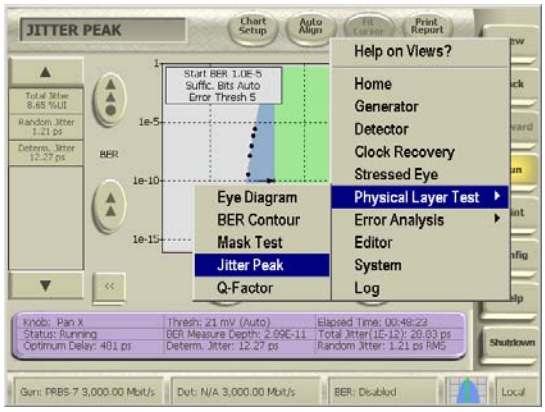


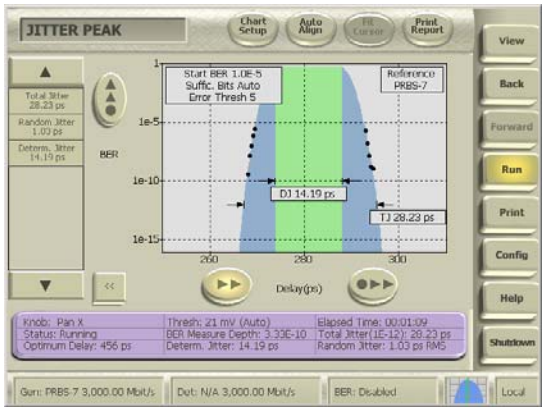


Enter "5" setting the grab length to 5 words and click "OK".

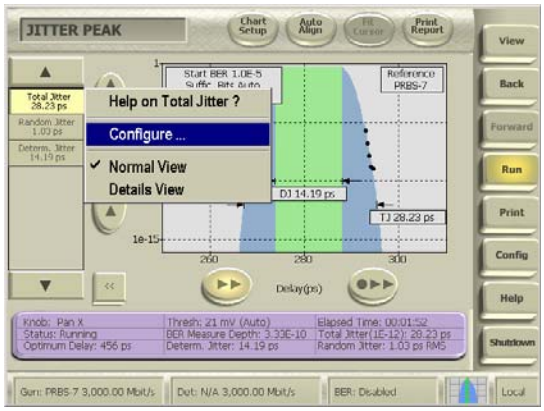


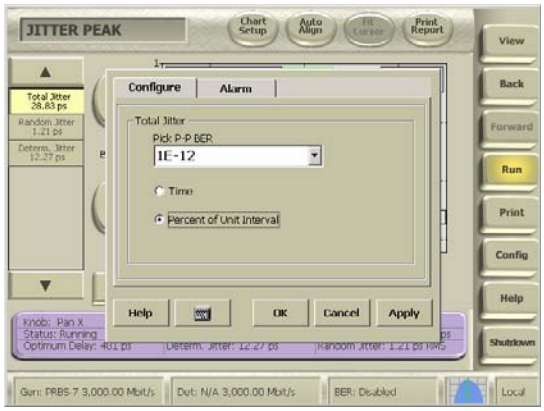
4. Initiate the PUT transmitting the HFTP pattern using either the BIST T,S,A mode or other suitable method as described in Appendix A.
5. Connect the PUT to the iSATA receptacle
6. On the BERTScope, select "View" then "Physical Layer Test" and "Jitter Peak" and click on "Auto Align". Click "Yes" to perform delay line calibrations if prompted by a pop-up window. Wait until at least three points has been measured on each side of the Jitter Peak and record the TJ value in UI (DJ may be recorded at the same time as this completes the TSG-10 measurement as well).





The measurement units can be altered from pico seconds to UI by right click on “Total Jitter” on the left side bar; then click on “Configure”, select “Percentage Unit Interval”, click “OK”.





7. Repeat 4 through 6 with the PUT initiated transmitting the LBP pattern.

8. Optionally repeat 4 through 6 with the PUT initiated transmitting the SSOP pattern.

Observable Results: The pass/fail criteria are:

- TJ measured must be less than 0.37 UI at 1.5 Gb/s for each of the test patterns.
- DJ measured must be less than 0.19 UI at 1.5 Gb/s for each of the test patterns.

Test Title: TSG-11: TJ at Connector, Clock, 500
Test Title: TSG-12: DJ at Connector, Clock, 500

Purpose: Verify that the Product Under Test, PUT, meets the TJ specification of section 7.2.2.3.12 and 7.3 of Serial ATA revision 2.5 while transmitting various specified patterns, namely HFTP (D10.2), LBP and optionally if test time permits SSOP at 3 Gb/s.

Resource Requirements:

- One BERTScope 7500 or BERTScope 12500 with software version 7.3 or later
- One clock recovery instrument BERTScope CR 12500A with software version SW 0.9.6 FPGA 2.8or later
- One iSATA receptacle to SMA Female Adapter, Comax H303000202, H303000204 or equivalent
- One short SMA Male to SMA Male Cable less than or equal to 12" length, Sucoflex 104 or equivalent
- A pair of matched length short SMA Male to SMA Male Cables, Suhner Sucoflex 104 or equivalent
- A pair of matched length low loss SMA Male to SMA Male Cables of approximately 2 meters length, Suhner Sucoflex 106 or equivalent.

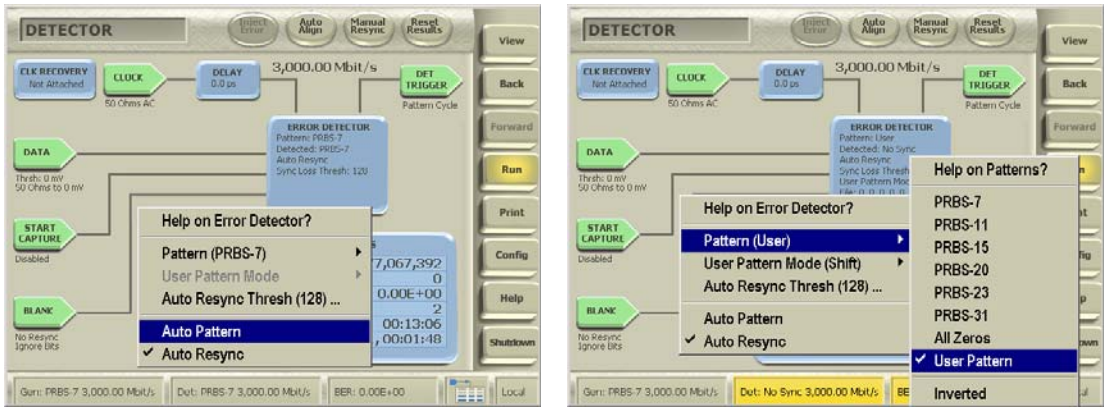
Last Modification: November 6, 2006

Discussion: This test requirement is only applicable to components claiming to be capable of running at 3Gb/s. The BERTScope simultaneously measures the TJ and DJ for TSG-11 and TSG-12 using the BERT method according to sections 7.4.6 and 7.4.8 of the Serial ATA revision 2.5.

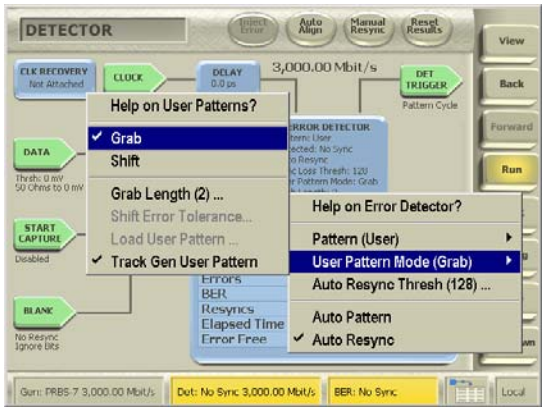
Test Setup as shown in Appendix B: Connect the CR 12500A sub-rate clock output to the BERTScope clock input using the short SMA Male to SMA Male Cable. Connect the Data Output + and - ports of the CR 12500A to the Data Input + and – ports of the BERTScope using the matched pair of cables. Connect both of the B+ and B- ports of iSATA receptacle, these are the pins marked 6 and 5 respectively, to SMA Adapter via the short matched pair of SMA Male to Male Cables to the respective CR 12500A Data Input + and - ports.

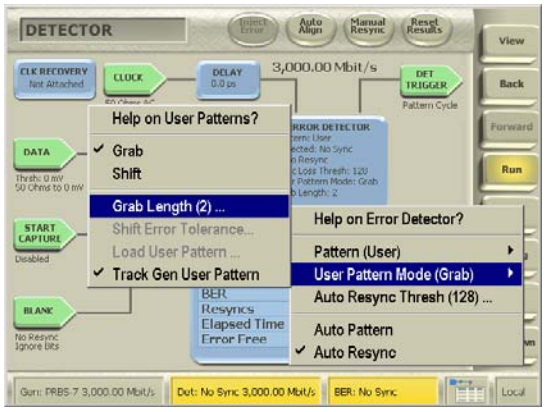
Test Procedure:

1. On CR 12500A, choose the pre-stored selection: "SATA2 (6.0)"; by pressing "Enter", scroll to the desired setting and press "Enter" again. On the CR 12500A also set the sub-rate clock divider to 1 by scrolling to "SubDiv: 4" press "Enter" select "1" and press "Enter" again.
2. On the BERTScope, select "View" then "Detector". Click on "Error Detector", deselect "Auto Pattern". Click on "Error Detector" again, select "Pattern" and click on "User Pattern".

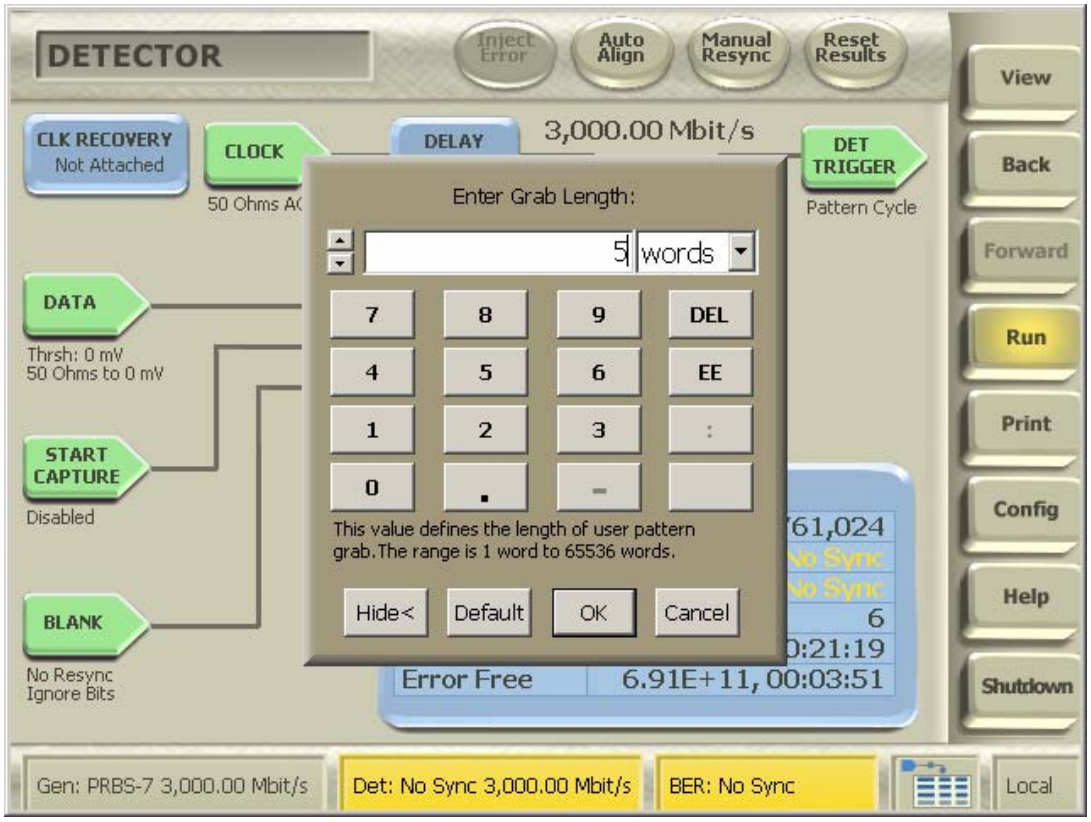


3. Click on "Error Detector" a third time, select "User Pattern Mode" and click on "Grab". Click a fourth time on "Error Detector", select "User Pattern Mode" again and click on "Grab Length".

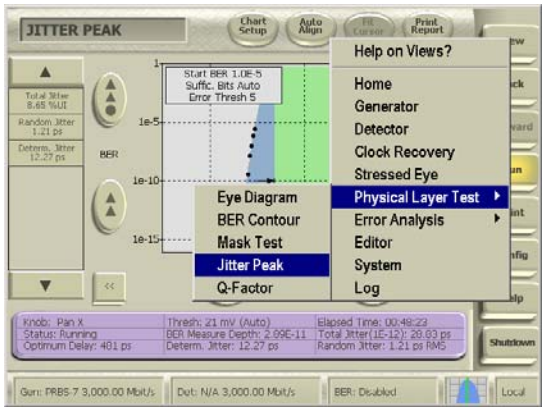


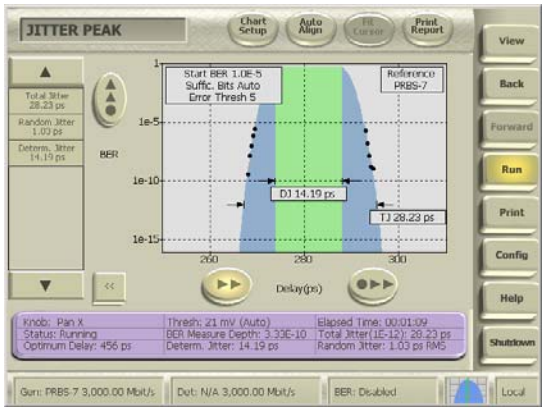


Enter “5” setting the grab length to 5 words and click “OK”.

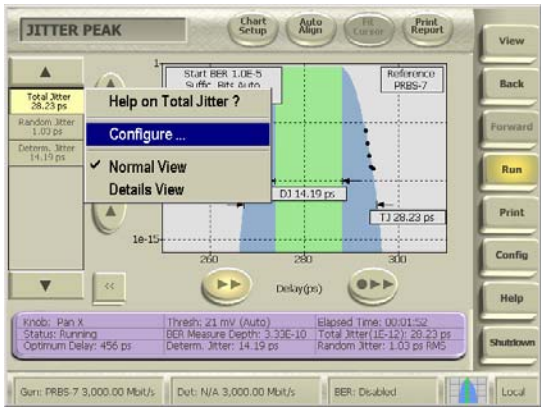


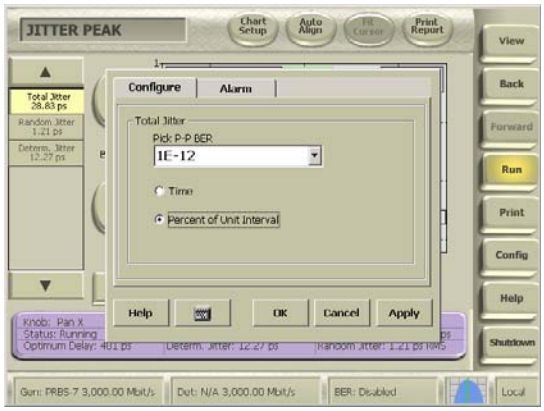
4. Initiate the PUT transmitting the HFTP pattern at 3 Gb/s using either the BIST T,S,A mode or other suitable method as described in Appendix A.
5. Connect the PUT to the iSATA receptacle
6. On the BERTScope, select “View” then “Physical Layer Test” and “Jitter Peak” and click on “Auto Align”. Click “Yes” to perform delay line calibrations if prompted by a pop-up window. Wait until at least three points has been measured on each side of the Jitter Peak and record the TJ value in UI (DJ may be recorded at the same time as this completes the TSG-12 measurement as well).





The measurement units can be altered from pico seconds to UI by right click on "Total Jitter" on the left side bar; then click on "Configure", select "Percentage Unit Interval", click "OK".





7. Repeat 4 through 6 with the PUT initiated transmitting the LBP pattern.

8. Optionally repeat 4 through 6 with the PUT initiated transmitting the SSOP pattern.

Observable Results: The pass/fail criteria are:

- TJ measured must be less than 0.37 UI at 3 Gb/s for each of the test patterns.
- DJ measured must be less than 0.19 UI at 3 Gb/s for each of the test patterns.

Appendix A:

Initiation of PUT using BIST modes.

Purpose: The PUT is placed in one of two BIST modes, namely T+S+A or L and programmed with the desired test pattern as an initiation before the BERTScope measurements.

References:

1. Serial ATA version 2.5, SerialATA_Revision_2_5_RC.pdf, section 10.3.9 BIST Active
2. U-Link Operating Help Files
3. Catalyst BIST MOI

Resource Requirements:

- Stimulus Tool: Any device or system capable of :
  i. Generating SATA OOB, negotiate speed and bringing the PUT to a state where it can receive a BIST Activate FIS.
  ii. Generating the required BIST Activate FIS, T,S,A or L respectively.

Examples of Stimulus Tools:

- Intel ICH7 based computer with U-Link DriveMaster 2006 software version 3.0.198e or later.
- SCT-BIST Drive
- Serial ATA Protocol Analyzer
  a. Catalyst
  b. Finisar
  c. CATC

Last Modification: September 14, 2006

Discussion: The BERTScope acts as a monitoring tool fully capable of verifying the patterns transmitted by the PUT and merely need a stimulus tool to generate SATA OOB, negotiate speed and bring the PUT to a state where it can receive a BIST Activate FIS in according to section 10.3.9 of the Serial ATA revision 2.5.

Test Setup: Stimulus Tool with an iSATA cable.

Test Procedure:

1. Connect PUT to the Stimulus Tool using the SATA cable.
2. Make sure that the Stimulus Tool is turned on and ready.
3. Allow the PUT to power up and go through OOB.
4. Initiate speed negotiation using the Stimulus Tool if change of speed is required.
5. Generate a BIST Active FIS with the appropriate bits set for either BIST T, A, S, including the pattern words or BIST L as required using the Stimulus Tool.

10.3.9 BIST Activate - Bidirectional

0	Reserved (0)	Pattern Definition T A S L F P R V	R R R R PM Port	FIS Type (58h)
1	Data1 [31:24]	Data1 [23:16]	Data1 [15:8]	Data1 [7:0]
2	Data2 [31:24]	Data2 [23:16]	Data2 [15:8]	Data2 [7:0]

Figure 197 – BIST Activate - Bidirectional

Field Definitions

FIS Type - Set to a value of 58h. Defines the rest of the FIS fields.

PM Port – When an endpoint device is attached via a Port Multiplier, specifies the device port address that the FIS should be delivered to or is received from. This field is set by the host for Host to Device transmission and this field is set by the Port Multiplier for Device to Host transmission. Endpoint devices shall set this field to 0h for Device to Host transmissions.

R - Reserved – shall be cleared to zero.

Pattern Definition

F – Far End Analog (AFE) Loopback (Optional)

L - Far End Retimed Loopback* Transmitter shall insert additional $ALIGN_P$ primitives

T - Far end transmit only mode

A - $ALIGN_P$ Bypass (Do not Transmit $ALIGN_P$ primitives) (valid only in combination with T Bit)

S - Bypass Scrambling (valid only in combination with T Bit)

P - Primitive bit. (valid only in combination with the T Bit) (Optional)

V - Vendor Specific Test Mode. Causes all other bits to be ignored

Data1 – Dword #1 of data information used to determine what pattern is transmitted as a result of the BIST Activate FIS. Applicable only when the T bit is set to one.

Data2 - Dword #2 of data information used to determine what pattern is transmitted as a result of the BIST Activate FIS. Applicable only when the T bit is set to one.

Example Using the U-Link Stimulus Tool:

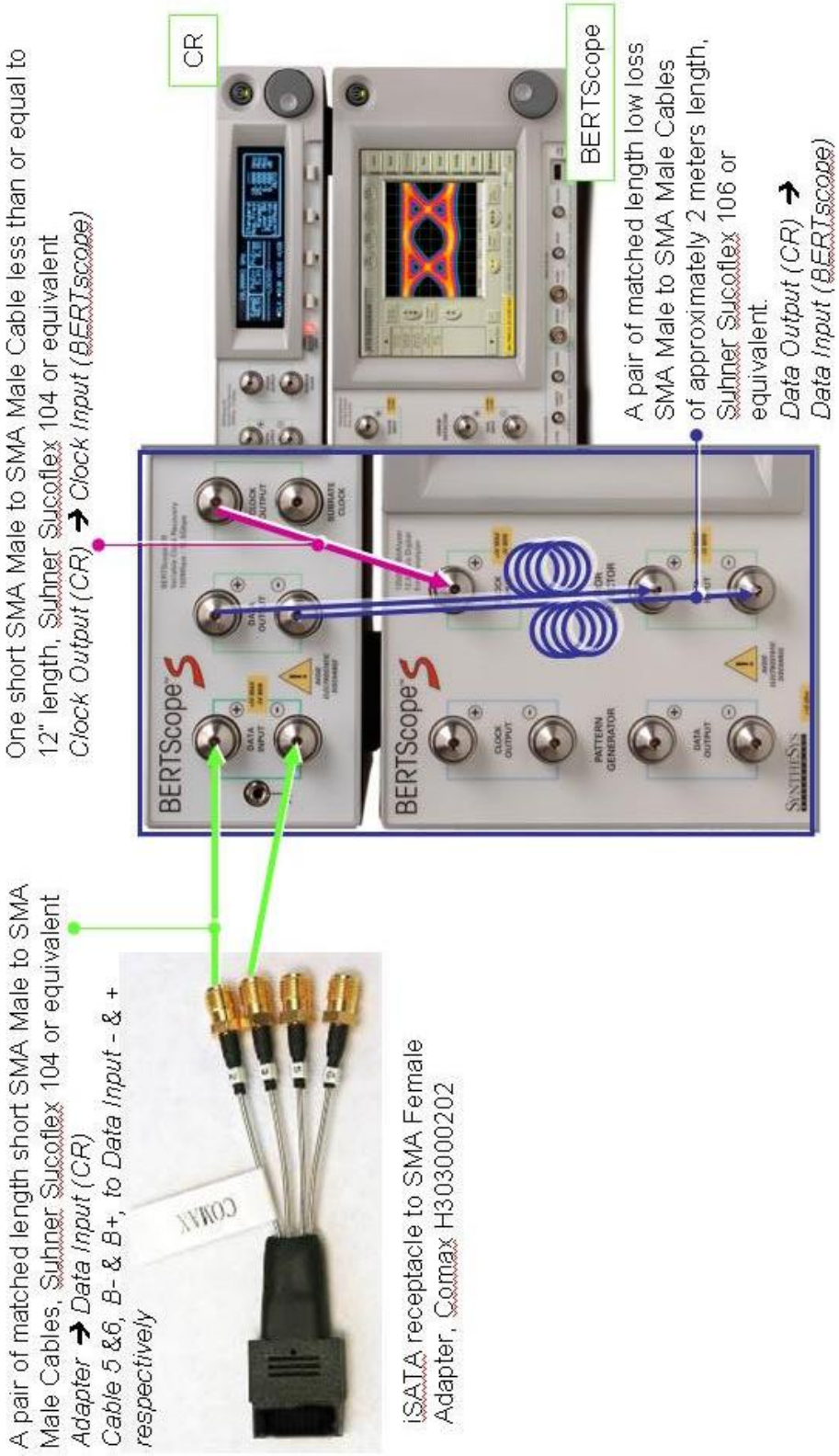
1. Start the U-Link program
2. Click “Power Up” and observe the power supply spin up. Leave it on.
3. Click “CtlSATA”
4. Click COMRESET and observe that COMRESET was received on the log on the right side of the DriveMaster window..
5. Select the appropriate data rate “1” or “2” and observe that the “RDSTATUS” displays “00000113” or “00000123” for 1.5 Gb/s and 3 Gb/s respectively.
6. Select the appropriate “BIST mode T, S, A” for PHY and TSG Testing or “BIST mode L” for RTL Testing
7. When initiating PHY or TSG tests; select the desired pattern from the list.
8. Click “BIST” and observe that “BIST FIS SUCEEDED” is displayed in the lower left corner of the SATA Control Panel.
9. PUT should now be ready for test.

Possible Issues: Some PUTs may require sequences of ALIGN words to be transmitted when switched from the U-Link initiation to the BERTScope set-up when doing RTL tests. This can be accomplished by using the pattern sequencing on the BERTScope having the A pattern be ALIGNs followed by the B pattern being the desirable test pattern. AB patterns are pre-stored on the BERTScope for this purpose.

If the PUT lacks support of physical disconnect then a pair of couplers or power dividers are needed to be able to communicate with the PUT using the U-Link software on the computer and the BERTScope without physical disconnect.

Appendix B:

Serial ATA Interoperability Program Unified Test Setup using BERTScope[1].



[1]Setup including cables and adaptors to have return loss per SATA specifications and be deskewed to within 1 ps.

Appendix C:

Calibration of Test Setup Differential Skew.

Purpose: Calibration of the skew between the Data + and Data - matched pair of short SMA Male to SMA Male cables combined with the CR 12500A Data Input to Data Output paths can improve the accuracy of the differential skew test in TSG-03.

Resource Requirements:

- One BERTScope 7500 or BERTScope 12500 with software version 7.3 or later
- One clock recovery instrument BERTScope CR 12500A with software version SW 0.9.6 FPGA 2.8or later
- One short SMA Male to SMA Male Cable less than or equal to 12" length, Sucoflex 104 or equivalent
- A pair of matched length short SMA Male to SMA Male Cables, Suhner Sucoflex 104 or equivalent
- One low loss SMA Male to SMA Male Cables of approximately 2 meters length, Suhner Sucoflex 106 or equivalent
- One 50 ohms termination, SUHNER 65SMA-50-0-1 or equivalent.

Last Modification: September 14, 2006

Discussion: The skew between the Data + and Data - matched pair of short SMA Male to SMA Male cables combined with the CR 12500A Data Input to Data Output paths can directly increase or decrease the measured differential skew of the PUT. This calibration removes the effect of these skews from the test.

Calibration Setup as shown in Appendix B: Except the BERTScope clock output is connected to the BERTScope clock input using the short SMA Male to SMA Male Cable. Connect only the Data Output + port of the CR 12500A to the Data Input + port of the BERTScope using one of the matched pair of cables. Remember to terminate the other CR 12500A Data Output port with the 50 ohms Termination. Initially connect the BERTScope Data Output + port to the one of the short matched pair of SMA Male to Male Cables that connects to the CR 12500A Data Input + ports.

Calibration Procedure:

1. Use the MFTP pattern, but generated by the pattern generator of the BERTScope Data Output + port. The MFTP pattern is pre-loaded on the BERTScope in "View", then "Generator", click on "Pattern", "User Pattern", "Load User File" then "SATA II" to select a pattern then click "Enable Outputs".
2. On the BERTScope, select "View" then "Physical Layer Test" and "Eye Diagram" and click on "Auto Center". Click "Yes" to perform delay line calibrations if prompted by a pop-up window. Zoom in on the right most crossing by clicking on it and dragging it to the center of the display.
3. Click on "Eye Setup" on the BERTScope then "Cursors" and select "Time Cursors". Place one cursor at the mid point of the rising edge. Place the second cursor near by and zoom in on the mid point by changing the time and/or voltage scale. It is desirable to allow the time scale to show a full 20 ps to either side of the mid point cursor.
4. Move the cable from the CR 12500A Data Output + port to the CR 12500A Data Output - port. Remember to terminate the Data Output + port with the 50 ohms Termination.
5. Connect the BERTScope Data Output + port to the CR 12500A Data Input - port via the other short cable that is used between the iSATA receptacle to SMA Female Adapter and the CR 12500A Data Input - port in the setup to be calibrated.
6. Place the second cursor at the mid point of the rising edge. The delta between the first and second cursor is the skew between the Data + and Data - matched pair of short SMA Male to SMA Male cables combined with the CR 12500A Data Input to Data Output paths.

Observable Results: Record the calibrated differential skew for this value to be subtracted from the measured differential skew in TSG-03.

Appendix D:

Fast SATA Testing.

When testing manually it is recommended to run all tests that require the same PUT pattern in a sequence, then switch pattern and run another sequence of tests in order to expedite and automate testing since the time to initiate PUT in various BIST modes with different patterns take longer time than changing the views on the BERTScope.

To assist the test using sequences the following Table has been provided. For complete test reference one should consult the entire MOI and the following references:

[1] Serial ATA version 2.5, SerialATA_Revision_2_5.pdf
[2] Serial ATA Interoperability Program Unified Test Document, Interop_UnifiedTest_Rev1_1_v092.doc
[3] Serial ATA Interoperability Program Policy Document, Interop_Policy_Rev1_1_v091.doc
[4] ECN 018 against Serial ATA version 2.5.

SATA Test	#1	#2	#3	#4 (optional)
PHY-01	HFTP			
PHY-02	HFTP			
PHY-03	HFTP			
PHY-04	HFTP			
TSG-01	HFTP	LBP	MFTP	
TSG-02	HFTP			
TSG-03	HFTP		MFTP	
TSG-04			MFTP	
TSG-05	HFTP		MFTP	
TSG-06	HFTP		MFTP	
TSG-09*	HFTP	LBP		SSOP
TSG-10*	HFTP	LBP		SSOP
TSG-11	HFTP	LBP		SSOP
TSG-12	HFTP	LBP		SSOP

*at 1.5 Gb/s only

It is further convenient to run all LBP tests through TSG-12 then run the SSOP in the opposite order switch to HFTP and run TSG-09 through TSG-12 followed by PHY-01 through PHY-04 and TSG-01 so that one will run all the differential test that do not require switching cables first and eliminates setting up TSG-12 and TSG-09 one additional time each.

Please also note that each of the pairs of measurement results, TSG-01 and TSG-02; TSG-09 and TSG-10; TSG-11 and TSG-12 are obtained with one test per pattern per pair.

SSOP tests are informative only and therefore kept for the end time permitting.

Appendix E:

Resource Requirements Summary for all PHY and TSG tests as covered by this MOI:

- One BERTScope 7500 or BERTScope 12500 with software version 9.51 or later
- One clock recovery instrument BERTScope CR 12500A with software version SW 0.9.6 FPGA 2.8or later
- One iSATA receptacle to SMA Female Adapter, Comax H303000202, H303000204 or equivalent
- One short SMA Male to SMA Male Cable less than or equal to 12" length, Sucoflex 104 or equivalent
- A pair of matched length short SMA Male to SMA Male Cables, Suhner Sucoflex 104 or equivalent
- A pair of matched length low loss SMA Male to SMA Male Cables of approximately 2 meters length, Suhner Sucoflex 106 or equivalent
- One50 ohms termination, SUHNER 65SMA-50-0-1 or equivalent
- One passive power combiner, Weinschel 1515 or equivalent
- One first order low pass filter having a cutoff equal to the bitrate/2, namely 1.5 GHz.
- Switch, Keithley S46TX0000000TTTTA
- Ethernet to GPIB interface for Keithley switch
- 7 Cables 6" each for switch: 32081-2-29094C-6
- BERTScope Serial ATA Test Fixture for support of non-disconnect PUTs.
- BERTScope Serial ATA Interop Test Suite software, revision 0.7.1
- One BIST initiation tool as per Appendix A

Last Modification: October 30, 2006

Appendix F:

Measurement Accuracy:

The following Table highlights some of the measurement and instrumentation uncertainties related to the PHY and TSG tests. Please note that the full accuracy analysis would be much more comprehensive and include other uncertainties

Test #	Measurement	Uncertainty	Notes
PHY-01	UI	<1 ppm per year plus +/-2.5 ppm -30 to +70 ^{o}C	Time base stability
PHY-02	Long Term Frequency	<1 ppm per year plus +/-2.5 ppm -30 to +70 ^{o}C	Time base stability (see PHY-04 for uncertainties for SSC capable PUTs)
PHY-03	SSC Frequency	<1 ppm per year plus +/-2.5 ppm -30 to +70 ^{o}C 0.1 Hz	Time base stability Display resolution
PHY-04	SSC deviation	<1 ppm per year plus +/-2.5 ppm -30 to +70 ^{o}C 1 kHz (equivalent to 0.33 ppm at 3 Gb/s and 0.66 ppm at 1.5 Gb/s). 311 cycles of SSC provides 189 ppm improving proportional to the square root of the number of 311 cycle measurements averaged. Averaging 100 measurements of 311 cycles each will yield 18.9 ppm resolution.	Time base stability Display resolution Counter resolution
TSG-01	Differential Voltage		
TSG-02	Rise/Fall Time	Two tests of +/-0.1 ps each	Vertical noise is averaged
TSG-03	Skew	Four tests of +/-0.2 ps each	Vertical noise is averaged
TSG-04	AC Common Mode Voltage		
TSG-05	Rise/Fall Time Imbalance	<0.6 %	Vertical noise is averaged
TSG-06	Amplitude Imbalance		
TSG-09	TJ at 1.5 Gb/s		
TSG-10	DJ at 1.5 Gb/s		
TSG-11	TJ at 3.0 Gb/s		
TSG-12	DJ at 3.0 Gb/s		

Appendix G:

Setup Verification and Measurement Data:

Purpose: One time verification that the Setup meets the 20 dB Lab Load return loss requirement of the Serial ATA 2.5 specification.

References:

1. Serial ATA version 2.5, SerialATA_Revision_2_5_RC.pdf, section 7.2.2.5 Lab Load Details

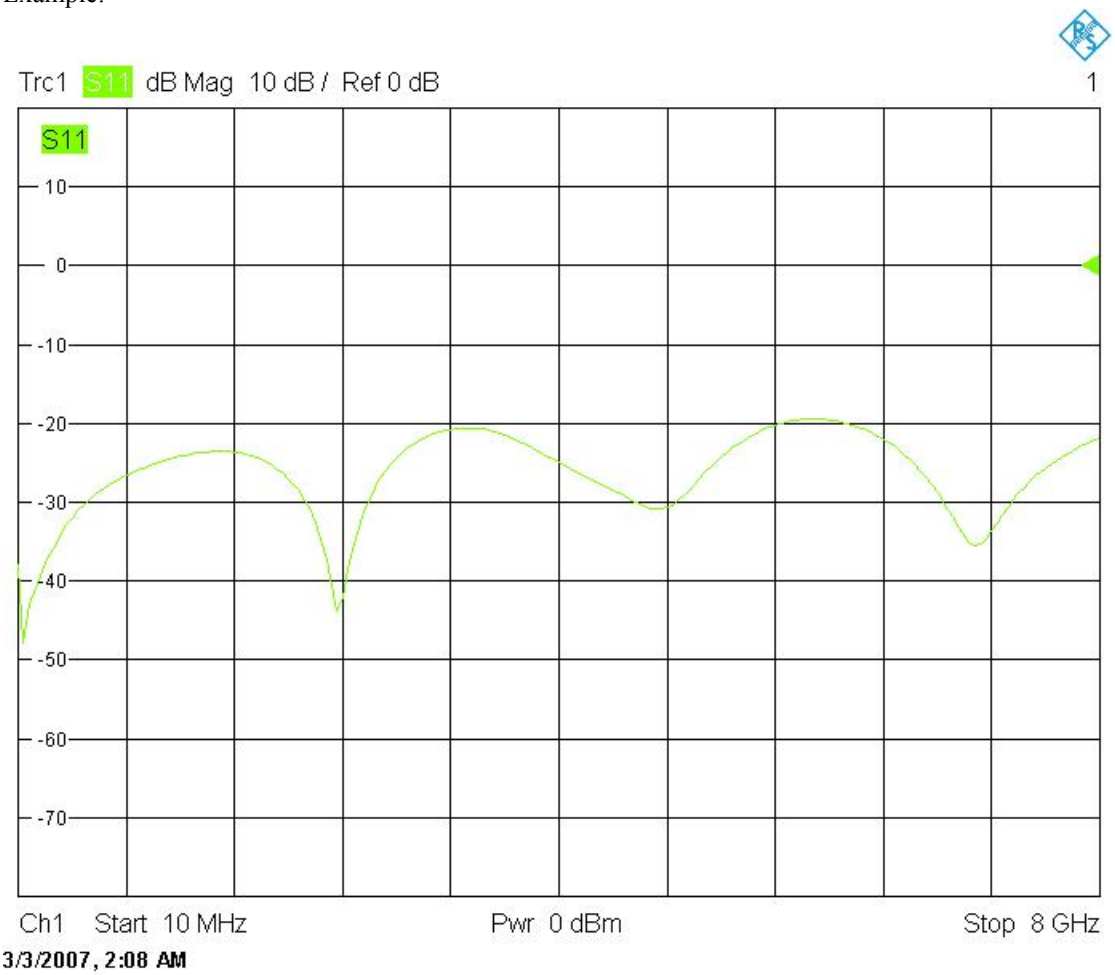
Resource Requirements:

- Time Domain Reflectometer (TDR), BERTScope 7500B or similar
  Or
- Network Analyzer, R&S or similar.

Measurement Description:

1. Calibrate the TDR or VNA following the manufacturers instructions.
2. Measure the Return Loss, S11

Pass/Fail Criteria:

The return loss of the setup shall be better then 20 dB from 100 MHz to 5000 MHz and 10 dB from 5 GHz to 8 GHz.

Example: