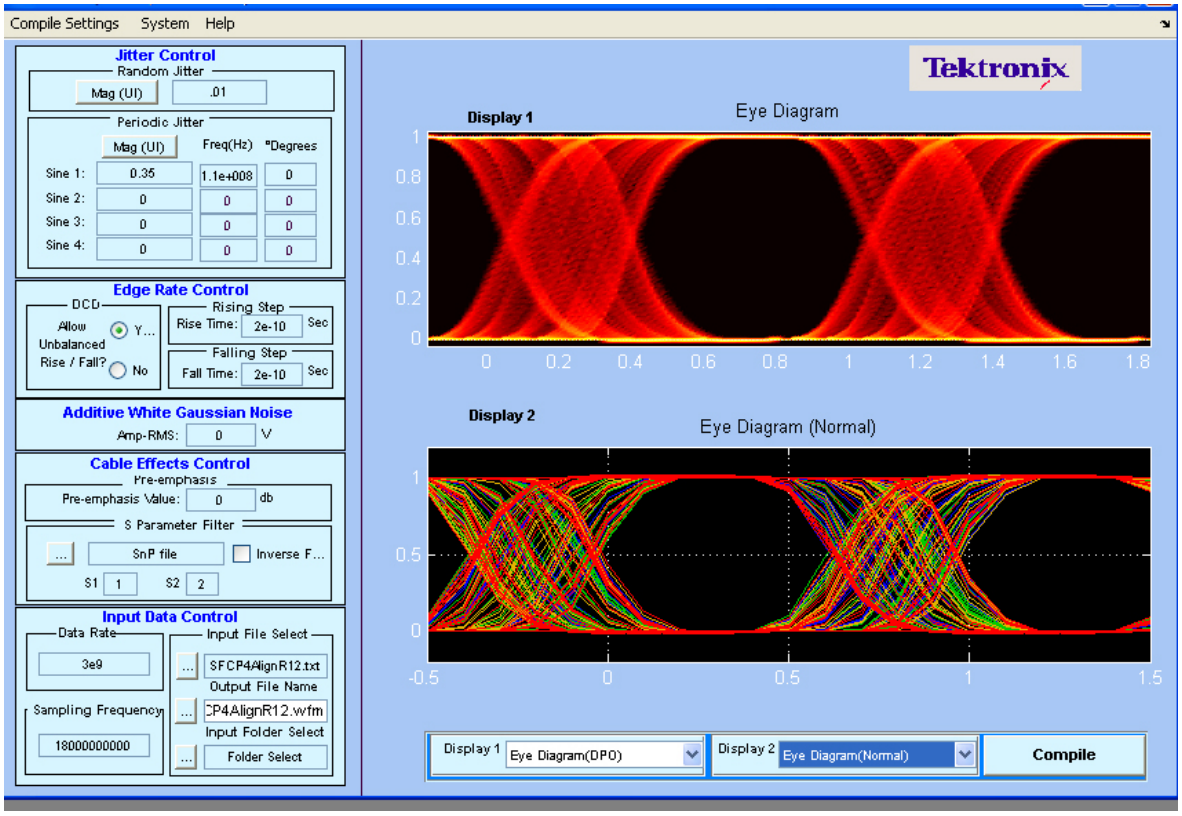
Serial ATA International Organization

Version 1.0
September 27, 2007

Serial ATA Interoperability Program Revision 1.2 Tektronix MOI for RSG Tests (Using AWG7102 and CHS Frame Error Analyzer)



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MODIFICATION RECORD

September 6, 2006 (Version 0.7) INITIAL RELEASE
Mike Martin, John Calvin: RSG MOI contributions

September 7, 2006 (Version 0.71) Updated Test Setup information in Appendix B
Mike Martin

September 19, 2006 (Version 0.72) Updated to reflect the omission of the SSC margin test, and decisions around focusing the tests around 10, 62 and 5 MHZ and increasing the time interval to 20 minutes each.
John Calvin

September 20, 2006 (Version 0.8) Reviewed by SATA IW working group and incorporated comments.
John Calvin

November 15, 2006 (Version 0.81) Revised CHS Frame Error Detector nomenclature.
John Calvin, Daniel Jackson (CHS)

December 14, 2006 (Version 0.82) 2'nd round of review by SATA IW .
John Calvin

April 4, 2007 (Version 0.83) Third round to incorporate introduction of 33 MHZ Sj term, removal of 5MHz term and amplitude calibration methods (Minimum and Maximum).

April 26, 2007 (Version 0.90) Incorporated feedback from review session, clarified the dependency on the true 413 bit pattern required for amplitude measurements and added new logo.

July 12, 2007 (Version 1.0RC) released for general membership review.

September 26, 2007 (Version 1.0) Revised after 90 day general membership review, and submitted for inclusion with the SATA 1.2 IW test program.
Chris Skach

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John Calvin
Mike Martin
Chris Skach

UNH IOL. – Provider of the SATA Framed Composite pattern.
Andrew Baldman

INTRODUCTION

The tests contained in this document are organized in order to simplify the identification of information related to a test, and to facilitate in the actual testing process. Tests are separated into groups, primarily in order to reduce setup time in the lab environment, however the different groups typically also tend to focus on specific aspects of device functionality.

The test definitions themselves are intended to provide a high-level description of the motivation, resources, procedures, and methodologies specific to each test. Formally, each test description contains the following sections:

Purpose

This document outlines precise and specific procedures required to conduct SATA IW 1.2 tests, as they pertain to receiver testing. This document covers the following tests which are all based around testing the receiver channel using a directly synthesized framed composite pattern with a precise level of digital impairment using an Arbitrary Waveform Generator.

The actual framed Composite pattern utilized is a synthesized version of the pattern outlined in the SATA_Pretest_MOI revision 1.2.

Test Coverage

Phy Receiver Signal Requirements (RSG 1-2), as specified in section 2.15 of the Unified Test Document revision 1.2.

Documents

Reference the Serial ATA document repository found at http://www.serialata.org/testing.asp for most current versions of these documents.

Detailed Tests

Test RSG-01 - Gen1 (1.5Gb/s)Receiver Jitter Test

Purpose: To verify that the SATA Gen1 and Gen2 PUT will receive a 1.5Gbps stressed data pattern without receive errors.

References:

[1] SATA Standard revision 2.5, 7.2.1, Table 24 – Lab-Sourced Signal (for Receiver Tolerance Testing)
[2] Ibid, 7.2.2.6.7 –
[3] Ibid, 7.3 - Jitter
[4] Ibid, 7.4.1 – Frame Error Rate
[5] Ibid, 7.4.9 – Receiver Tolerance
[6] SATA unified test document, 2.15.1

Resource Requirements:

See appendix A

Signal Calibration:

See appendix C.3 for Amplitude calibration Note: this step should precede the Jitter Calibration steps.
See appendix C.1 for Rj calibration
See appendix C.2 for Tj calibration
See appendix C4 for Transition time validation.

Last Template Modification: September 6, 2006 (Version 1.0)

Discussion:

Reference [1] specifies the general RSG conformance limits for SATA devices. This specification includes conformance limits for the Receiver Amplitude. Reference [2] provides the definition of Frame Error Rate for the purposes of SATA receiver testing. Reference [4] defines the measurement requirements for this test.

Test Setup:

Connect equipment as shown in Appendix B, figure 1 or 2 as appropriate.

Use AWG Framed Long COMP Receiver Test Pattern library of stressed data patterns outlined in Appendix D. This library includes 1.5Gbps stressed patterns with sine Dj source frequencies of:

10MHz
33MHz
62MHz

Test Procedure:

This procedure should be applied to the worst case port (in a multi-port system/host) as determined through the worst case port identification MOI.

If necessary, use ancillary equipment to place the SATA product-under-test (host or drive) in BIST-L mode .

Note: In most cases the AWG will complete the entire process from OOB sequencing to BIST-L, and finally issuing a repeating Framed COMP pattern. In certain cases, it may be necessary to use ancillary equipment to properly initiate BIST-L modes of operation..

Once in BIST-L mode, connect the AWG to the PUT.

To validate that the frame error counting HW is functioning properly, recall the error injector (1 Frame Error) framed comp pattern. (SFCP_1ERR_Clean.wfm from the SATA-Gen1-RSG-Compliance.awg setup). Observe that the frame error counter increments by one every time the AWG Run button is pressed. Clear the error counters back to 0 once this has been validated.

Recall the clean (no jitter) framed comp pattern (SFCP_0ERR_Clean.wfm from the SATA-Gen1-RSG-Compliance.awg setup) and run to observe that no frame error count increments are occurring for 1 minute of initial operation.

For each of the three sine jitter (SJ) frequencies defined, apply the appropriate Stressed Framed COMP patterns outlined in Appendix D to the PUT. Perform the Frame Error Count test for each frequency for a period of 20 minutes. Record Frame Error Count for each jitter frequency.

Test pattern setup file :	**SATA usage model:**
SATA-Gen1-RSG-Compliance.awg	1.5Gbps(Gen1)

Observable Results:

Frame Error Counter must record 0 frame errors over a 20 minute period at each of the prescribed jitter frequencies. Record the number of observed errors at each of the three phases of this test.

Accuracy:

Possible Problems:

Test RSG-02 – Gen2 (3 Gb/s) Receiver Jitter Test

Purpose: To verify that the SATA Gen2 PUT will receive a stressed data pattern without receive errors.

References:

[1] SATA Standard revision 2.5, 7.2.1, Table 24 – Lab-Sourced Signal (for Receiver Tolerance Testing)
[2] Ibid, 7.2.2.6.8 –
[3] Ibid, 7.3 - Jitter
[4] Ibid, 7.4.1 – Frame Error Rate
[5] Ibid, 7.4.9 – Receiver Tolerance
[6] SATA unified test document, 2.15.2

Resource Requirements:

See appendix A.

Signal Calibration:

See appendix C.3 for Amplitude calibration Note: this step should precede the Jitter Calibration steps.
See appendix C.1 for Rj calibration
See appendix C.2 for Tj calibration
See appendix C4 for Transition time validation.

Last Template Modification: September 6, 2006 (Version 1.0)

Discussion:

Reference [1] specifies the general RSG conformance limits for SATA devices. This specification includes conformance limits for the Receiver Amplitude. Reference [2] provides the definition of Frame Error Rate for the purposes of SATA receiver testing. Reference [4] defines the measurement requirements for this test.

Test Setup:

Connect equipment as shown in Appendix B, figure 1 or 2 as appropriate.

Use AWG Framed Long COMP Receiver Test Pattern library of stressed data patterns. This library includes 3Gbps stressed patterns with sine Dj source frequencies of:

10MHz
33MHz
62MHz

Test Procedure:

This procedure should be applied to the worst case port (in a multi-port system/host) as determined through the worst case port identification MOI.

If necessary, use ancillary equipment to place the SATA product-under-test (host or drive) in BIST-L mode .

Note: In most cases the AWG will complete the entire process from OOB sequencing to BIST-L, and finally issuing a repeating Framed COMP pattern. In certain cases, it may be necessary to use ancillary equipment to properly initiate BIST-L modes of operation..

Once in BIST-L mode, connect the AWG to the PUT.

To validate that the frame error counting HW is functioning properly, recall the error injector (1 Frame Error) framed comp pattern. (SFCP_1ERR_Clean.wfm from the SATA-Gen2-RSG-Compliance.awg setup). Observe that the frame error counter increments by one every time the AWG Run button is pressed. Clear the error counters back to 0 once this has been validated.

Recall the clean (no jitter) framed comp pattern (SFCP_0ERR_Clean.wfm from the SATA-Gen2-RSG-Compliance.awg setup) and run to observe that no frame error count increments are occurring for 1 minute of initial operation.

For each of the three sine jitter frequencies defined, apply the appropriate Stressed Framed COMP patterns outlined in Appendix D to the PUT. Perform the Frame Error Count test for each frequency for a period of 20 minutes. Record Frame Error Count for each jitter frequency.

Test pattern setup file :	**SATA usage model:**
SATA-Gen2-RSG-Compliance.awg	3Gbps(Gen2)

Observable Results

Frame Error Counter must record 0 frame errors over a 20 minute period at each of the prescribed jitter frequencies.

Accuracy:

Possible Problems:

Appendix A – Resource Requirements

The resource requirements include two separate sets of equipment. The equipment required for PHY and TSG tests is shown in section A.1, and the equipment required for TX and RX tests is shown in section A.2, and the equipment required for OOB tests is shown in section A.3.

A.1 Equipment for verifying Signal Source Calibration

1. Real-time Digital Oscilloscope
   DPO/DSA71254 (or higher), TDS6154C, TDS612C, or TDS6804B (gen1 only!)

2. Test Fixture
   Crescent Heart Software Fixture TF-SATA-NE-XP, TF-SATA-NE-ZP
   or equivalent

3. Cables
   179-4944-00 for valid results using the distributed AWG setup files

4. Software
   Tektronix AWG7000 Framed Long COMP Receiver Test Pattern library
   Tektronix TDSJIT3v2
   Tektronix TDSRT-Eye (RTeye version 2.0.3 or later, SST version 1.1.2 or later)

A.2 Equipment for Performing Receiver Tests

1. Signal Generator
   AWG7102, option 6 and 1 (interleaved output with 20Gs/s sample rate)

2. Frame Error Counter
   Crescent Heart Software SATA-II Probe Adapter

3. Test Fixture
   Crescent Heart Software Fixture TF-SATA-NE-ZP
   or equivalent
4. Cables
   179-4944-00 for valid results using the distributed AWG setup files.
5. Attenuators
   Two 6 dB (2:1) attenuators should inserted at the end of the cables from the AWG attaching to the inputs of the fixtures. Part number (Tek) 015-1001-01 are recommended.

6. SATA BISTFIS initialization system
   Any system capable of controlling Gen1 and Gen2 products-under-test (PUT), and capable of placing the PUT into BIST-L mode. For host testing, this could be a system such as the Catalyst SATA analyzer and device emulator. For drive testing, this could be a system such as the Ulink DriveMaster running on a SATA capable host system. It is possible that the AWG7000 might be used to perform the BIST-L setup, as well as provide the stressed data pattern for receiver testing. It is also acceptable to utilize proprietary solutions to meet this requirement.

7. Software
   Tektronix AWG7000 Framed Long COMP Receiver Test Pattern library
   ftp://ftp.tek.com/outgoing/SATA-Gen2-RSG-Compliance.zip
   ftp://ftp.tek.com/outgoing/SATA-Gen1-RSG-Compliance.zip

Appendix B – Test Setups

Drive receiver tests using BIST-FIS
Once the Device or Drive DUT has been put in BIST-L mode, the Framed Long COMP pattern is applied with the AWG7102, and the frame errors are counted using the Crescent Heart Software SATA-II Probe Adapter using the following configuration:

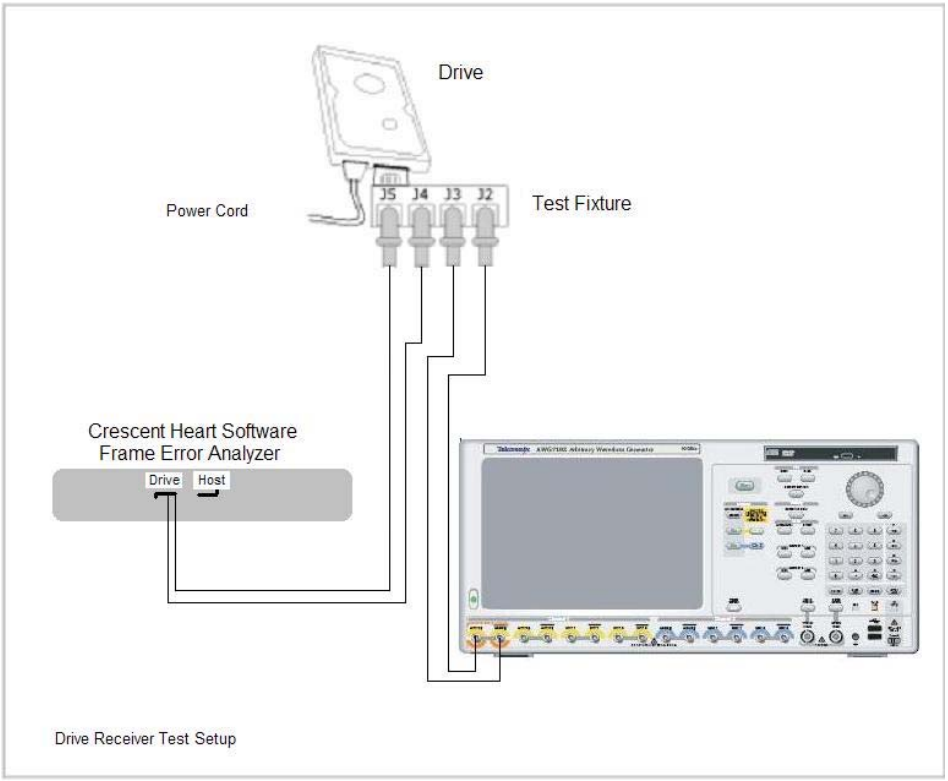
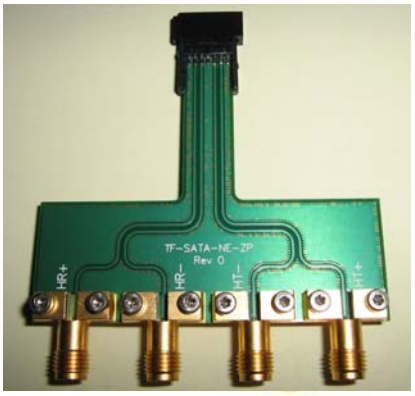


Figure 1: Test the drive receiver using BIST-L

Fixture Pinout Info
For DRIVE connection



J2	J3	J4	J5
Rx+	Rx-	Tx-	Tx+
S2	S3	S5	S6

Host receiver tests using BIST-FIS

Once the Host DUT has been put in BIST-L mode, the AWG7102 is set to generate the Framed Long COMP pattern. Frame Errors are counted by the Crescent Heart Software SATA-II Probe Adapter.

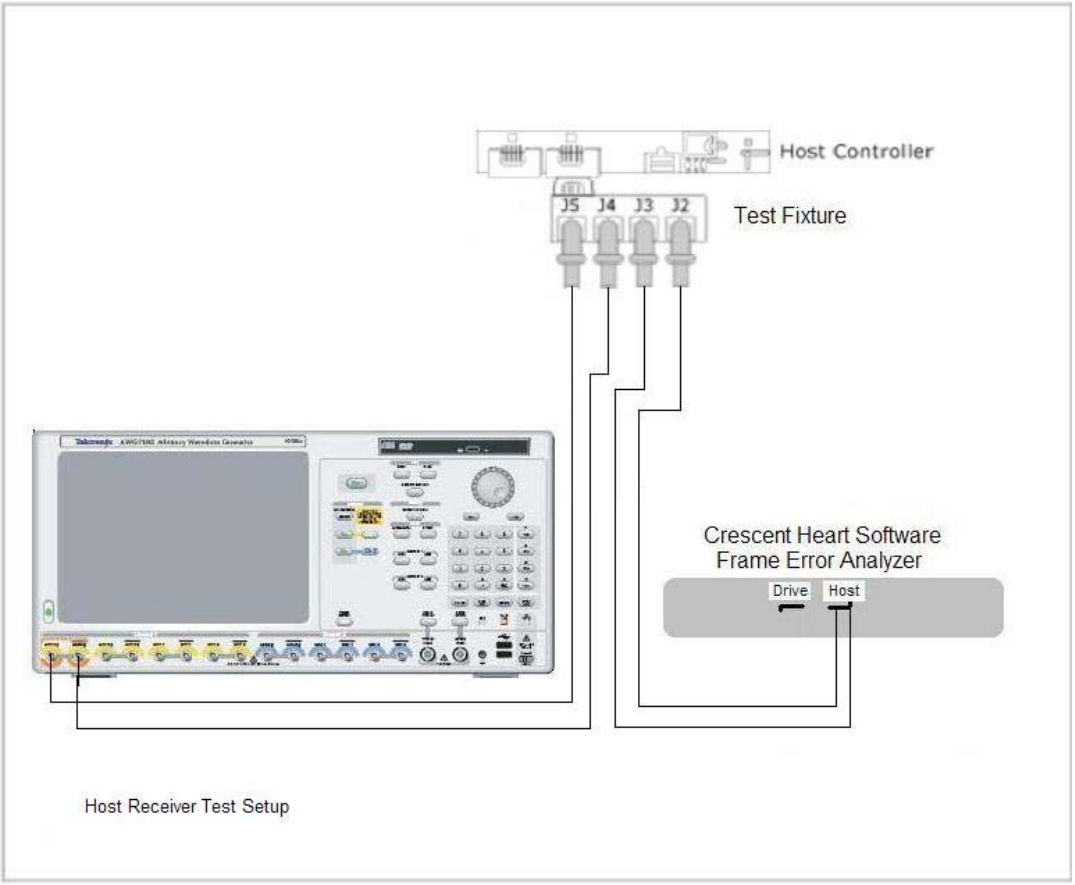
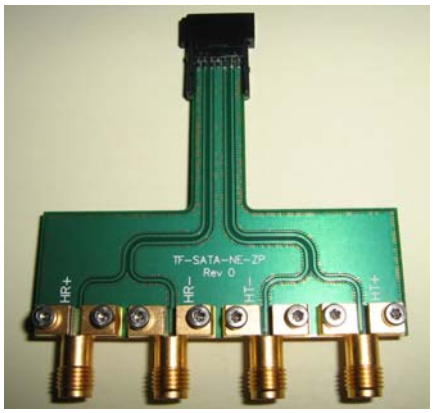


Figure 2: Test the transmitter host DUT using BIST FIS/User method

Fixture Pinout Info
For HOST connection



J2	J3	J4	J5
Tx+	Tx-	Rx-	Rx+
S2	S3	S5	S6

Appendix C – Measurement Calibration

Calibration:

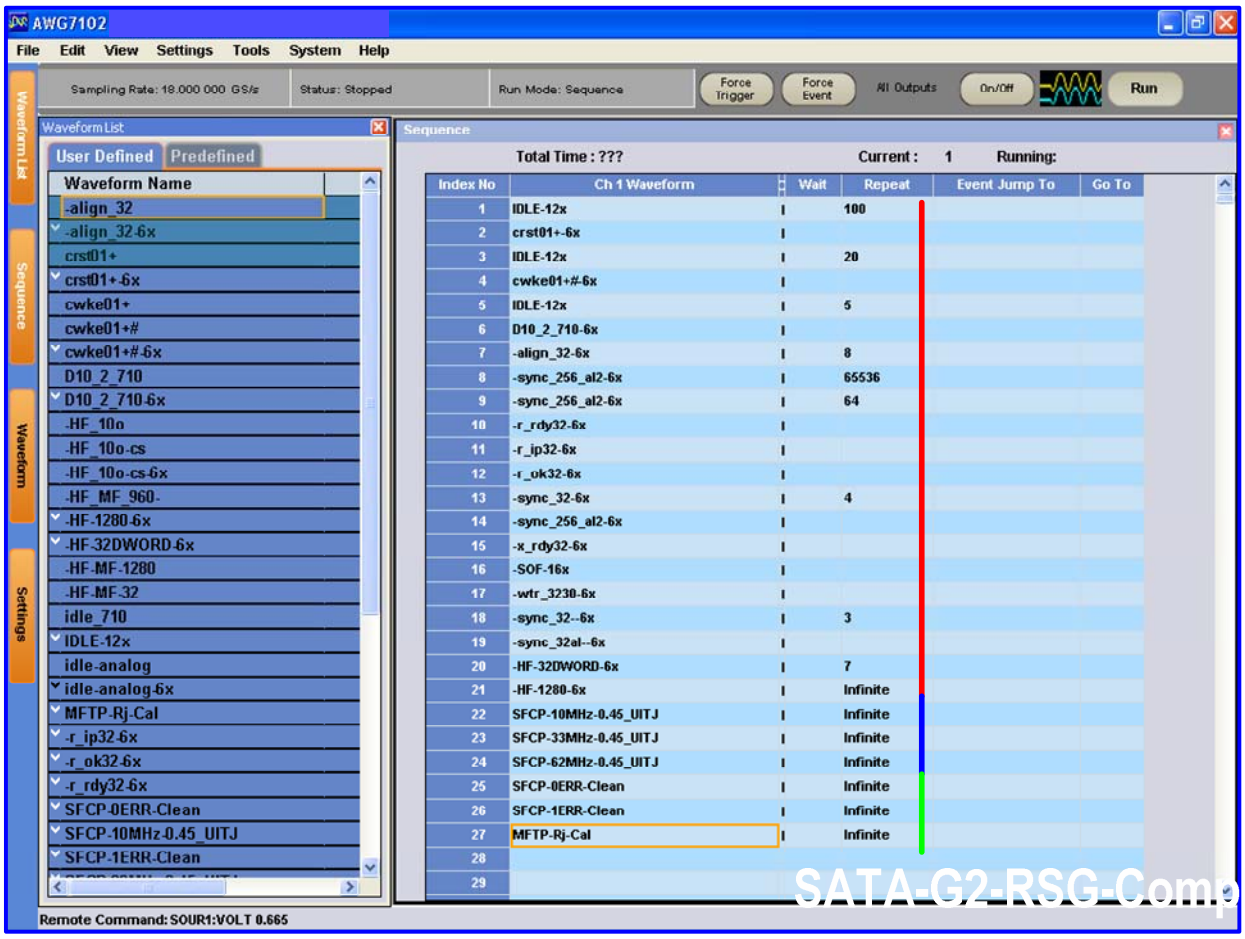


Figure 1: AWG sequence table for the setup file SATA-G2-RSG-Compliance.awg illustrating three principal sets of waveforms. 1. BIST-L initiator, 2. .45UI test vectors and 3. Various diagnostic vectors.

After recalling the SATA-Gn-RSG-Compliance.awg setup , with the output of the AWG directed into CH1 and CH3 of Tektronix Oscilloscope (JNB) as outlined in appendix A.1, One may select the various test or diagnostic vectors sequentially and verify the overall system calibration.

Test Vectors can be individually selected by clicking on the desired sequence and with a right click perform a AWG " force jump here" operation. As these patterns are sequenced for infinite repetition, they will remain in this state until user intervention occurs.

Jitter measurements will be performed using TDSJIT3.V2 using a DATA-TIE (Time Interval Error) without a PLL configuration.

Setups for Jit3V2:

ftp://ftp.tek.com/outgoing/SATA-RSG-Gen-1-Calibration.zip

or **ftp://ftp.tek.com/outgoing/SATA-RSG-Gen-2-Calibration.zip**

Using the appropriate setup files to conduct the following Rj, and Tj jitter calibration steps.

C.1 RJ Calibration

A reference Gen1 and Gen2 MFTP pattern (MFTP-Rj-Cal.wfm) is provided in the AWG bases RSG waveform library support package to facilitate verification of calibration of Rj. Rj is specified to be .18UI PtP @ 7 Sigma or 4.285pSec RMS for Gen2 signaling rates and correspondingly 8.57pSec for Gen1 signaling rates.

The RJ found in the Tektronix AWG MFTP pattern has been synthesized and is a truncated Gaussian distribution with the truncation occurring at 5 Sigma.

Before performing the Rj calibration verification process, perform a SPC calibration on the Tektronix oscilloscope used to host JIT3 and perform a D/A channel calibration on the AWG to ensure instrument environmental conditions have been compensated for.

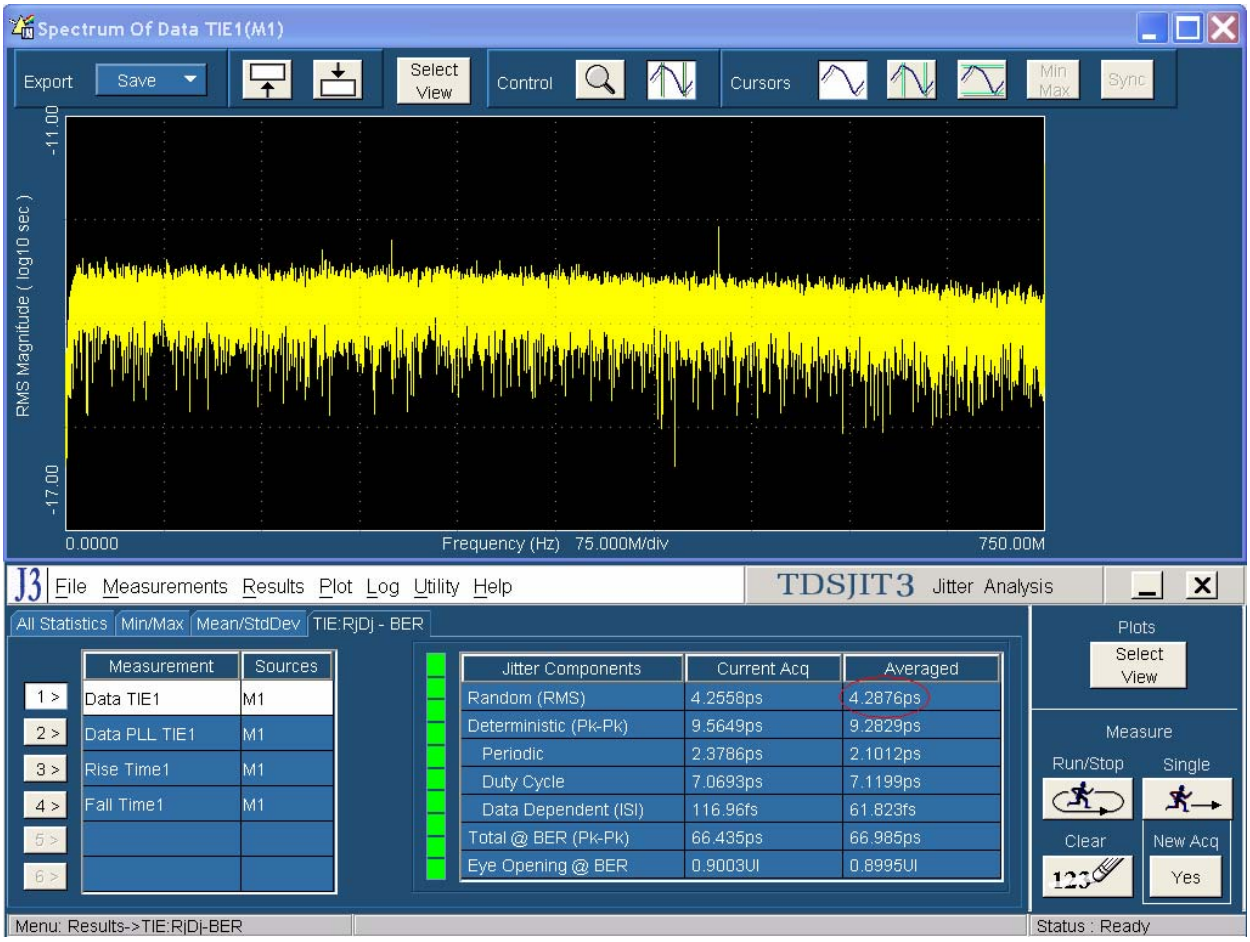


Figure 3: Average Rj value along with a jitter spectrum plot showing Rj content out to Nyquist.

As is illustrated in red circled area of Figure 2, ensure the averaged RJ is nominally reading 4.285pSec RMS +- 4% allowable variation. 4.11pSec < Nominal Value < 4.45pSec. The provided setup file will analyze 16E6 contiguous points per measurement, and 3 runs will typically converge on a averaged RJ close to 4.285pSec. Jitter magnitudes in excess of these values should result in re-calibration of the AWG.

For Gen-1 rates the nominal variation of Rj would be within 8.22 < Nominal Tj Value < 8.9).

C.2 TJ Calibration

The required test waveforms for both Gen1 and Gen2 have been pre-synthesized are provided in the AWG based RSG waveform library support package. These base patterns conform to the IW sanctioned Framed Composite pattern outline in the SATA_Pretest_MOI revision 1.2.

After instructing the AWG sequencer to step to any of the provided SCFP-xxMHz-0.45-UITJ test vectors, Jit-3 should be run and the Total jitter (Total @ BER (Pk-Pk) observed.

Nominal accuracy of a calibrated system will provide .45UI conformance within 4% of nominal error.

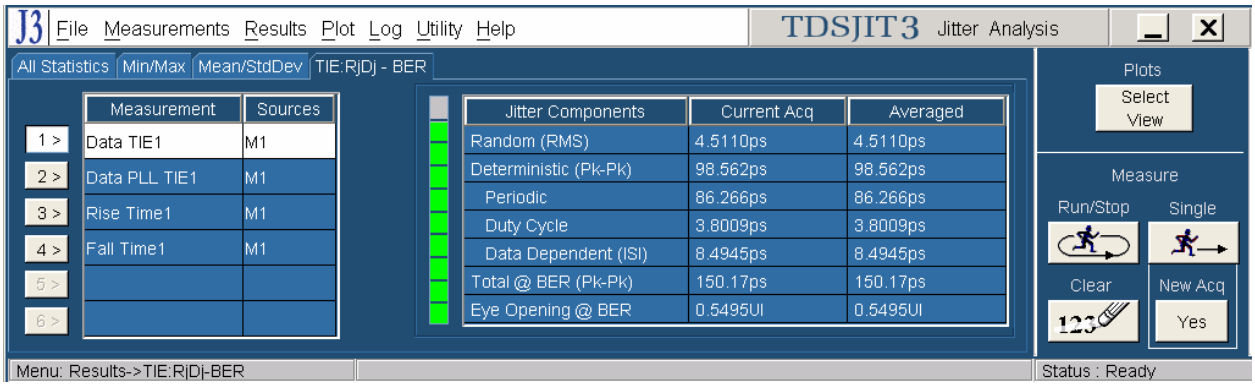


Figure 3: TIE RjDj-BER result Tab for DATA-TIE jitter measurements.

Observe the averaged Total @ BER (Pk-Pk) Jitter value after three acquisitions. The nominal accuracy of a calibrated system will provide .45UI Tj conformance within 4% of nominal error. As such The observed jitter for Gen 2 signaling Tj should nominally be 149.9pSec of Tj +- 4% allowable variation. 144pSec < Nominal Tj Value < 155.8 pSec. Jitter magnitudes in excess of these values should result in re-calibration of the AWG.

For Gen-1 rates the nominal variation of a Nominal value of Tj would be within 288 < Nominal Tj Value < 312pSec)

C.3 Amplitude Calibration

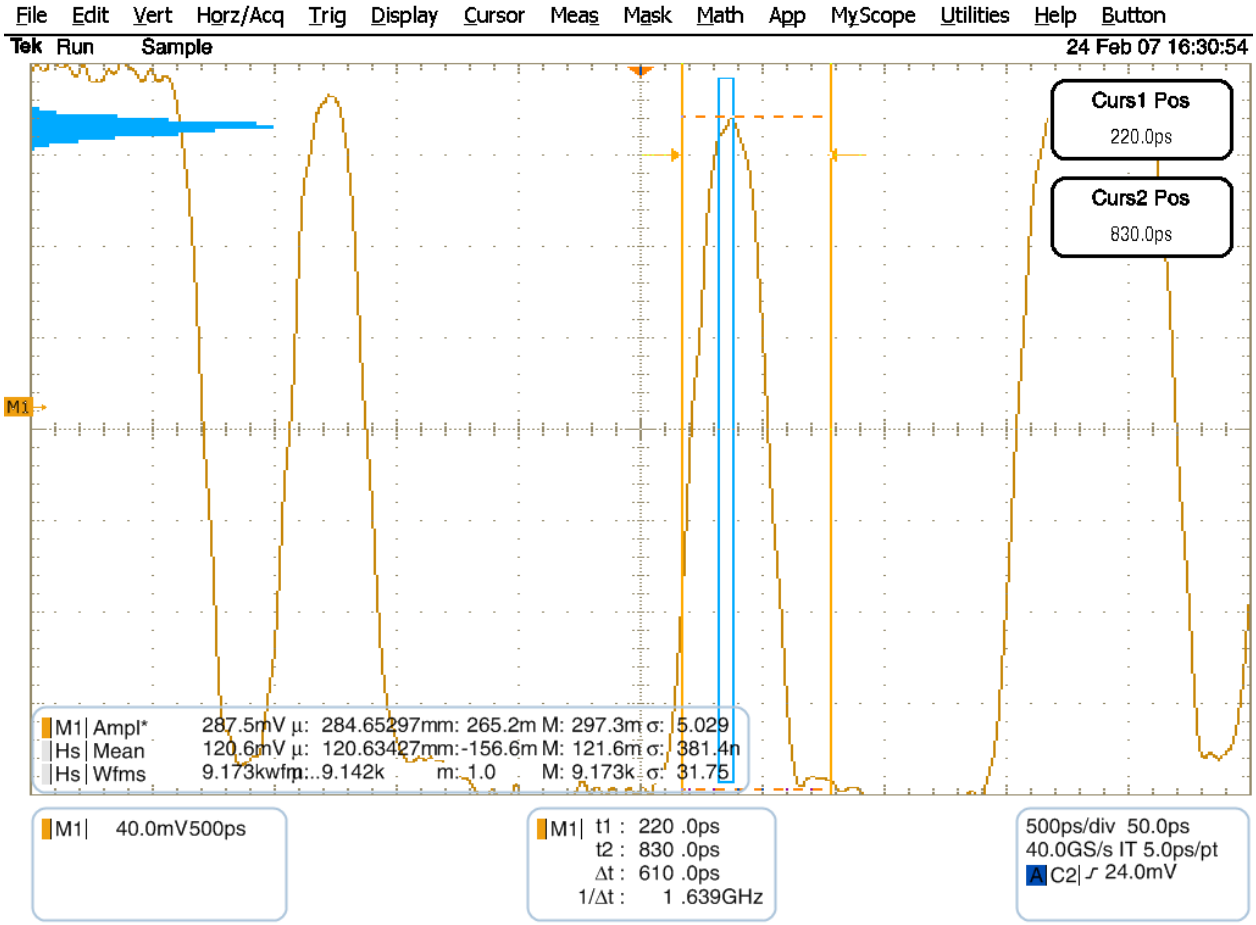
Signal amplitude conformance requires that Gen 1 and Gen 2 signaling not exceed 600mV or 750mV ptp and be within 5% of a target minimum amplitude of 325 and 275mV respectively.

The AWG RSG setup files such as SATA-Gn-RSG-Compliance.awg provide a set of test vectors with predefined minimum amplitude. Fine adjustment may be performed by adjusting the Vertical amplitude setting on the AWG's CH1 output.
The minimum amplitude measurements are performed on both 212141 (negative pulse) and 413 (positive pulse) RL patterns.

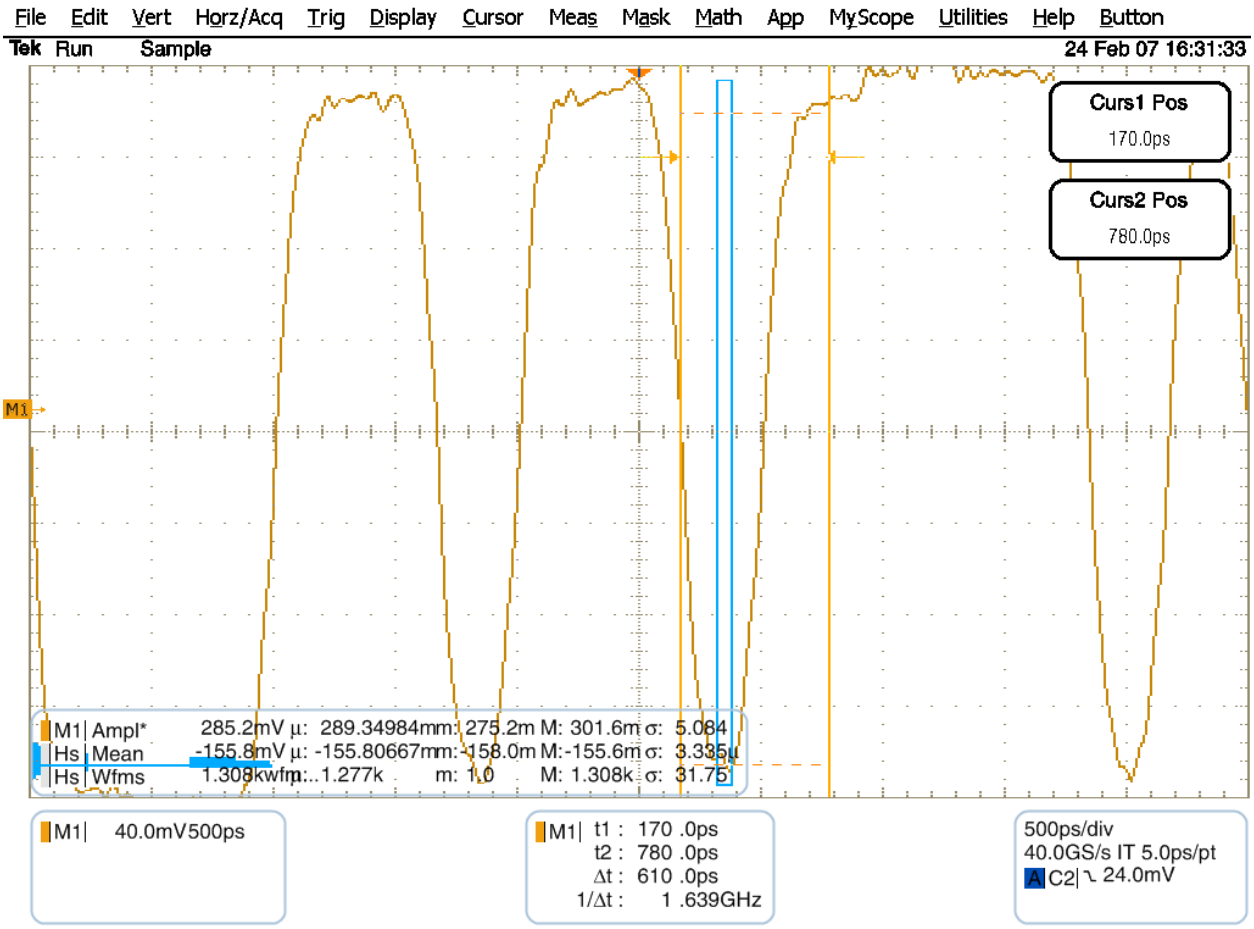
Reference SATA specifications on LBP based amplitude measurements.

The minimum amplitude over a 1UI epoch is the two consecutive bits at the string of a four or more consecutive bits, which is not a representative LBP pattern but is the minimum value in Framed Composite (Pre-ECN18) pattern.

A .45UI to .55UI Histogram is setup on the two lone bits of interest from which the difference of the mean values is computed to obtain the lone pulse amplitudes.



413 (One) LBP Sequence



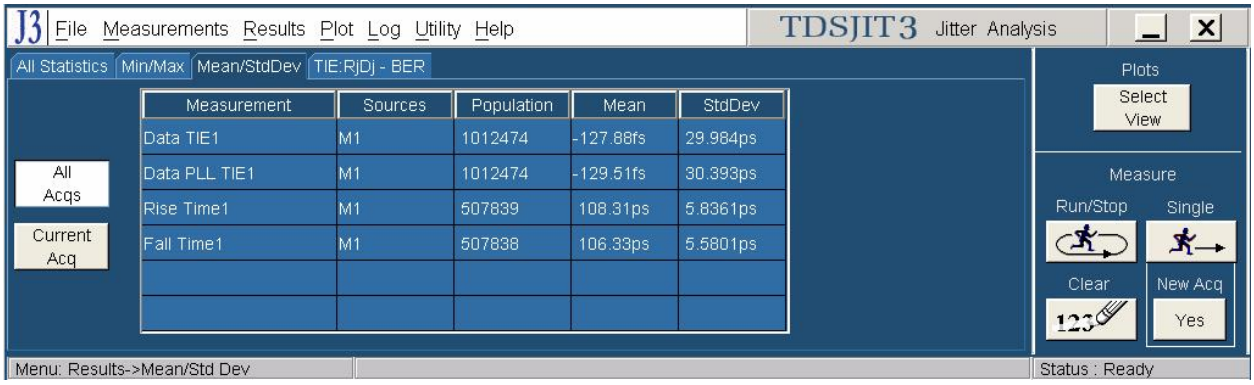
212141 (Zero) LBP Sequence

In this example the difference in the mean histograms is 278.4mv where as the similar native instrument measurement offers a value of 280mV.

Allowable amplitude values will conform to a range of values of 275mV or 325mV +- 13mV. Vertical channel adjustments can compensate for any deviation form these nominal values.

C.4 Transition Time Validation

The same JIT3 setup files used for Jitter calibration/validation have Rise and Fall time measurements which allow the user to validate that the transition rate does not exceed 100pSec 20/80.



JIT3 screen-shot of Framed-Composite signal transition time

Appendix D – AWG-7102 Setups

The AWG-7102 (with Option 6) arbitrary waveform generator is capable of regenerating a SATA Framed Composite pattern with prescribed amount of random and deterministic jitter. These synthesized waveforms are encapsulated in a series of setup files which will recall the waveform pattern to generate, set the proper AWG time-base settings and set the vertical drive amplitude accordingly. Properly calibrated AWG instruments will exhibit an instrument to instrument difference of less than 4% variation.

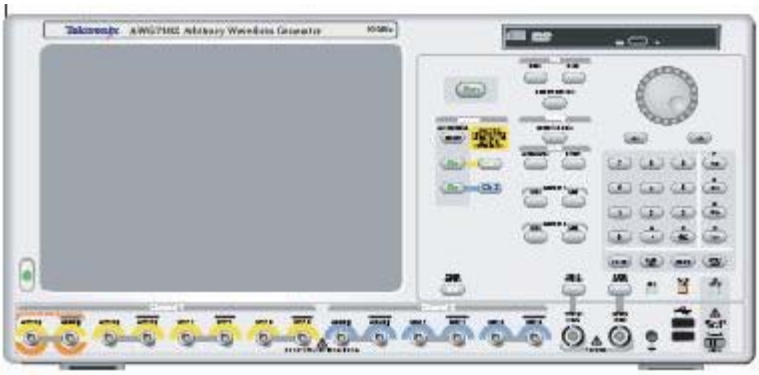
These AWG setup files reflect framed composite patters with five different jitter configurations modulated onto the clean pattern. The Total Jitter observed on these patterns will be .5UI of jitter with .32UI of Deterministic/Sinusoidal jitter and .18UI of Random jitter. The mean transition time for these signals is set to 120pSec, and the signal amplitude set to 325mV ppd (Gen1) or 275mV ppd (Gen2).

D.1 SATA 1.5Gb/Sec AWG7102 setup file descriptions.

SATA-Gen1-RSG-Compliance.awg

D.2 SATA 3.0Gb/Sec AWG7102 setup file descriptions.

SATA-Gen2-RSG-Compliance.awg

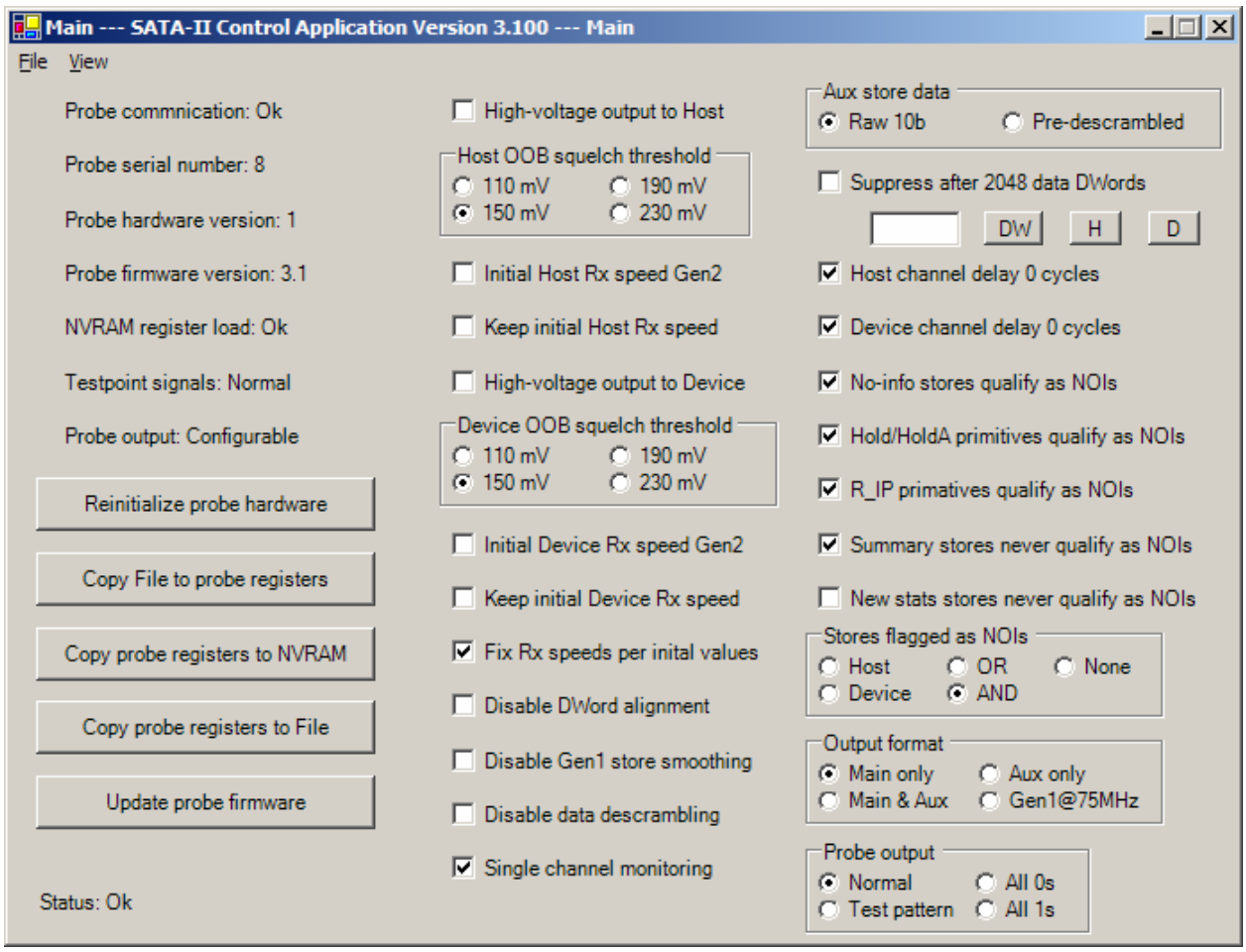


Appendix E – Frame Error Detector

(Crescent Heart Software SATA-II Probe Adapter)

While there are many methods of capturing SATA frame errors, the most inexpensive and easy-to-setup method outlined in this procedure utilizes a Crescent Heart Software SATA-II probe adapter, functioning as a frame error rate (FER) detector. The probe adapter, in addition to tracking and tallying frame errors, can also provide detailed bit- and frame-level protocol information when connected to a Tektronix logic analyzer. Note that use of the SATA-II in FER applications requires an enabling license (part number SATA-II-Option-1).

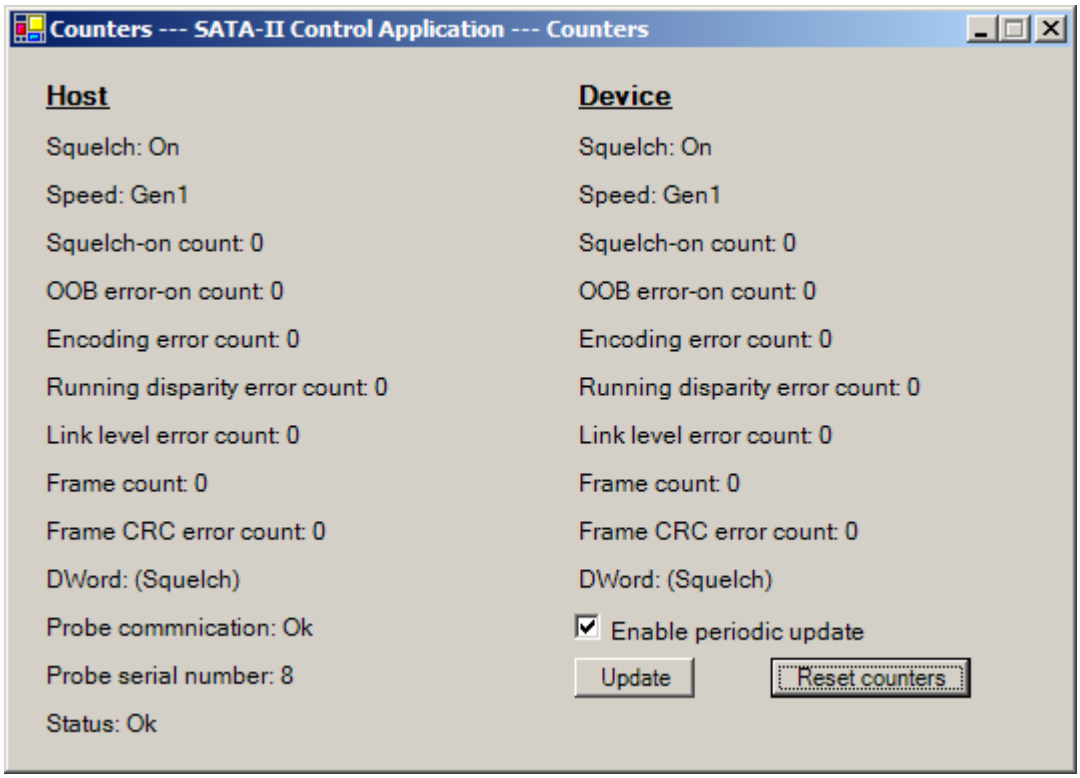
As outlined in Section 9.8 of the SATA-II users' manual, install the SATA-II control application on any host PC or instrument in proximity to the PUT. The SATA-II probe adapter must be powered using the provided DC power supply, and attached via USB cable to the host PC running the control application. After invoking the software the application's main window will be seen, as in Figure A.



A – SATA-II Main Window

The controls in the middle column set as shown above are appropriate for any simple Gen-I FER counting objective outlined in this MOI. For Gen-II use, the Initial Host Rx speed Gen2 and Initial Device Rx speed Gen2 checkboxes should also be enabled.

Select Counters on the View pulldown menu and the Counters window will be displayed, as seen in Figure B.



B – SATA-II Counters Window

Ensure that the periodic update checkbox is checked and 40-bit count statistics will be automatically updated when the events occur.

Appendix F – Arbitrary Waveform Generator Accuracy

Tables F.1 outline the system and individual measurement accuracy parameters for the SATA measurements outlined in his MOI when performed using a AWG 7102 Arbitrary Waveform Generator.

Table F.2 Measurement specific performance parameters for current IW RSG measurements.

Spec number	**Measurement**	**Accuracy**	**Notes:**
RSG-01	Receiver 1.5Gb/Sec	TBD.	TBD.
RSG-02	Receiver 3.0Gb/Sec	TBD.	TBD.