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**Serial ATA
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1 Introduction

This changes within this ECN are specifically addressing typographical errors relative to state names found in SATA Revision 2.6.

2 Technical Specification Changes

2.1 Host transport idle state diagram

[**Editor's Note:** The changes marked in red (and underlined/strikethrough) will be incorporated in section 10.4.1]

HTI2: HT_ChkTyp state: This state is entered when the Link layer indicates that a FIS is being received.

When in this state, the Transport layer checks the FIS type of the incoming FIS.

Transition HTI2:1: When the incoming FIS is a register type, the Transport layer shall notify the Link layer that it has received a valid FIS, and make a transition to the HTR1: HT_RegFIS state.

Transition HTI2:2: When the incoming FIS is a Set Device Bits type, the Transport layer shall notify the Link layer that it has received a valid FIS and make a transition to the HTDB0:HT_DB_FIS state.

Transition HTI2:3: When the incoming FIS is a DMA Activate type, the Transport layer shall notify the Link layer that it has received a valid FIS, and make a transition to the HTDA1: HT_DMA_FIS state.

Transition HTI2:4: When the incoming FIS is a PIO Setup type, the Transport layer shall notify the Link layer that it has received a valid FIS, and make a transition to the HTPS1: HT_PS_FIS state.

Transition HTI2:5: When the incoming FIS is a DMA Setup type, the Transport layer shall notify the Link layer that it has received a valid FIS, and make a transition to the HTDS1: HT_DS_FIS state.

Transition HTI2:6: When the incoming FIS is a BIST Activate type, the Transport layer shall notify the Link layer that it has received a valid FIS, and make a transition to the HTRBIST1:HT_RcvBIST state.

Transition HTI2:7: When the incoming FIS is a Data type, and the previous FIS was not a PIO Setup type, the Transport layer shall notify the Link layer that it has received a valid FIS, and make a transition to the HTDA5:HT_DMAITrans state.

Transition HTI2:8: When the incoming FIS is a Data type, and the previous FIS was a PIO Setup type, the Transport layer shall notify the Link layer that it has received a valid FIS, and make a transition to the ~~HTPS6:HT_PIOITrans~~~~HTPS5:HT_PIOITrans~~1 state.

Transition HTI2:9: When the received FIS is of an unrecognized, or unsupported type, the Transport layer shall notify the Link layer that it has received an unrecognized FIS, and make a transition to the HTI1: HT_HostIdle state.

Transition HTI2:10: When the Transport layer receives notification from the Link layer of an illegal state transition, the Transport layer shall make a transition to the HTI1: HT_HostIdle state.

2.2 Host Transport decomposes a DMA Activate FIS diagram

[Editor's Note: The changes marked in red (and underlined/strikethrough) will be incorporated in section 10.4.8]

HTDA5: HT_DMAITrans state: This state is entered when the Transport layer has determined that the DMA transfer being activated is from device to host.

When in this state, the Transport layer shall activate the DMA controller if the DMA controller is initialized. A data frame is received from the device and a received data Dword shall be placed in the data FIFO.

When in this state, the Transport layer shall wait until the Link layer has begun to receive the DMA data frame and data is available to be read by the host.

Transition HTDA5:1: When the transfer is not complete, the Transport layer shall transition to the HTDA5: HT_DMAITrans state. This includes the condition where the host DMA engine has not yet been programmed and the transfer is therefore held up until the DMA engine is prepared to transfer the received data to the destination memory locations.

Transition HTDA5:2: When the SRST bit is asserted by the host writing the Device Control register, or a device reset command has been written to an ATAPI device, the Link layer shall be informed to send SYNC_P, and the Transport layer shall transition to the ~~HT11:HT_Idle~~HT11:HT_HostIdle state.

Transition HTDA5:3: When the requested DMA transfer is complete, the Transport layer shall transition to the HTDA4: HT_DMAEnd state.

Transition HTDA5:4: When the Transport layer receives notification from the Link layer of an illegal state transition, the Transport layer shall make a transition to the HT11: HT_HostIdle state.

2.3 Host Transport decomposes a PIO Setup FIS state diagram

[Editor's Note: The changes marked in red (and underlined/strikethrough) will be incorporated in section 10.4.9]

HTPS6: HT_PIOITrans2 state: This state is entered when PIO data is available in the PIO FIFO to be read by the host and the initial shadow register content has been set.

When in this state, the Transport layer shall wait for the Link layer to indicate that the data transfer is complete

Transition HTPS6:1: When the transfer is not complete, the Transport layer shall transition to the HTPS6: HT_PIOITrans2 state.

Transition HTPS6:2: When the byte count for this DRQ data block is reached, the Transport layer shall transition to the ~~HTPS5:HT_PIOEnd~~HTPS4:HT_PIOEnd state.

Transition HTPS6:3: When notified by the Link layer that the DMA Abort primitive was received, the Transport layer shall transition to the ~~HTPS5:HT_PIOEnd~~HTPS4:HT_PIOEnd state.

Transition HTPS6:4: When the Transport layer receives notification from the Link layer of an illegal state transition, the Transport layer shall make a transition to the HT11:HT_HostIdle state.

Transition HTPS6:5: When the host has asserted the SRST bit by writing to the Device Control register, or the DEVICE RESET command is requested, the Transport layer shall inform the Link layer to send a SYNC Escape, and the Transport layer shall transition to the HT11: HT_HostIdle state.

2.4 Device Transport transmit DMA Setup – Device to Host FIS state diagram

[Editor's Note: The changes marked in red (and underlined/strikethrough) will be incorporated in section 10.5.6]

DTDMASTUP1: DT_DMASTUPTransStatus	Check Link and Phy transmission results and if an error occurred take appropriate action.
1. Status checked, and no error detected.	→ DT_DeviceIdle
2. Status checked, and error detected.	→ DT_DMASTUPFIS DT_DMASTUPDHFIS

~~DTDMASTUP1~~DTDMASTUP1: DT_DMASTUPTransStatus state: This state is entered when the entire FIS has been passed to the Link layer.

When in this state, the Transport layer shall wait for the Link and Phy ending status for the FIS and take appropriate error handling action if required.

Transition DTDMASTUP1:1: When the FIS status has been handled and no error detected, the Transport layer shall transition to the DTI0: DT_DeviceIdle state.

Transition DTDMASTUP1:2: When the FIS status has been handled and an error detected, the Transport layer shall report status to the Link layer and retry this transfer by transitioning to the ~~DT_DMASTUPFIS~~~~DT_DMASTUPDHFIS~~ state.