Proposed Draft

Serial ATA International Organization

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Title : f_{baud}/10 Jitter Parameter Removal

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Document History

Version	Date	Comments
0	5 March 2007	Initial release.
1	6 March 2007	Strike out typo fixed

1 Introduction

For the SATA Gen2i and Gen2m electrical specifications, the jitter related compliance requirements (TX Jitter and RX Tolerance Lab-Sourced Signal requirements) presently have two parameters that both need to be met to achieve compliance. They are referred to as the $f_{baud}/10$ and $f_{baud}/500$ parameters. These names represent the closed loop bandwidth of the Type 2 PLLs that defines the frequency components that are to be considered as jitter. In the case of Gen2 they equate to 300 MHz and 6 MHz respectively. This erratum affects only the $f_{baud}/10$ parameter.

Gen2 jitter is defined in the SATA spec as the variation of the time difference between the Data Edge and a Reference Clock Edge generated by a hardware or software Type 2 PLL processing that data. All jitter measurements methods shall have the same characteristics as this reference system. The $f_{baud}/10$ jitter parameter requires a PLL with a Closed Loop Bandwidth of 300 MHz processing data at 3.0 Gb/s (f_{baud}). Due to the naturally occurring time delays in the arrivial of the data edges, a quality PLL with predictable characteristics is impractical to implement, when the closed loop bandwidth is only 1/10 of the data rate. 8b10b encoded data has run lengths up to 5 UI which in that case, the bandwidth, as specified, is at the Nyquist frequency of the data rate . By it's nature, the PLL is a sampled data system with the sampling rate set by the rate of the available data transitions. It is not possible to implement a PLL to meet these requirements.

Since the fbaud/10 jitter parameter requires a PLL that is impossible or impractical at best to implement, this measurement is not possible as defined in the specification. Since this compliance requirement parameter is impossible to measure, it has no purpose or value. With no value, it is being removed.

2 Technical Specification Changes

2.1 Physical Layer Requirements Tables

[**Editor's Note:** The changes marked in red (and underlined/strikethrough) will be incorporated in section 7.2.1]

Table 29 – Transmitted Signal Requirements

Parameter	Units	Limit	Electrical Specification						Detail Cross-Ref Section	Meas. Cross-Ref Section
			Gen1i	Gen1m	Gen1x	Gen2i	Gen2m	Gen2x		
~~TJ at Connector, Clk-Data, f_{BAUD}/10~~	~~UI~~	~~Max~~	~~-~~			~~0.30~~		-	7.2.2.3.12 7.3	7.4.7
~~DJ at Connector, Clk-Data, f_{BAUD}/10~~	~~UI~~	~~Max~~	~~-~~			~~0.17~~		-		
TJ at Connector, Clk-Data, f_{BAUD}/500	UI	Max	-			0.37		-		
DJ at Connector, Clk-Data, f_{BAUD}/500	UI	Max	-			0.19		-		
TJ after CIC, Clk-Data, f_{BAUD}/1667	UI	Max	-		0.55	-		0.55		
DJ after CIC, Clk-Data, f_{BAUD}/1667	UI	Max	-		0.35	-		0.35		

[**Editor's Note:** Remove deleted rows from the table.]

2.2 Physical Layer Requirements Tables

[**Editor's Note:** The changes marked in red (and underlined/strikethrough) will be incorporated in section 7.2.1]

Table 31 – Lab-Sourced Signal (for Receiver Tolerance Testing)

Parameter	Units	Limit	Electrical Specification						Detail Cross-Ref Section	Meas. Cross-Ref Section
			Gen1i	Gen1m	Gen1x	Gen2i	Gen2m	Gen2x		
~~TJ at Connector, Clk-Data, f_{BAUD}/10~~	~~UI~~	~~Max~~	~~-~~			~~0.46~~		-	7.2.2.6.8 7.3	7.4.7 7.4.9
~~DJ at Connector, Clk-Data, f_{BAUD}/10~~	~~UI~~	~~Max~~	~~-~~			~~0.35~~		-		
TJ at Connector, Clk-Data, f_{BAUD}/500	UI	Max	-			0.60		-		
DJ at Connector, Clk-Data, f_{BAUD}/500	UI	Max	-			0.42		-		
TJ at Connector, Clk-Data, f_{BAUD}/1667	UI	Max	-		0.65	-		0.65		
DJ at Connector, Clk-Data, f_{BAUD}/1667	UI	Max	-		0.35	-		0.35		

[**Editor's Note:** Remove deleted rows from the table.]

2.3 Clock-Data Receiver Jitter Tolerance (Gen2i, Gen1x, Gen2x)

[**Editor's Note:** The changes marked in red (and underlined/strikethrough) will be incorporated in section 7.2.2.6.8]

7.2.2.6.8 Clock-Data Receiver Jitter Tolerance (Gen2i, Gen1x, Gen2x)

Jitter tolerance is the ability of the receiver to recover data in the presence of jitter. The minimum amount of jitter that a receiver shall be able to operate is the jitter tolerance specification provided in Table 31 and section 7.4.9 describes the measurement. ~~Receivers shall tolerate at least the jitter for both corner frequencies listed.~~

2.4 Reference Clock Definition

[**Editor's Note:** The changes marked in red (and underlined/strikethrough) will be incorporated in section 7.3.2]

7.3.2 Reference Clock Definition

The Reference Clock is defined as that clock recovered from a Serial ATA data stream. The Reference Clock provides the distinction between Spread Spectrum Clocking (SSC) and jitter. The Reference Clock tracks SSC and wander, but not jitter. In addition, it provides a definition for determining the SSC profile.

Reference Clock extraction is performed using either hardware or software PLLs. Two Reference Clock PLLs are defined as type 2 PLL with a -3 dB corner frequency $f_{c3dB} = f_{BAUD}/N$ (N = ~~10 (Gen2i),~~ 500 (Gen2i, Gen2m), 1667 (Gen1x, Gen2x)) given a transition density of 1.0 (corresponding to a 1010101010 clock-like pattern) and damping factor ξ = 0.707 min to 1.00 max. This frequency dependent shape assumes that the Clock and Data Recovery circuit (CDR) may track low frequency modulation and SSC. This clock extraction eliminates the spread spectrum frequency modulation from the jitter measurements.

At least two receiver architectures are possible within the SATA specification – over-sampling and tracking. Over-sampling architectures may respond to data period changes quickly while tracking architectures tend to have a slower response time.

~~Several~~ Two corner frequencies are provided in the jitter budget (~~$f_{c3dB} = f_{BAUD}/10$ (Gen2i, Gen2m),~~ $f_{c3dB} = f_{BAUD}/500$ (Gen2i, Gen2m), and $f_{c3dB} = f_{BAUD}/1667$ (Gen1x, Gen2x)). ~~For Gen2i and Gen2m, transmitters and receivers shall meet both $f_{BAUD}/10$ and $f_{BAUD}/500$ specifications.~~