Proposed Draft

Serial ATA International Organization

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Title : f_{baud}/500 Jitter Parameter Clarification

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Document History

Version	Date	Comments
0	3 April 2007	Initial release.
1	4 April 2007	Incorporate some suggestions after first review by the committee
	18 April 2007	Phy WG Approval

1 Introduction

1.1 Problem Statement

The present Jitter Definition does not provide for an unique interpretation resulting in a lack of capability of performing repeatable and reproducible jitter measurements.

More detail is provided in the paragraphs that follow:

For the SATA Gen2i and Gen2m electrical specifications, the jitter related compliance requirements (TX Jitter and RX Tolerance Lab-Sourced Signal requirements) are controlled by the fbaud/500 TJ and DJ Electrical Specification parameters. Gen2 jitter is defined in the SATA spec as the variation of the time difference between the Data Edge and a Reference Clock Edge generated by a hardware or software Type 2 PLL processing that data. All jitter measurement methods shall have the same characteristics as this reference system.

The present definition for the Reference Clock, that defines what is considered jitter and what is considered to be allowable timing variations, has two problems in the present specification:

1) The Type 2 PLL characteristics, which are provided in the specification section 7.3.2, are the CLTF (Closed Loop Transfer Function) – 3dB bandwidth and a damping factor. When the time difference of the Reference Clock edge and the associated data edge is performed, this does not provide a unique definition for what is defined as jitter. The resulting JTF (Jitter Transfer Function) varies greatly depending on how the PLL is designed. Additionally, using a damping factor, in the context of a PLL, does not directly control the peaking in the CLTF or the JTF, due to the intentional compensation dynamics present in a PLL. One erroneous assumption initially made, was that the PLL could be specified in the same manner as a second order low pass filter.

2) Section 7.4.7 is not only unclear on how the resulting JTF relates to the PLL CLTF, but is it misleading in the fact that one might assume that the -3dB BW of the JTF (referenced as the H_H High Pass Function) is the same as the -3dB BW of the PLL CLTF (referenced as the H_L Low Pass Function). This leads to two possible interpretations of the Jitter Definition: 1) If correctly interpreted, the resulting JTF BW would be much lower (typically about 1/3) than the PLL BW. This ratio is not unique so this still allows for wide variance of the Jitter Definition characteristics. 2) If incorrectly interpreted, one could assume that the resulting JTF, after taking the time difference between the PLL output (Reference Clock) and the Data, could be replaced with a second order High Pass Function when defining or measuring jitter. This can result in a variation of 3:1 or more in analysis bandwidths for measuring jitter.

The combination of these two problems in the specification result in a large variation of what is considered jitter and what is considered as allowable timing variations. The danger here is that communication system elements that are individually controlled by the specification, and may be tested to multiple interpretations of the Jitter Definition, and therefore are not well controlled as is desired for interoperability.

1.2 Background Information

Written evidence and background information supporting the comments above is attached:
[SATA-IO PHY WG Gen2i jitter P3 0107.pdf]

1.3 Solution

The solution to this is to directly specify the requirements for the JTF (the resulting H_H after the time difference function). Since the transformation from the PLL CLTF to the resulting JTF is not unique, this conversion has been performed using typical PLL characteristics attempting to maintain the present specification requirement. By specifying the JTF, this provides for a clear Jitter Definition that prevents multiple interpretations, and closer represents what jitter the actual receiver will be subjected to.

2 Technical Specification Changes

[**Editor's Note:** The changes below assume that ECN 006 has been incorporated in the specification. This prevents confusion on what items are changed in this ECN versus ECN 006, since some of the sections changing are common to both ECNs. Additionally, all active cross references have been frozen, or converted to text, to keep the original paragraph, table, and figure designations for direct comparison. These will need to be updated when updating the master document.]

2.1 Physical Layer Requirements Tables

[**Editor's Note:** The changes marked in red (and underlined/strikethrough) will be incorporated in section 7.2.1]

Table 29 – Transmitted Signal Requirements

Parameter	Units	Limit	Electrical Specification							
			Gen1i	Gen1m	Gen1x	Gen2i	Gen2m	Gen2x		
TJ at Connector, Clk-Data, $f_{BAUD}/500$ JTF Defined	UI	Max	-			0.37		-	7.2.2.3.12 7.3	7.4.7
DJ at Connector, Clk-Data, $f_{BAUD}/500$ JTF Defined	UI	Max	-			0.19		-		
TJ after CIC, Clk-Data, $f_{BAUD}/1667$	UI	Max	-		0.55	-		0.55		
DJ after CIC, Clk-Data, $f_{BAUD}/1667$	UI	Max	-		0.35	-		0.35		

2.2 Physical Layer Requirements Tables

[**Editor's Note:** The changes marked in red (and underlined/strikethrough) will be incorporated in section 7.2.1]

Table 31 – Lab-Sourced Signal (for Receiver Tolerance Testing)

Parameter	Units	Limit	Electrical Specification							
			Gen1i	Gen1m	Gen1x	Gen2i	Gen2m	Gen2x		
TJ at Connector, Clk-Data, f_{BAUD}/500 JTF Defined	UI	Max	-			0.60		-	7.2.2.6.8 7.3	7.4.7 7.4.9
DJ at Connector, Clk-Data, f_{BAUD}/500 JTF Defined	UI	Max	-			0.42		-		
TJ at Connector, Clk-Data, f_{BAUD}/1667	UI	Max	-		0.65	-		0.65		
DJ at Connector, Clk-Data, f_{BAUD}/1667	UI	Max	-		0.35	-		0.35		

2.3 Clock-Data Receiver Jitter Tolerance (Gen2i, Gen1x, Gen2x)

[**Editor's Note:** The changes marked in red (and underlined/strikethrough) will be incorporated in section 7.2.2.6.8]

7.2.2.6.8 Clock-Data Receiver Jitter Tolerance (Gen2i, Gen2m, Gen1x, Gen2x)

Jitter tolerance is the ability of the receiver to recover data in the presence of jitter. The minimum amount of jitter that a receiver shall be able to operate is the jitter tolerance specification provided in Table 31 and section 7.4.9 describes the measurement.

2.4 Definition

[**Editor's Note:** The changes marked in red (and underlined/strikethrough) will be incorporated in section 7.3.1]

7.3.1 Definition

For Gen1x, Gen2i, Gen2m, and Gen2x, jitter is defined as the difference in time between a data transition and the associated Reference Clock event. The jitter at the receiver is the result of the

aggregate jitter in the transmission path. First, jitter is generated during clocking of the data in the transmitter. Then, each element in the channel between the transmitter and the receiver influences the jitter. Finally, the receiver shall be able to recover the data despite the jitter, otherwise errors occur. The receiver jitter tolerance shall be greater than the transmitter's generated jitter and the expected jitter accumulation through the channel.

Jitter budgets are dependent on the desired bit error rate (BER). SATA assumes a BER target of less than 10^{-12}. For Gen1x, Gen2i, Gen2m, and Gen2x, jitter levels are defined as Reference Clock to data. The Reference Clock is extracted from a serial data stream using either a PLL (hardware) or a clock recovery algorithm (software). For Gen1i, jitter levels are defined as data to data.

The Reference Clock to data jitter methodology allows for jitter measurements to be made on a device or host using a Spread Spectrum Clock or a non-spreading clock.

2.5 Clock-to-Data Transmit Jitter (Gen1x, Gen2i, Gen2m, Gen2x)

[**Editor's Note:** The changes marked in red (and underlined/strikethrough) will be incorporated in section 7.2.2.3.12]

7.2.2.3.12 Clock-to-Data Transmit Jitter (Gen1x, Gen2i, Gen2m, Gen2x)

Gen1x, Gen2i, Gen2m, and Gen2x use a Clock-to-Data jitter requirement. Transmitters shall meet the jitter specifications for the ~~tracking PLL frequency corners~~ Reference Clock characteristics specified in each case. Table 29 shows the maximum amount of jitter that a transmitter may generate and still be SATA compliant and section 7.4.7 describes the measurement. Since this specification places the compliance point at the connector, any jitter generated at the package connection, on the printed circuit board, and at the board connector shall be included in the measurement.

2.6 Reference Clock Definition

[**Editor's Note:** The changes marked in red (and underlined/strikethrough) will be incorporated in section 7.3.2]

7.3.2 Reference Clock Definition

~~The Reference Clock is defined as that clock recovered from a Serial ATA data stream. The Reference Clock provides the distinction between Spread Spectrum Clocking (SSC) and jitter. The Reference Clock tracks SSC and wander, but not jitter. In addition, it provides a definition for determining the SSC profile.~~

~~Reference Clock extraction is performed using either hardware or software PLLs. Two Reference Clock PLLs are defined as type 2 PLL with a -3 dB corner frequency $f_{c3dB} = f_{BAUD}/N$ (N = 500 (Gen2i, Gen2m), 1667 (Gen1x, Gen2x)) given a transition density of 1.0 (corresponding to a 1010101010 clock like pattern) and damping factor $\xi = 0.707$ min to 1.00 max. This frequency dependent shape assumes that the Clock and Data Recovery circuit (CDR) may track low frequency modulation and SSC. This clock extraction eliminates the spread spectrum frequency modulation from the jitter measurements.~~

~~At least two receiver architectures are possible within the SATA specification – over-sampling and tracking. Over-sampling architectures may respond to data period changes quickly while tracking architectures tend to have a slower response time.~~

~~Two corner frequencies are provided in the jitter budget ($f_{c3dB} = f_{BAUD}/500$ (Gen2i, Gen2m), and $f_{c3dB} = f_{BAUD}/1667$ (Gen1x, Gen2x)).~~

The Reference Clock is defined as that clock recovered from a Serial ATA data stream. The Reference Clock provides the distinction between Spread Spectrum Clocking (SSC) and jitter. The Reference Clock tracks SSC and wander, but not jitter. In addition, it provides a definition for determining the SSC profile. Reference Clock extraction is performed using either hardware or software PLLs.

7.3.2.1 Gen2i and Gen2m Normative Requirements

For Gen2i and Gen2m, the Reference Clock characteristics are controlled by the resulting JTF (Jitter Transfer Function) characteristics obtained by taking the time difference between the Type 2 PLL output (the Reference Clock) and the data stream sourced to the PLL. The PLL CLTF -3 dB corner frequency, and other adjustable CLTF parameters such a peaking, are determined by the value required to meet the requirements of the JTF. (See section 7.4.7 for JTF information)

The JTF for Gen2i and Gen2m shall have the following characteristics for an encoded D24.3 pattern (1100110011 0011001100). This is the MFTP which is a test pattern that has clock-like characteristics and a transition density of 0.5.

1) The -3 dB corner frequency of the JTF shall be 2.1 MHz +/- 1 MHz.
2) The magnitude peaking of the JTF shall be 3.5 dB maximum.
3) The attenuation at 30 KHz +/- 1% shall be 72 dB +/- 3 dB.

The JTF -3dB corner frequency and the magnitude peaking requirements shall be measured with sinusoidal PJ applied, with a peak-to-peak amplitude of 0.3 UI +/- 10%. The attenuation at 30 KHz shall be measured with sinusoidal phase (time) modulation applied, with a peak-to-peak amplitude of 20.8 ns +/- 10%.

7.3.2.2 Gen2i and Gen2m Informative Comments

Typically a CLTF -3 dB corner frequency of f_{BAUD} /500 could provide a JTF with characteristics close to the requirements, but due to differences in Type 2 PLL designs, the actual CLTF settings required to meet the required JTF can vary widely.

It is desired that the phase response of the JTF of a JMD (Reported Jitter / Applied Jitter) be that of the JTF of the time difference of the output of a Type 2 PLL to the Data stream applied to the PLL. This is the reference design. In the presence of multiple jitter component frequencies, the relative phase at these frequencies determines how they are combined to construct the final reported jitter value. In the case of discrepancies between the reported jitter levels, between JMDs with the same JFT magnitude response, the JMD with the JTF phase characteristics closest to that of the reference design, is to be considered correct. The JTF phase response of a JMD is important, but it is not always possible to determine this without proprietary information concerning the JMD processing methods, and it is not externally observable in some classes of JMDs.

The JTF of the time difference of the output of a Type 2 PLL to the Data stream applied to the PLL, or the reference design, is defined with a pattern that has a transition density of 0.5. Since this Type 2 PLL contains a sampled data mode phase detector, with a gain that varies proportionally with transition density, the JTF -3 dB corner frequency will change with the transition density of the applied pattern. For a well designed PLL, with significant phase margin in the open loop response, the JTF -3 dB corner frequency, with shift proportionally with the change of pattern transition density. For example, the 2.1 MHz JTF -3dB corner frequency, set with a pattern with a transition density of 0.5, will shift to 4.2 MHz when a pattern with a transition density of 1.0, such as the D10.2 pattern, is applied. A proportional decrease of the JTF -3dB corner frequency will also be observed for a decrease in pattern transition density compared to a 0.5 transition density. This is the expected JMD response to changes in pattern transition density as the reference design would exhibit. If a JMD shifts the JTF -3dB corner frequency in a manner that does not match this characteristic, or does not shift at all, measurements of jitter with patterns with transition densities significantly different than 0.5 may lead to discrepancies in reported jitter levels. In the case of reported jitter discrepancies between JMDs, the JMD with the shift of the -3dB corner frequency, closest to the proportional characteristic of the reference design, it to be considered correct. This characteristic may be measured using the conditions defined above for measuring the -3dB corner frequency, using multiple patterns with different transition densities.

7.3.2.3 Gen1x and Gen2x Normative Requirements

For Gen1x and Gen2x, the Reference Clock PLL is defined as type 2 PLL with a -3 dB corner frequency $f_{c3dB} = f_{BAUD}$ /1667 given a transition density of 1.0 (corresponding to a 1010101010 clock-like pattern) and damping factor ξ = 0.707 min to 1.00 max.

2.7 Jitter Measurements

[**Editor's Note:** The changes marked in red (and underlined/strikethrough) will be incorporated in section 7.4.7]

7.4.7 Jitter Measurements

This section does not apply to Gen1i jitter measurements.

Jitter is the difference in time between a data transition and the associated Reference Clock event, taken as the ideal point for a transition. The causes of jitter are categorized into random sources (RJ) and deterministic sources (DJ). Although the total jitter (TJ) is the convolution of the probability density functions for all the independent jitter sources, this specification defines the random jitter as Gaussian and the total jitter as the deterministic jitter plus 14 times the random jitter. The TJ specifications of Table 29 and Table 31 were chosen at a targeted BER of 10^{-12}.

The BERT scan method described in section 7.4.7.1 is the only method that measures the actual TJ and is used as the reference for all TJ estimation methods. The method for estimating TJ is unique to each measurement instrument.

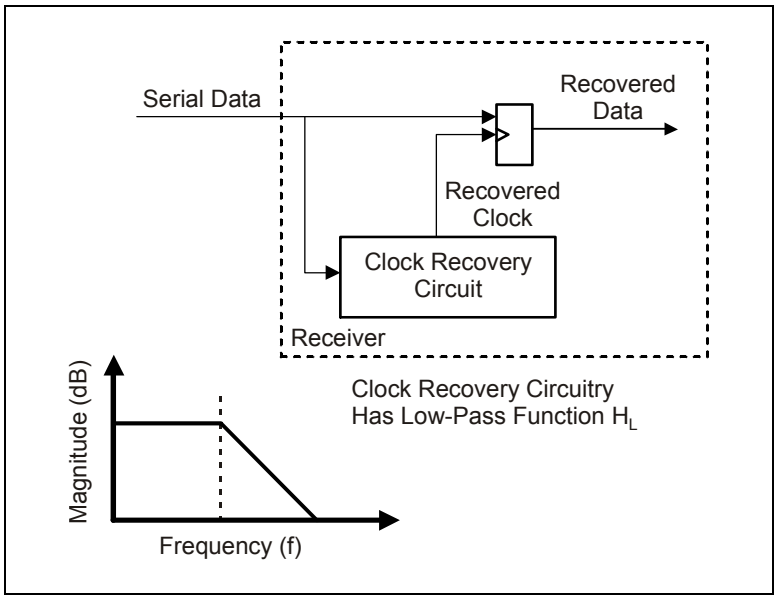


Figure 137 - Receiver Model for Jitter

The jitter measurement methodology is defined as a clock to data jitter measurement. Figure 137 shows a block diagram of a deserializer input. The serial data is split into two paths. One path feeds clock recovery circuitry, which becomes the reference signal used to latch the data bits of the serial data stream. This clock recovery circuitry has a low pass transfer function H_L. This low pass function is the CLTF of the PLL or clock recovery circuit. The jitter seen by the receiver is the time difference of the recovered clock edge to the data edge position. This time difference function is shown in Figure 138. The resulting jitter seen by the receiver has a high pass function H_H shown in Figure 139. This high pass function is the JTF (Jitter Transfer Function) of the system. This defines the measurement function required by all jitter measurement methodologies. ~~The corner frequency f_c is given is section 7.3.2.~~ The required characteristics for the JTF (Gen2i, Gen2m) and the CLTF corner frequency f_c (Gen1x, Gen2x) are provided in section 7.3.2. In the case of a JMD, the JTF may be simply viewed as the ratio of the reported jitter to the applied jitter, for a sinusoidal PJ input.

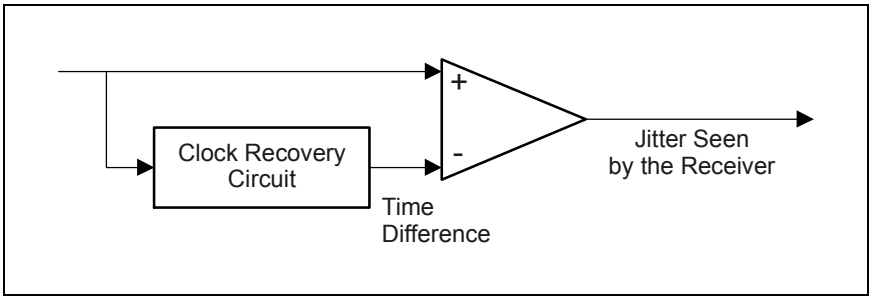
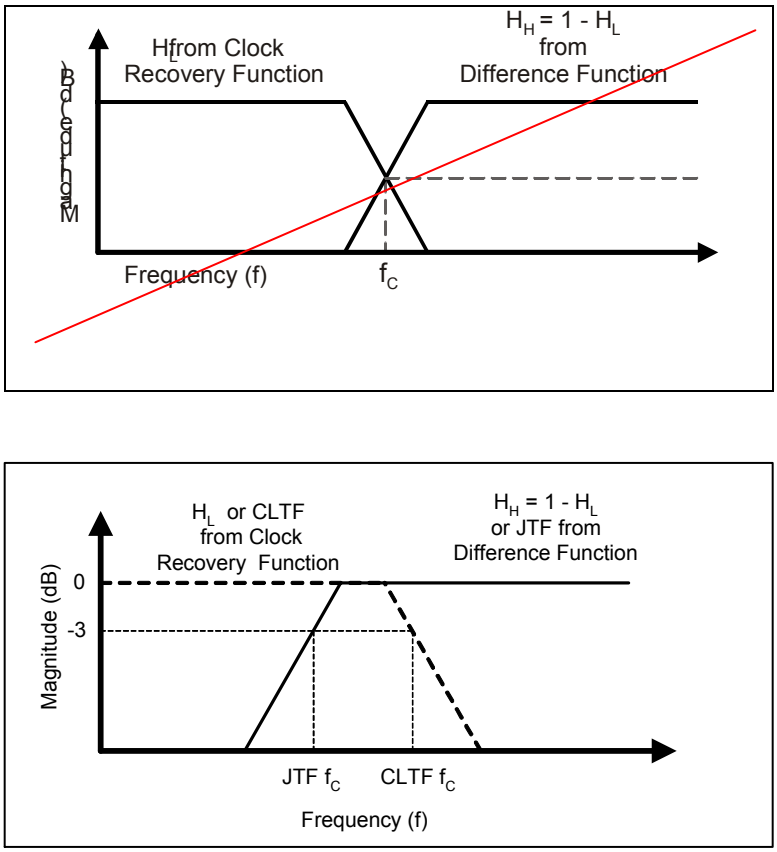


Figure 138 – Jitter at Receiver



Editor's Note: Picture Red = Addition

Figure 139 – Jitter at Receiver, High Pass Function

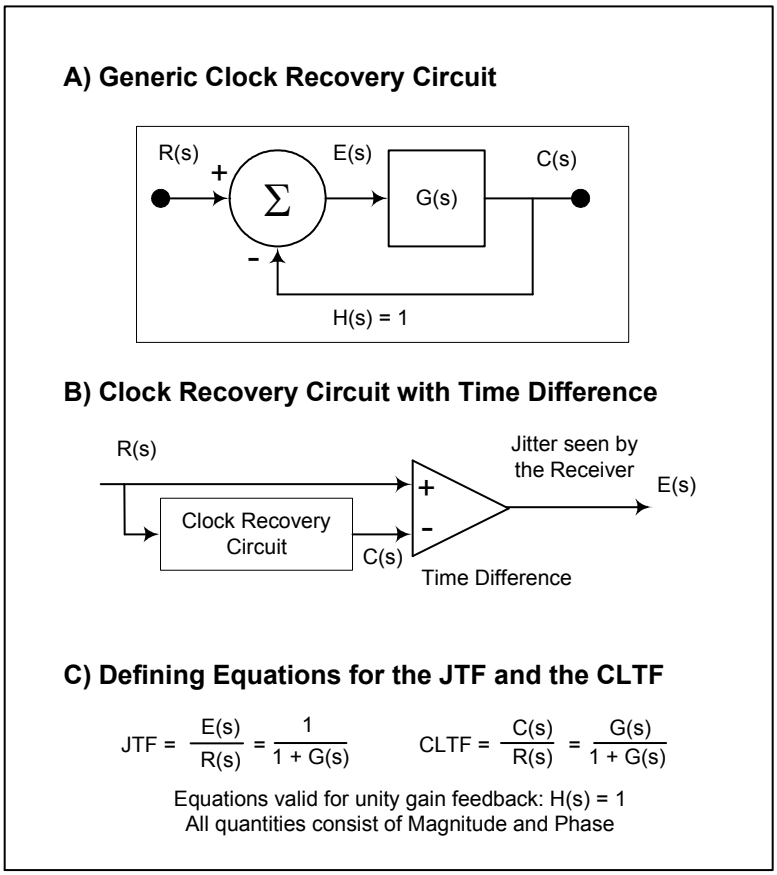
This ~~response function~~ JTF (H_H in Figure 139) mimics the receiver's ability to track lower frequency jitter components (wander, SSC) and not include them in the jitter measurement. This measurement methodology enables any measurement instrument to accurately measure the jitter seen by a receiver and produce measurements that correlate from measurement instrument to measurement instrument.

It should be noted that the corner frequency of the JTF is not the corner frequency of the clock recovery CLTF. This may not be obvious until one considers the phase shift caused by the clock recovery circuit. In general the vector sum $H_L(f) + H_H(f) = 1$. All quantities consist of changing magnitude and phase as a function of frequency. This accounts for differences in corner frequencies and peaking in the two frequency dependant functions.

Figure 140 shows more detail into how the JTF and CLTF relate to the jitter that would be applied to a receiver. The subfigure A) represents a generic control system block diagram for a feedback loop based clock recovery system. Subfigure B) translates the same complex variables to the combined system of the clock recovery circuit and the time difference function. It can be seen that E(s) is the jitter seen by the receiver, as well as being the error signal in the clock recovery circuit. Subfigure C) provides the defining equations for the clock recovery circuit CLTF and the combined system JTF function.

Both the CLTF and the JTF are uniquely defined by the open loop transfer function G(s). Defining a CLTF does not uniquely define the G(s) and subsequently the JTF due to the level of cancellation of G(s) in the numerator and denominator of the CLTF especially when G(s) is much greater than 1, which is necessary for jitter tracking by the clock recovery circuit. This is the

rational for Gen2i and Gen2m directly specifying the JTF rather than the CLTF of the clock recovery circuit. When the JTF of a JMD meets the requirements specified, the JMD reported jitter levels will closer represent the jitter applied to the receiver in this reference design.



Editor's Note: Picture Red = Addition

Figure 140 – JTF and CLTF Definition

2.8 Definitions and abbreviations

[**Editor's Note:** The changes marked in red (and underlined/strikethrough) will be incorporated in section 4.1]

4.1.12 ClickConnect

An optional positive latch solution for internal single lane interconnects (see section 6.1.4).

4.1.xx CLTF (Closed Loop Transfer Function)

For a feedback system, the CLTF is the ratio of the magnitude and phase of the output variable to the magnitude and phase of the input variable, as a function of frequency for sinusoidal excitation. This term is used in the Reference Clock sections of this specification.

4.1.13 code violation

A code violation is an error that occurs in the reception process as a result of (1) a running disparity violation or (2) an encoded character that does not translate to a valid data or control character or (3) an encoded character that translates to a control character other than K28.5 or

K28.3 in byte 0 of a Dword or (4) an encoded character that translates to any control character (valid or invalid) in bytes 1-3 of a Dword.

4.1.62 JMD (jitter measuring device)

A device used to measure jitter. Examples are a bit error rate tester (BERT), a timing interval analyzer (TIA), a single shot capture oscilloscope and processing software, or a HBWS.

4.1.yy JTF (Jitter Transfer Function)

In general terms, the JTF of a system is the ratio of the jitter magnitude and phase of the output variable to the jitter magnitude and phase of the input variable, as a function of frequency for sinusoidal jitter excitation. In the case of a jitter definition, this defines the magnitude of the jitter, as a function of frequency allowed to be generated by the transmitter or tolerated by the receiver. In the case of a JMD, this defines the ratio of the reported jitter to the applied jitter, as a function of frequency for sinusoidal excitation.

4.1.63 junk

An 8b/10b encoded data Dword sent between $CONT_P$ and another primitive transmitted on the link. All junk Dwords shall be ignored by the receiver.