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**Serial ATA
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Document History

Version	Date	Comments
0	<Date>	Initial release as technical proposal.
1	03/19/2007	Re-documented to disallow invalid data, rather than utilizing an invalidated CRC.
2	04/04/2007	Re-documented to highlight clarifications to the existing definition regarding data validity per 4/2 Digital meeting consensus.
3	04/09/2007	Re-documented as ECN with clarifications clarifying that hosts are NOT to utilize data for a command until command completion is received from the device.
4	04/10/2007	Integrated proposed Data FIS reception changes to require reception error reporting in command completion/status.
5	04/16/2007	Clarified "command completion status".

1 Introduction

The current specification does not require devices to provide an invalid CRC to the host when the device knowingly provides corrupt data. In cases where a device error occurs in the middle of the transfer, there are implementations which will add padded data into the stream to the host before reporting the error. Due to the nature of various device behaviors in these data transfer error cases, the host may not assume the validity or state of data received until final ending status is received for the command in question.

This errata intends to clarify that the host may not rely upon the state of data transferred by the device until final status has been received for the complete transfer (command). The CRC within an individual data FIS may not completely identify whether the data within that FIS is valid for the transfer in process. In cases where large transfer sizes are associated with individual commands, it may be interesting for a host to design optimizations where data as its received is relied upon or used prior to transfer completion of the remaining data for the associated command. These types of optimizations are not advised as the true status of the data transferred may not be completely understood until ending status is received from the device. If an error has occurred the device must report the type of error that occurred and also return the appropriate data location of the error (protocol specific) within the ending status of the command.

2 Technical Specification Changes

2.1 Data FIS changes

2.1.1 Reception

[Editor's Note: The changes marked in red (and underlined/strikethrough) will be incorporated in section 10.3.11.3]

Neither the host nor device is expected to buffer an entire Data FIS in order to check the CRC of the FIS before processing the data. Incorrect data reception for a Data FIS ~~should~~shall be reflected in the overall command completion status.

2.2 Protocol changes

2.2.1 Host Transport decomposes a DMA Activate FIS diagram

[Editor's Note: The changes marked in red (and underlined/strikethrough) will be incorporated in section 10.4.8]

HTDA4: HT_DMAEnd state: This state is entered when the DMA data transfer is complete.

When in this state, the Transport layer shall ensure that the activities of the DMA controller have completed.

Transition HTDA4:1: When the DMA controller has completed its activities, whether it has exhausted its transfer count or has been deactivated as a result of reaching the 2048 Dword data payload limit, the Transport layer shall transition to the HTI1: HT_HostIdle state. This transition occurs if no error is detected.

NOTE : The host should not assume received data is valid (even with a valid CRC receipt for the FIS) until command completion status is returned by the device.

Transition HTDA4:2: When an error is detected, status shall be reported to the Link and Application layers. The Transport layer shall transition to the HTI1:HT_HostIdle state.

Transition HTDA4:3: When notified by the Link layer that a DMA Abort primitive was received, the transfer shall be truncated, and the Link layer notified to append CRC and end the frame. When it is determined that the transfer is completed with no error, the Transport layer shall make a transition to the HTI1:HT_HostIdle state.

Transition HTDA4:4: When notified by the Link layer that a DMA Abort primitive was received, the transfer shall be truncated, and the Link layer notified to append CRC and end the frame. When it is determined that the transfer is completed with an error, the Transport layer shall report status to the Application layer and make a transition to the HTI1:HT_HostIdle state.

2.2.2 Host Transport decomposes a PIO Setup FIS state diagram

[Editor's Note: The changes marked in red (and underlined/strikethrough) will be incorporated in section 10.4.9]

HTPS4: HT_PIOEnd state: This state is entered when the PIO data transfer is complete. When in this state, the Transport layer shall place the ending register content from the received PIO request FIS into the shadow registers.

Transition HTPS4:1: When the ending register content for the PIO request FIS has been placed into the shadow registers and there were no errors detected with the transfer, the Transport layer shall transition to the HTI1: HT_HostIdle state.

NOTE : The host should not assume received data is valid (even with a valid CRC receipt for the FIS) until command completion status is returned by the device.

Transition HTPS4:2: When the ending register content from the previous PIO Setup FIS has been placed into the shadow registers, the Transport layer shall transition to the HTI1:HT_HostIdle state. For data in transfers, the Transport layer shall notify the Link layer of any error encountered during the transfer, and the error shall be reflected in the end of frame handshake. If the transfer was not the final transfer for the PIO data in command, the device shall reflect the error status by transmitting an appropriate Register FIS to the host. If the transfer was the final transfer for the associated PIO data in command, the error condition is not detectable. For data out transfers, errors detected by the device shall be reflected in the end of frame handshake. The device shall reflect the error status by transmitting an appropriate Register FIS to the host.