

**Proposed
Draft**

**Serial ATA
International Organization**

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Document History

Version	Date	Comments
0	8/10/2006	Initial release.
0.1	10/11/2006	Revised figures and added explanation of GD&T usage
0.2	4/30/2007	Re-issued and reformatted for Rev. 2.6

1 Introduction

The original SATA connector set has been found to have a tolerance overlap condition of the features which provide cable retention. These features are defined as a “bump” on the cable receptacle and a “slot” on the plug. The tolerance stack of feature size and feature location results in an overlap condition which prevents the bump from engaging with the slot.

2 Technical Specification Changes

In order to minimize impact to existing products in the market, the following changes will be made to the feature location tolerances. The proposed changes make use of Geometric Dimensioning & Tolerancing (GD&T) by utilizing Maximum Material Condition (MMC), the new tolerancing scheme allows “bonus” tolerance when features are less than the maximum allowable size.

Glossary:

GD&T = Geometric Dimensioning & Tolerancing

MMC = Maximum Material Condition

WRT = with respect to

2.1 Figure 27 – Device plug connector

Section E-E

Delete dimensions for locations of slots (7.05mm & 5.78mm)

Replace with basic dimensions from Centerline of Datum B to Centerlines of Slot

Change 7.62 dimension to basic dimension

Add Geometric Tolerance Control frame to feature size.

GD&T = True position of 0.05mm @ MMC, WRT Datum B @ MMC

2.2 Figure 30 – Cable receptacle connector interface dimensions

Front View

Delete dimension for bump location (4.71mm)

Replace with basic dimension from Centerline of Datum B to Centerline of Bump

Add Geometric Tolerance Control frame to feature size.

GD&T = True position of 0.05mm @ MMC, WRT Datum B @ MMC

2.3 Figure 32 – Host signal plug connector interface dimensions

Section B-B

Delete dimension for slot location (5.78mm)

Replace with basic dimension from Centerline of Datum B to Centerline of Slot

Add Geometric Tolerance Control frame to feature size.

GD&T = True position of 0.05mm @ MMC, WRT Datum B @ MMC

2.4 Figure 38 – Power receptacle connector interface dimensions

Front View

Delete dimensions for locations of bump (5.98mm & 7.62mm)

Replace with basic dimensions from Centerline of Datum B to Centerlines of Bump

Add Geometric Tolerance Control frame to feature size.

GD&T = True position of 0.05mm @ MMC, WRT Datum B @ MMC

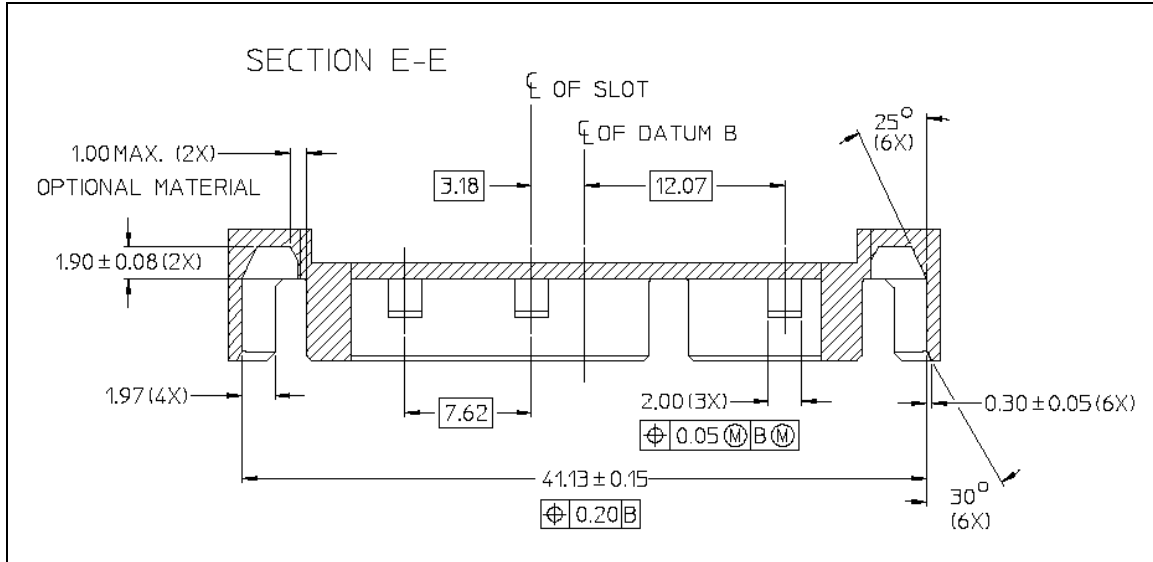


Figure 27 – Section E-E

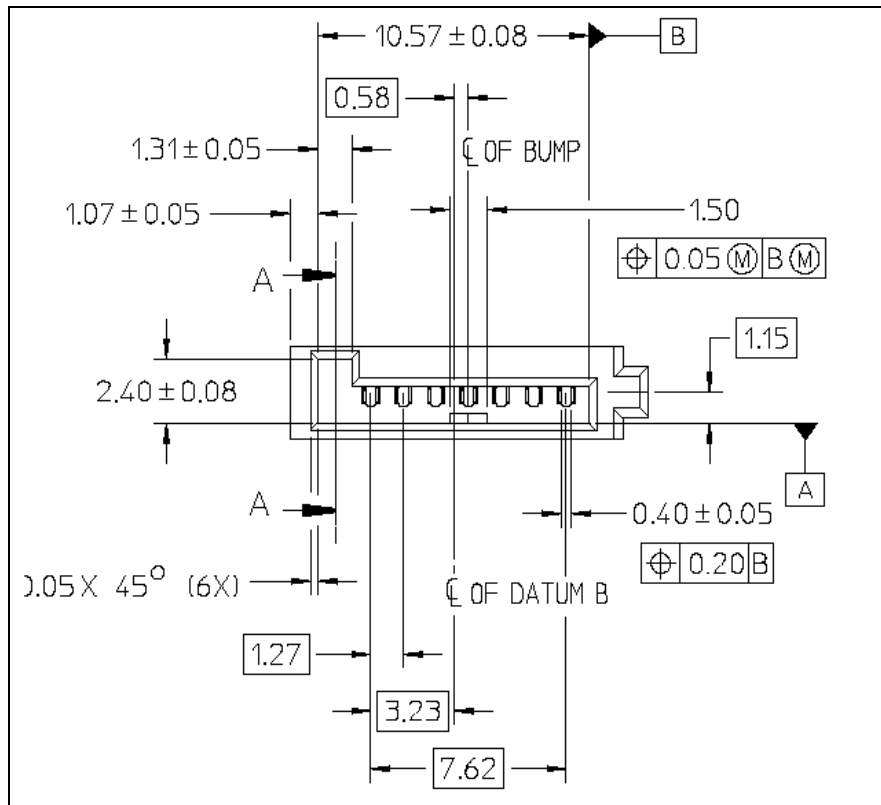


Figure 30 – Front View

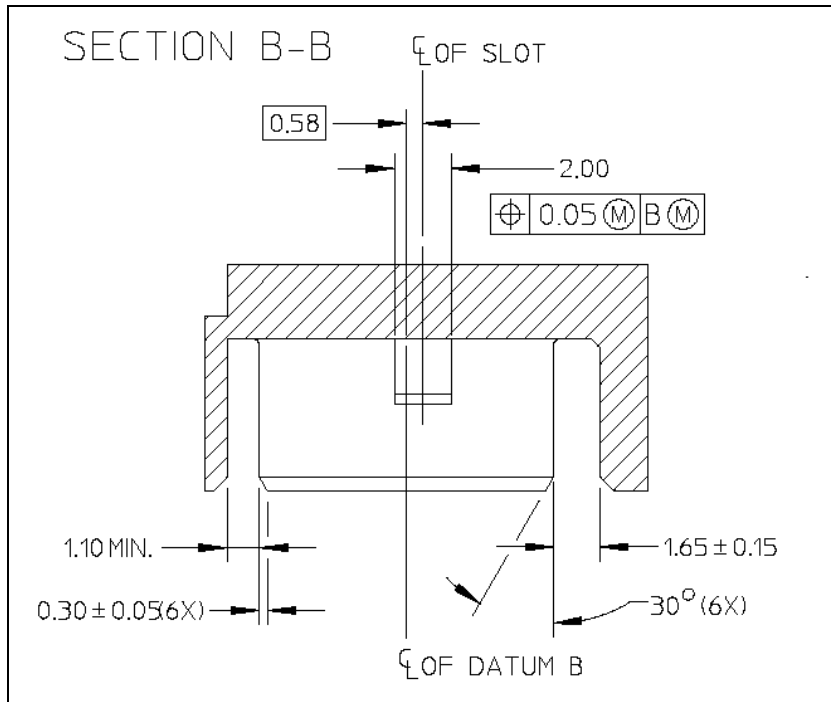


Figure 32 – Section B-B

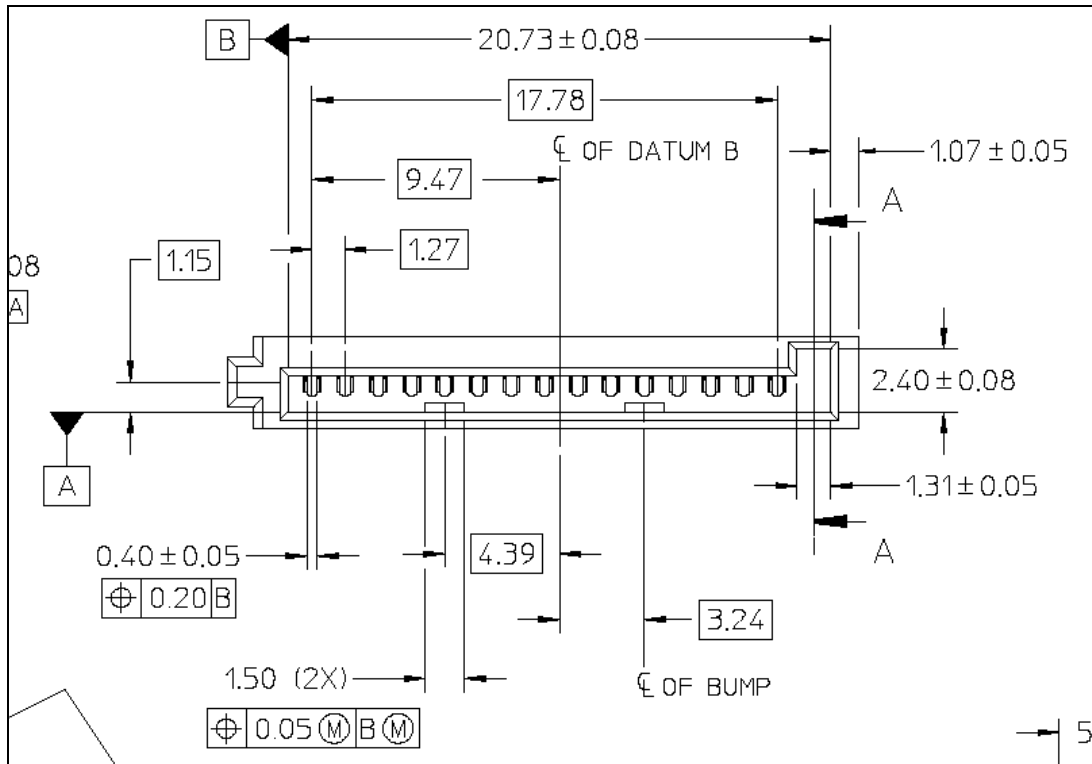


Figure 38 – Front View