Proposed Draft

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Title : PACKET State Names

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Document History

Version	Date	Comments
0	05/08/2007	Initial release.

1 Introduction

1.1 Problem Statement

Several state machines within the specification use the same acronym/numbering combinations for shorthand reference of the states. Specifically the Device Phy (sec 8.4.2) and Device Packet Protocol (sec 11.11) use the DP acronym as shorthand for the states.

1.2 Solution Summary

To eliminate any potential confusion or mis-representation of critical state machines within the specification, this errata proposes modifications to the Packet Protocol state names to differentiate them.

1.3 Background (optional)

2 Technical Specification Changes

2.1 Device Idle protocol

[**Editor's Note:** The changes marked in red (and underlined/strikethrough) will be incorporated in section 11.2, specifically states DI2 and DI7]

DI2: Check_command[1]	Check the command to determine required command protocol. If asynchronous notification is supported then NotifyPending is cleared to zero.	
1. Non-data command protocol and no native queued command outstanding.	→	DND0: Non-data
2. PIO data-in command protocol and no native queued command outstanding.	→	DPIOI0: PIO_in
3. PIO data-out command protocol and no native queued command outstanding.	→	DPIOO0: PIO_out
4. READ DMA command protocol and no native queued command outstanding.	→	DDMAI0: DMA_in
5. WRITE DMA command protocol and no native queued command outstanding.	→	DDMAO0: DMA_out
6. PACKET command protocol and no native queued command outstanding.	→	DPKT0: PACKET
7. * READ DMA QUEUED command protocol and no native queued command outstanding.	→	DDMAQI0: DMA_queued_in
8. * WRITE DMA QUEUED command protocol and no native queued command outstanding.	→	DDMAQIO: DMA_queued_out
9. EXECUTE DEVICE DIAGNOSTIC command protocol and no native queued command outstanding.	→	DEDD0: Execute_device_diag
10. DEVICE RESET command protocol.	→	DDR0: Device_reset
11. Command not implemented and no native queued command outstanding.	→	DI3: No_command
12. * SERVICE command protocol and no native queued command outstanding.	→	DI5: Service_test
13. * READ FPDMA QUEUED command protocol.	→	DFPDMAQ1: AddCommand_ ToQueue
14. * WRITE FPDMA QUEUED command protocol.	→	DFPDMAQ1: AddCommand_ ToQueue
15. * Not READ FPDMA QUEUED and not WRITE FPDMA QUEUED and not DEVICE RESET and native queued command(s) outstanding	→	DFPDMAQ12: BrokenHost_ ClearBusy
NOTE: 1. This state shows transitions for all commands. If a device does not implement any particular command, then that transition should not be processed.		

* DI7: Service_decode	Check command type to be serviced.	
1. PACKET PIO data-in.	→	DPKT4: PACKET_PIO_in
2. PACKET PIO data-out.	→	DPKT6: PACKET_PIO_out
3. PACKET DMA data-in.	→	DPKT9: PACKET_DMA_in
4. PACKET DMA data-out.	→	DPKT11: PACKET_DMA_out
5. READ DMA QUEUED.	→	DDMAQI1: Send_data
6. WRITE DMA QUEUED.	→	DDMAQO1: Send_DMA_activate

DI2: Check_command state: This state is entered when the device recognizes that the received Register FIS contains a new command. NOTE: This state shows transitions for all commands. If a device does not implement any particular command, then transition DI2:11 to state DI3:No_command shall be made.

When in this state, the device shall check the command protocol required by the received command and clears NotifyPending to zero if asynchronous notification is supported. Clearing NotifyPending to zero allows future asynchronous notification messages to be sent to the host.

Transition DI2:1: When the received command is a non-data transfer command, the device shall transition to the DND0: Non-data state.

Transition DI2:2: When the received command is a PIO data-in command, the device shall transition to the DPIOI0: PIO_in state.

Transition DI2:3: When the received command is a PIO data-out command, the device shall transition to the DPIOO0: PIO_out state.

Transition DI2:4: When the received command is a READ DMA command, the device shall transition to the DDMAI0: DMA_in state.

Transition DI2:5: When the received command is a WRITE DMA command, the device shall transition to the DDMAO0: DMA_out state.

Transition DI2:6: When the received command is a PACKET command, the device shall transition to the DPKT0: PACKET state.

*** Transition DI2:7:** When the received command is a READ DMA QUEUED command, the device shall transition to the DDMAQI0: DMA_queued_in state.

*** Transition DI2:8:** When the received command is a WRITE DMA QUEUED command, the device shall transition to the DDMAQO0: DMA_queued_out state.

Transition DI2:9: When the received command is an EXECUTE DEVICE DIAGNOSTICS command, the device shall transition to the DEDD0: Execute_device_diag state.

Transition DI2:10: When the received command is an RESET DEVICE command, the device shall transition to the DDR0: Device_reset state.

Transition DI2:11: When the received command is not implemented by the device, the device shall transition to the DI3: No_command state.

*** Transition DI2:12:** When the received command is a SERVICE command, the device shall transition to the DI5: Service_test state.

*** Transition DI2:13:** When the received command is a READ FPDMA QUEUED command protocol, the device shall transition to the DFPDMAQ1: AddCommandToQueue state.

*** Transition DI2:14:** When the received command is a WRITE FPDMA QUEUED command protocol, the device shall transition to the DFPDMAQ1: AddCommandToQueue state.

*** Transition DI2:15:** When the received command is a not a READ FPDMA QUEUED; and not a WRITE FPDMA QUEUED; and not a DEVICE RESET; and there are native queued command(s) outstanding, an error has occurred and the device shall transition to the DFPDMAQ12: BrokenHost_ClearBusy state.

*** DI7: Service_decode state:** This state is entered when a Register FIS has been transmitted, if necessary to send the register contents, including the desired command tag, in response to a SERVICE command.

When in this state, the device shall again determine the type of command that the device has requested service to complete, and branch to that command's data transfer and completion.

Transition DI7:1: When the command to be serviced is a PIO data-in command, the device shall transition to the DPKT4: PACKET_PIO_in state.

Transition DI7:2: When the command to be serviced is a PIO data-out command, the device shall transition to the DPKT6: PACKET_PIO_out state.

Transition DI7:3: When the command to be serviced is a DMA data-in command, the device shall transition to the DPKT9: PACKET_DMA_in state.

Transition DI7:4: When the command to be serviced is a DMA data-out command, the device shall transition to the DPKT11: PACKET_DMA_out state.

Transition DI7:5: When the command to be serviced is a READ DMA QUEUED command, the device shall transition to the DDMAQI1: Send_data state.

Transition DI7:6: When the command to be serviced is a WRITE DMA QUEUED command, the device shall transition to the DDMAQO1: Send_DMA_activate state.

2.2 PACKET protocol

[**Editor's Note:** The changes marked in red (and underlined/strikethrough) will be incorporated in section 11.11]

This class includes:

- PACKET

States marked with an * are only utilized when queuing is implemented

DPKT0: PACKET	Request transmission of a PIO Setup FIS.		
	1. FIS transmission complete.	→	DPKT1: Receive_command

DPKT1: Receive_command	Receive Data FIS containing command packet.		
	1. FIS reception complete.	→	DPKT2: Check_command

DPKT2: Check_command	Determine the protocol required for the received command.		
	1. Non-data command.	→	DPKT3: PACKET_non-data
	2. PIO data-in command.	→	DPKT4: PACKET_PIO_in
	3. PIO data-out command.	→	DPKT6: PACKET_PIO_out
	4. DMA data-in command	→	DPKT9: PACKET_DMA_in
	5. DMA data-out command	→	DPKT11: PACKET_DMA_out

DPKT3: PACKET_non-data	Execute Non-data command.		
	1. Command execution complete.	→	DPKT14: Send_status

DPKT4: PACKET_PIO_in	Prepare a DRQ data block for transfer to the host.		
	1. DRQ data block ready to transfer.	→	DPKT4a: PIO_in_setup
	2. Transfer complete or command aborted due to error.	→	DPKT14: Send_status
	3. * DRQ block is not ready for immediate transfer	→	DPKT15: Release

DPKT4a: PIO_in_setup	Request transmission of a PIO Setup FIS to host.		
	1. PIO Setup FIS transmitted.	→	DPKT5: Send_PIO_data

DPKT5: Send_PIO_data	Request transmission of a Data FIS to host.		
	1. Data FIS transmitted.	→	DPKT4: PACKET_PIO_in

DPKT6: PACKET_PIO_out	Prepare to receive DRQ data block from the host.	
1. Ready to receive DRQ data block transfer.	→	DPKT7: PIO_out_setup
2. All DRQ data blocks received or command aborted due to error.	→	DPKT14: Send_status
3. * Not ready to accept DRQ block immediately.	→	DPKT15: Release

DPKT7: PIO_out_setup	Request transmission of a PIO Setup FIS to host.	
1. PIO Setup FIS transmitted.	→	DPKT8: Receive_PIO_data

DPKT8: Receive_PIO_data	Receive Data FIS from the Transport layer.	
1. Data FIS received.	→	DPKT6: PACKET_PIO_out

DPKT9: PACKET_DMA_in	Prepare data for the transfer of a Data FIS.	
1. Data for Data FIS ready to transfer.	→	DPKT10: Send_DMA_data
2. Command completed or aborted due to error.	→	DPKT14: Send_status
3. * Data is not ready for immediate transfer.	→	DPKT15: Release

DPKT10: Send_DMA_data	Request transmission of a Data FIS to host.	
1. Data FIS transmitted. No more data transfer required for this command, or 2048 Dwords (8KB) transmitted.	→	DPKT9: PACKET_DMA_IN

DPKT11: PACKET_DMA_out	Prepare to receive a Data FIS from the host.	
1. Ready to receive Data FIS.	→	DPKT12: Send_DMA_activate
2. All data requested for this command received or command aborted due to error.	→	DPKT14: Send_status
3. * Not ready for immediate transfer.	→	DPKT15: Release

DPKT12: Send_DMA_activate	Request transmission of a DMA Activate FIS to host.	
1. DMA Activate FIS transmitted.	→	DPKT13: Receive_DMA_data

DPKT13: Receive_DMA_data	Receive Data FIS from the Transport layer.	
1. Data FIS received.	→	DPKT11: PACKET_DMA_out

DPKT14: Send_status	Request transmission of a Register FIS.	
1. FIS transmission complete.	→	DI0: Device_idle

* DPKT15: Release	Request transmission of a Register FIS.	
1. FIS transmission complete.	→	DI0: Device_idle

DPKT0: PACKET: This state is entered when the device receives a PACKET command.

When in this state, the device shall request that the Transport layer transmit a PIO Setup FIS to acquire the command packet associated with this command. The initial status shall have BSY bit cleared to zero and DRQ bit set to one. The Interrupt bit shall be cleared to zero. The ending status shall have BSY bit set to one and DRQ bit cleared to zero. The byte count for the DRQ data block shall be indicated.

Transition DPKT0:1: When the PIO Setup FIS has been transferred, the device shall transition to the DPKT1: Receive_command state.

DPKT1: Receive_command: This state is entered when the device transmitted a PIO Setup FIS to the host to get the command packet.

When in this state, the device shall receive the requested Data FIS from the Transport layer.

Transition DPKT1:1: When the Data FIS has been received, the device shall transition to the DPKT2: Check_command state.

DPKT2: Check_command: This state is entered when the Data FIS containing the command packet has been received.

When in this state, the device shall determine the protocol for the command contained in the command packet.

Transition DPKT2:1: When the command is a non-data transfer command, the device shall transition to the DPKT3: PACKET_non-data state.

Transition DPKT2:2: When the command is a PIO data-in transfer command, the device shall transition to the DPKT4: PACKET_PIO_in state.

Transition DPKT2:3: When the command is a PIO data-out transfer command, the device shall transition to the DPKT6: PACKET_PIO_out state.

Transition DPKT2:4: When the command is a DMA data-in transfer command, the device shall transition to the DPKT9: PACKET_DMA_in state.

Transition DPKT2:5: When the command is a DMA data-out transfer command, the device shall transition to the DPKT11: PACKET_DMA_out state.

DPKT3: PACKET_non-data State: This state is entered when a received command is a non-data command.

When in this state, the device shall execute the requested command.

Transition DPKT3:1: When command execution completes, the device shall transition to the DPKT14: Send_status state.

DPKT4: PACKET_PIO_in State: This state is entered when the device receives a PIO data-in command or the transmission of one or more DRQ data blocks is required to complete the command.

When in this state, device shall prepare a DRQ data block for transfer to the host.

Transition DPKT4:1: When the device has a DRQ data block ready to transfer, the device shall transition to the DPKT4a: PIO_in_setup.

Transition DPKT4:2: When all of the data requested by this command has been transferred or the device has encountered an error that causes the command to abort before completing the transfer of the requested data, then the device shall transition to the DPKT14: Send_status state.

*** Transition DPKT4:3:** When the device supports overlap and queuing and does not have a DRQ data block ready to transfer immediately, the device shall transition to the DPKT15: Release state.

DPKT4a: PIO_in_setup: This state is entered when the device is ready to transfer a DRQ block to the host.

When in this state, the device shall request that the Transport layer transmit a PIO Setup FIS. The initial status shall have BSY bit cleared to zero and DRQ bit set to one. The Interrupt bit shall be set to one. The ending status shall have BSY bit set to one and DRQ bit cleared to zero. The byte count for the DRQ data block shall be indicated.

Transition DPKT4a:1: When the PIO Setup FIS has been transferred, the device shall transition to the DPKT5:Send_PIO_data state.

DPKT5:Send_PIO_data: This state is entered when the device is ready to transfer a DRQ data block to the host.

When in this state, the device shall request that the Transport layer transmit a Data FIS containing the DRQ data block.

Transition DPKT5:1: When the Data FIS has been transferred, the device shall transition to the DPKT4: PACKET_PIO_in state.

DPKT6: PACKET_PIO_out State: This state is entered when the device receives a PIO data-out command or the receipt of one or more DRQ data blocks is required to complete the command.

When in this state, device shall prepare to receive a DRQ data block transfer from the host.

Transition DPKT6:1: When the device is ready to receive a DRQ data block transfer, the device shall transition to the DPKT7: PIO_out_setup state.

Transition DPKT6:2: When the device has received all DRQ data blocks requested by this command or the device has encountered an error that causes the command to abort before completing the transfer of the requested data, then the device shall transition to the DPKT14: Send_status state.

*** Transition DPKT6:3:** When the device supports overlap and queuing and is not in a state in which it can accept a DRQ data block immediately, the device shall transition to the DPKT15: Release state.

DPKT7: PIO_out_setup: This state is entered when the device is ready to receive a DRQ data block from the host.

When in this state, the device shall request that the Transport layer transmit a PIO Setup FIS. The initial status shall have BSY bit cleared to zero and DRQ bit set to one. The Interrupt bit shall

be set to one. The ending status shall have BSY bit set to one and DRQ bit cleared to zero. The byte count for the DRQ data block shall be indicated.

Transition DPKT7:1: When the PIO Setup FIS has been transferred, the device shall transition to the DPKT8: Receive_PIO_data state.

DPKT8: Receive_PIO_data: This state is entered when the device transmitted a PIO Setup FIS to the host.

When in this state, the device shall receive the requested Data FIS from the Transport layer.

Transition DPKT8:1: When the Data FIS has been received, the device shall transition to the DPKT6: PACKET_PIO_out state.

DPKT9: PACKET_DMA_in State: This state is entered when the device receives a DMA data-in command or the transmission of one or more Data FIS is required to complete the command.

When in this state, device shall prepare the data for transfer of a Data FIS to the host.

Transition DPKT9:1: When the device has the data ready to transfer a Data FIS, the device shall transition to the DPKT10: Send_DMA_data state.

Transition DPKT9:2: When the device has transferred all of the data requested by this command or has encountered an error that causes the command to abort before completing the transfer of the requested data, then the device shall transition to the DPKT14: Send_status state.

*** Transition DPKT9:3:** When the device supports overlap and queuing and does not have data ready to transfer immediately, the device shall transition to the DPKT15: Release state.

DPKT10: Send_DMA_data: This state is entered when the device has the data ready to transfer a Data FIS to the host.

When in this state, the device shall request that the Transport layer transmit a Data FIS containing the data.

Transition DPKT10:1: When the Data FIS has been transferred, the device shall transition to the DPKT9: PACKET_DMA_in state. The device command layer shall request a data FIS size of no more than 2048 Dwords (8KB).

DPKT11: PACKET_DMA_out State: This state is entered when the device receives a DMA data-out command or the receipt of one or more Data FIS is required to complete the command.

When in this state, device shall prepare to receive a Data FIS from the host.

Transition DPKT11:1: When the device is ready to receive a Data FIS, the device shall transition to the DPKT12: Send_DMA_activate state.

Transition DPKT11:2: When the device has received all the data requested by this command or the device has encountered an error that causes the command to abort before completing the transfer of the requested data, then the device shall transition to the DPKT14: Send_status state.

*** Transition DPKT11:3:** When the device supports overlap and queuing and is not in a state which it can accept a Data FIS immediately, the device shall transition to the DPKT15: Release state.

DPKT12: Send_DMA_activate: This state is entered when the device is ready to receive a Data FIS from the host.

When in this state, the device shall request that the Transport layer transmit a DMA Activate FIS.

Transition DPKT12:1: When the DMA Activate FIS has been transferred, the device shall transition to the DPKT13: Receive_DMA_data state.

DPKT13: Receive_DMA_data: This state is entered when the device transmitted a DMA Activate FIS to the host.

When in this state, the device shall receive the requested Data FIS from the Transport layer.

Transition DPKT13:1: When the Data FIS has been received, the device shall transition to the DPKT11: PACKET_DMA_out state.

DPKT14: Send_status: This state is entered when the device has received all the data requested by this command or the device has encountered an error that causes the command to abort before completing the transfer of the requested data.

When in this state, the device shall request that the Transport layer transmit a Register FIS with register content as described in the command description in the ATA/ATAPI-6 standard and the Interrupt bit set to one.

Transition DPKT14:1: When the FIS has been transmitted, then the device shall transition to the DI0: Device_idle state.

*** DPKT15: Release:** This state is entered when the device is not able to do a data transfer immediately.

When in this state, the device shall request that the Transport layer transmit a Register FIS with register content as described in the command description in the ATA/ATAPI-6 standard, with the REL bit set to one, and, if the bus release interrupt has been enabled by a previous Set Features Command, with the Interrupt bit set to one.

Transition DPKT15:1: When the FIS has been transmitted, then the device shall transition to the DI0: Device_idle state.