Proposed Draft

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Serial ATA Revision 3.2 Design Guide # 005 Title : Recommendation to Disconnect P1 and P2 on Device Sleep or Power Disable Capable Host Systems

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Document History

Version	Date	Comments
0	3/12/2013	Initial release.
1	3/17/2013	Minor editorial updates based on Harvey's feedback
2	3/20/2013	Updates per CabCon feedback. Added new diagram showing path to ground
2a	3/25/2013	Additional CABCON feedback
3	3/27/2013	Update note in figure
4	6/14/2013	Ratified
5	2/7/2014	Add Power Disable
6	3/17/2014	Date correction, minor fixes and update to intro
7	3/21/2014	Corrections to sync with ratified version 4 for figures and tables
8	3/31/2014	Corrected 'tied' to 'connected' in footnotes
9	4/16/2014	Member review

1 Introduction

With the introduction of Device Sleep and Power Disable, drives using the standard SATA connector (3.5 inch and 2.5 inch) had the 3.3 V pins retired and then repurposed. Pins P1 and P2 have been retired and P3 of the standard SATA connector is now the DEVSLP/PWDIS signal line. ~~Device Sleep capable designs have a device side pull up resistor to establish the voltage for signaling entrance to DevSleep. The host mechanism is to float the DEVSLP signal line and the device's pull up resistor causes the line to be pulled high (signal entry to Device Sleep). The host pulls the DEVSLP line low (0 V) to exit Device Sleep.~~ For further descriptions on Device Sleep and Power Disable see SATA specification.

2 Situation

As a result of P3 being utilized as the DEVSLP/PWDIS signal line and 3.3 V not currently being used by the standard SATA connector, P1 and P2 are now defined as retired for both the host and device. The signal assignment table recommends the device connect P1 and P2 together to support legacy applications.

The SATA spec defines that a pin designated as retired should be disconnected, however, this does not prevent a host from adding Device Sleep or Power Disable support and continuing to provide 3.3 V to P1 and P2 since the retired definition states "should". While this is not an issue for Device Sleep/Power Disable capable devices (they may have P1 and P2 tied together), it may cause a problem for hosts if legacy or non Device Sleep/Power Disable capable drives are installed. A legacy device or a device which does not support Device Sleep/Power Disable may have P1, P2, and P3 tied together. A host that supplies 3.3 V to P1 and P2 may have that voltage then applied back through P3 (DEVSLP/PWDIS) if a device with P1, P2, and P3 tied together is connected to that host. This could possibly result in damage to the host system, depending on the DEVSLP/PWDIS circuitry.

3 Recommendation

It is strongly recommended that host solutions to not supply 3.3 V to P1 and P2 on Device Sleep/Power Disable capable ports.

4 Supplemental Information

Figure 1 is the electrical diagram for the DEVSLP signal line.

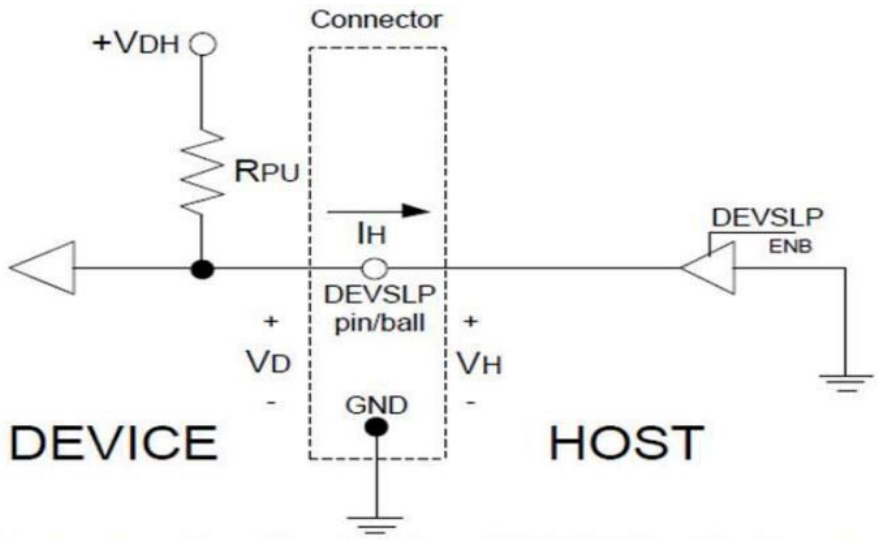
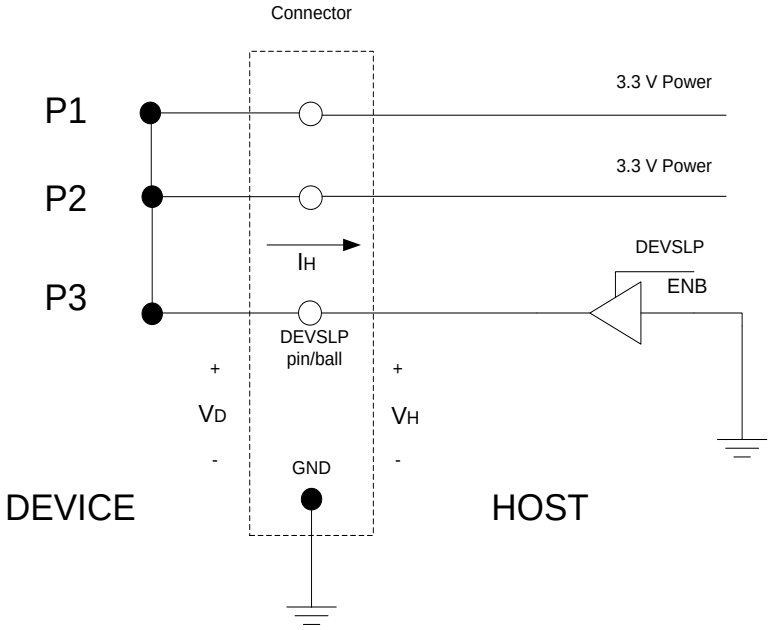


Figure 1 – Example DEVSLP electrical block diagram

Figure 2 shows a Device Sleep capable host plugged into a device that ties P1, P2, and P3 together. Applying 3.3 V to P1 and P2 provide a path to ground via the DEVSLP (P3) line with a device that ties P1, P2, and P3 together.



NOTE – Do not connect 3.3 V to P1 and P2 for a Device Sleep capable host.

Figure 2 – 3.3 V routed back to host via P3

Retired

A keyword indicating that the designated bits, bytes, fields, code values or physical resources (e.g., such as pins on a connector) that had been defined in previous standards are not defined in this standard and may be reclaimed for other uses in future standards. Retired pins on a connector should be left not connected. If retired bits, bytes, fields, code values or physical resources (e.g., such as pins on a connector) are utilized before they are reclaimed, they shall have the meaning or functionality as described in previous standards.

	Name	Type	Description	Cable Usage[b c]	Backplane Usage[c]
Signal Segment Key					
Signal Segment	S1	GND		1st Mate	2nd Mate
	S2	A+	Differential Signal Pair A	2nd Mate	3rd Mate
	S3	A-		2nd Mate	3rd Mate
	S4	GND		1st Mate	2nd Mate
	S5	B-	Differential Signal Pair B	2nd Mate	3rd Mate
	S6	B+		2nd Mate	3rd Mate
	S7	GND		1st Mate	2nd Mate
Signal Segment "L"					
Central Connector Gap[d]					
Power Segment "L"					
Power Segment	P1	Retired [e f g]		2nd Mate	3rd Mate
	P2	Retired [e f g]		2nd Mate	3rd Mate
	P3	PWDIS [e]/ DEVSLP [e]	Enter/Exit Power Disable/ Enter/Exit DevSleep	1st Mate	2nd Mate
	P4	GND		1st Mate	1st Mate
	P5	GND		1st Mate	2nd Mate
	P6	GND		1st Mate	2nd Mate
	P7	V_5	5 V Power, Pre-charge	1st Mate	2nd Mate
	P8	V_5	5 V Power	2nd Mate	3rd Mate
	P9	V_5	5 V Power	2nd Mate	3rd Mate
	P10	GND		1st Mate	2nd Mate
	P11	DAS/DSS/DHU	Device Activity Signal / Disable Staggered Spinup/ Direct Head Unload / Vendor Specific[a]	2nd Mate	3rd Mate
	P12	GND		1st Mate	1st Mate
	P13	V_{12}	12 V Power, Pre-charge	1st Mate	2nd Mate
	P14	V_{12}	12 V Power	2nd Mate	3rd Mate
	P15	V_{12}	12 V Power	2nd Mate	3rd Mate
Power Segment Key					

NOTE:

[a] For specific optional usage of pin P11 see SATA specification.

[b] Although the mate order is shown, hot plugging is not supported when using the cable connector receptacle.

[c] All mate sequences assume zero angular offset between connectors.

[d] The signal segment and power segment may be separate.

[e] Previous versions of this specification assigned 3.3V to pins P1, P2 and P3. In addition, device plug pins P1, P2, and P3 were required to be bused together.

[f] If using DEVSLP, it is recommended to have P1 and P2 ~~tied~~connected together for purpose of legacy functionality.

[g] If using PWDIS, it is recommended to have P1 and P2 connected together for purpose of legacy functionality.