Proposed Draft **Serial ATA International Organization**

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Serial ATA ECN #045 for SATA30_TPR_C101 mSATA Connector Specification Title: Interface Detect Pin for mSATA Connector

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Document History

Version	Date	Comments
1	04/05/2010	Initial ECN draft converted over from a previewed TPR draft. Includes editorial cleanup to remove named reference to non-mSATA cards plus additional detail in introduction material to discuss managing the change transition prior to the next major SATA specification release.
2	05/05/2010	Editorial updates for clarification benefit

1. Introduction

1.1 Problem Statement

This ECN is intended to define a change to the electrical pin-out to the mSATA interface connector. This change will enable in a consistent way the ability to detect the platform OEM installation of either mSATA cards or non-mSATA cards in a socket intended to be configurable between these multiple card types.

This ECN accepts as a premise that it is reasonable to assume that platform designers will want to enable configurable sockets such that when mSATA card installation is not needed in a particular platform configuration, the socket should still be alternately available for use with non-mSATA cards. Given that these other cards have been in the market much longer than mSATA, the change to support configurability is being made of the mSATA solution as opposed to trying to affect a change to the specifications upon which non-mSATA products have been shipping for years.

1.2 Solution Summary

This ECN changes one of the 14 GND pins (Pin 43 is proposed) to a No Connect pin such that it differentiates mSATA cards from existing non-mSATA cards. The will enable a platform OEM to construct a logic signal using a pull-up resistor that could be used for socket configuration purposes.

1.3 Change Applicability

Given that this ECN changes an existing pin definition on mSATA products that are shipping, the applicability of this change to future cards that ship as mSATA compliant product will have to be managed by the platform OEMs. If a platform OEM chooses to implement configurable shareable sockets, then that OEM will be responsible for making sure that the particular mSATA cards that are acquired and used in that socket comply with this change request. When TRP_C101 (mSATA specification) is integrated into the next SATA specification release, this ECN will become a normative specification. Once this ECN is approved, mSATA card suppliers are encouraged to incorporate this change at their earliest convenience to help smooth the transition.

2 Technical Specification Changes

2.1 Changes to Section 1.4.2 of TPR_C101

<Changes are highlighted in red>

1.4.2 Internal mSATA pin signal definition

Table 1 defines the signal assignment of the internal mSATA connection. This connection does not support hot plug capability, so there is no connection sequence specified. There are a total of 52 pins.

- 5 pins for 3.3V source
- 3 pins for 1.5V source
- ~~14~~13 pins for GND
- 4 pins for transmitter/receiver differential pairs
- 1 pin for device activity / disable staggered spin-up
- 1 pin for presence detection
- 2 pins for Vendor Specific / Manufacturing
- 2 pins for Vendor Specific
- 20 reserved pins (no connect)
- 1 pin to indicate mSATA use (no connect)

Table 1 Signal Assignments for mSATA (proposed)

Pin #	Type	Description
P1	Reserved	No Connect
P2	+3.3V	3.3V Source
P3	Reserved	No Connect
P4	GND	Return Current Path
P5	Reserved	No Connect
P6	+1.5V	1.5V Source
P7	Reserved	No Connect
P8	Reserved	No Connect
P9	GND	Return Current Path
P10	Reserved	No Connect
P11	Reserved	No Connect
P12	Reserved	No Connect
P13	Reserved	No Connect
P14	Reserved	No Connect
P15	GND	Return Current Path
P16	Reserved	No Connect
P17	Reserved	No Connect
P18	GND	Return Current Path
P19	Reserved	No Connect
P20	Reserved	No Connect
P21	GND	Return Current Path
P22	Reserved	No Connect
P23	+B	Host Receiver Differential Signal Pair
P24	+3.3V	3.3V Source
P25	-B	Host Receiver Differential Signal Pair
P26	GND	Return Current Path
P27	GND	Return Current Path
P28	+1.5V	1.5V Source
P29	GND	Return Current Path
P30	Two Wire Interface	Two Wire Interface Clock[3]
P31	-A	Host Transmitter Differential Signal Pair
P32	Two Wire Interface	Two Wire Interface Data[3]
P33	+A	Host Transmitter Differential Signal Pair

P34	GND	Return Current Path
P35	GND	Return Current Path
P36	Reserved	No Connect
P37	GND	Return Current Path
P38	Reserved	No Connect
P39	+3.3V	3.3V Source
P40	GND	Return Current Path
P41	+3.3V	3.3V Source
P42	Reserved	No Connect
P43	~~GND~~ No Connect	~~Return Current Path~~ No connect indicates mSATA use[4]
P44	Reserved	No Connect
P45	Vendor	Vendor Specific / Manufacturing Pin[2]
P46	Reserved	No Connect
P47	Vendor	Vendor Specific / Manufacturing Pin[2]
P48	+1.5V	1.5V Source
P49	DA/DSS	Device Activity Signal / Disable Staggered Spin-up
P50	GND	Return Current Path
P51	Presence Detection	Shall be pulled to GND by device[1]
P52	+3.3V	3.3V Source

NOTE:

1. Presence detection pin provided for tamper proof functionality
2. No connect on the host side.
3. Pins 30 and 32 are intended for use as a two wire interface to read a memory device to determine device information (an example of this would be for use as SMB bus pins). These pins are not designed to be active in conjunction with the SATA signal differential pairs.
4. Pin 43 to be No Connect on the mSATA card to enable differentiation between mSATA and non-mSATA cards – configurable shared socket designs may use a system side pull-up resistor to establish a logical differentiation usable to assist in interface configuration given that non-mSATA cards will ground this pin.