Proposed Draft

Serial ATA International Organization

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Title : Change of receiver test pattern specification to include Logo Framed Composite Pattern.

Author Information

Author Name	Company	Email address
John Calvin	Tektronix	John.c.calvin@tektronix.com

Workgroup Chair Information

Workgroup (Phy, Digital, etc…)	Chairperson Name	Email address
Phy WG	Chuck Hill	cphill@altaeng.comj

Document History

Version	Date	Comments
.10	03/04/2011	Initial release.
.20	03/10/2011	Revisions after first review by Phy on 03/09/2011 and group edits in Logo.
.30	03/14/2011	Added Harvey's tabular form of the Framed Composite pattern.
.40	03/14/2011	Table formatting.
.50	03/14/2011	Clean up text in table for number of times to repeat.

1 Introduction

1.1 Problem Statement

Clarify the precise pattern used to perform a frame error rate test on a receiver, and reduce the amount of test time by specifying a single test pattern to be used in this test.

The LOGO organization currently (has for the last 4 years) tested with a variant of the COMP pattern which has proven both efficient and effective. This pattern is found and specified in the UTD here.
http://www.serialata.org/documents/Interop_UnifiedTest_Rev1_4_v1_01_06242010.pdf
Page 109 (Section 4.1) Detailed at the end of this ECN for reference.

The LOGO Framed COMP pattern, incorporates three changes from the currently spec'ed COMP pattern.

1. In-line with section 7.2.4.2 the COMP pattern is framed. This changes the pattern.
2. LOGO has introduced 2 ALIGN primitives every 256 Dwords to make it compliant.
3. A short Inter Gap region is introduced before and after the SOF/EOF to ensure that when repeated sequentially by a generator the 256 Dword ALIGN primitives are perfectly and uniformly spaced 256 Dwords apart even after wrap-around by the generator.

These minimal changes are required in-order to make receiver testing work with Frame Error Detectors.

7.2.4.2 Compliant Frame Patterns

The frame error rates specified in section 7.4.1.2 shall be tested for compliance when subjected to any implementation-determined worst-case compliant patterns, as well as the following set of compliant patterns:

a) Compliant Lone Bit Patterns as per section 7.2.4.3.5.
b) Compliant composite patterns as per section 7.2.4.3.6.

Where the qualifying prefix term "compliant" signifies transmission of the cited pattern encapsulated in payload of a Data FIS, and used in a Serial ATA operational transmission context.

Note that the cited patterns should appear on the wire, and the N parameters of the reference patterns shall be extended to achieve the maximum frame length. These compliant patterns contain the necessary SOF_P leading primitive, the Dword header containing the FIS Type indicating a Data FIS, the specified test pattern, the calculated CRC, and the trailing EOF_P, as shown in Figure 141. To generate these patterns on the SATA link, scrambling needs to be taken into account.

SOF_P	Data FIS Header	Specified Test Pattern	CRC	EOF_P

Figure 141 – Compliant Test Patterns

Text Excerpt from section:

7.2.4.2 Compliant Frame Patterns

The frame error rates specified in section 7.4.1.2 shall be tested for compliance when subjected to any implementation-determined worst-case compliant patterns, as well as the following set of compliant patterns:

a) FCOMP pattern as per section xyz
b) Compliant Lone Bit Patterns as per section 7.2.4.3.5.
c) Compliant composite patterns as per section 7.2.4.3.6.

Where the qualifying prefix term "compliant" signifies transmission of the cited pattern encapsulated in payload of a Data FIS, and used in a Serial ATA operational transmission context.

Note that the cited patterns should appear on the wire, and the N parameters of the reference patterns shall be extended to achieve the maximum frame length. These compliant patterns contain the necessary SOF_P leading primitive, the Dword header containing the FIS Type indicating a Data FIS, the specified test pattern, the calculated CRC, and the trailing EOF_P, as shown in Figure 141. To generate these patterns on the SATA link, scrambling needs to be taken into account.

7.4.11 Receiver Tolerance (Gen1i, Gen2i, Gen1m, Gen2m)

The performance measure for receiver tolerance and common mode interference rejection is the correct detection of data by the receiver. When measuring receiver and Common Mode tolerance it is necessary to set the maximum allowable jitter and common mode interference on the signal sent to the receiver and monitor data errors.

The data signal source provides a data signal with jitter, and a controlled rise/fall time, with matched output impedance. The sine wave source provides common mode interference with matched output impedance. The two sources are combined with resistive splitters into the receiver under test (see Figure 168). Equivalent signal generation methods that provide the data with jitter, common mode interference, and an impedance-matched output are allowed. All the interconnect characteristics of the receiver, mated connector pair, printed circuit board traces, and package are included in the measured receiver jitter tolerance.

Figure 167 shows a setup to set the level of jitter and common mode signal at the compliance point, on the cable side of the mated pair connector. The JMD is used as the standard for measuring jitter, and the HBWS is used as the standard for measuring the common mode interference. Since the SATA adapter is not included when setting the level of jitter, good matching and low loss in the adapter are desirable to minimize contributions to the amount of receiver jitter used in testing. Unlike other measurements, it is generally not possible to remove the effects of the SATA adapter on jitter since jitter due to mismatch depends on the entire test setup. Figure 168 shows one example approach to generate the Lab-Sourced signal.

The receiver tolerance test shall be conducted over variations in parameters SSC on and off, maximum and minimum rise and fall times, minimum and maximum amplitude, common mode interference over the specified frequency range, the test patterns LBP and the full payload COMP described in section 7.2.4.3, and jitter which includes random and deterministic jitter of various types: data dependent, periodic, duty cycle distortion. The receiver tolerance to the impairments is required over all signal variations.

Text Excerpt from section:

The receiver tolerance test shall be conducted over variations in parameters SSC on and off, maximum and minimum rise and fall times, minimum and maximum amplitude, common mode interference over the specified frequency range, **the test patterns LBP and the full payload COMP described in section 7.2.4.3**, and jitter which includes random and deterministic jitter of various types: data dependent, periodic, duty cycle distortion. The receiver tolerance to the impairments is required over all signal variations.

7.2.1 **Physical Layer Requirements Tables**

Table 34 – General Specifications

Parameters	Units	Limit	Electrical Specification					Detail Cross-Ref Section	Measurement Cross-Ref Section
			Gen1i	Gen1m	Gen2i	Gen2m	Gen3i		
Channel Speed	Gbps	Nom	1.5		3.0		6.0	7.2.2.1.1	-
Fbaud	GHz	Nom	1.5		3.0		6.0	-	-
FER, Frame Error Rate		Max	8.2e-8 at 95% confidence level		8.2e-8 at 95% confidence level		8.2e-8 at 95% confidence level	7.2.2.1.2	7.4.1

Section 7.2.2.5

The Lab-Sourced signal is a laboratory generated signal which is calibrated into an impedance matched load of 100 Ohms differential and 25 Ohms common mode and then applied to the RX+ and RX- signals of the Receiver Under Test.In the case of Gen3i, the Gen3i CIC is inserted in the signal path applied to the RX. (see section 7.4.12) The load used to calibrate the LSS shall have an individual return loss greater than 20 dB over a bandwidth of 100 MHz to 5.0 GHz, and greater than 10 dB from 5 GHz to 8 GHz. During calibration, the characteristics of the Lab-Sourced signal shall comply with the specifications of Table 38. When this signal is then applied to the Receiver Under Test the Frame Error Rate specifications of Table 34 shall be met.

Text Excerpt from section:
matched load of 100 Ohms differential and 25 Ohms common mode and then applied to the RX+ and RX- signals of the Receiver Under Test. In the case of Gen3i, the Gen3i CIC is inserted in the signal path applied to the RX. (see section 7.4.12) The load used to calibrate the LSS shall have an individual return loss greater than 20 dB over a bandwidth of 100 MHz to 5.0 GHz, and greater than 10 dB from 5 GHz to 8 GHz. During calibration, the characteristics of the Lab-Sourced signal shall comply with the specifications of Table 38. **When this signal is then applied to the Receiver Under Test the Frame Error Rate specifications of Table 34 shall be met.**

1.2 Solution Summary

Assuming one agrees there is a problem here (and does not subscribe to the Short Version outlined above) there are two avenues to consider.

1. Modify the SATA spec to consider a bit error detector method rather than a frame error detection method. Estimate a significant amount of work here.
2. Modify the SATA spec to embrace the LOGO Framed COMP pattern into the specification (or replace the current COMP pattern) and retain the current frame error detection method of error analysis. Estimate an easier change here.

Proposed Spec Changes in support of option 2 above:

7.2.4.2 Compliant Frame Patterns

The frame error rates specified in section 7.4.1.2 shall be tested for compliance when subjected to any implementation-determined worst-case compliant patterns, as well as the following set of compliant patterns:

a) Compliant Framed Composite patterns as per section 7.2.4.3.7.
~~a~~b) Compliant Lone Bit Patterns as per section 7.2.4.3.5.
~~b~~c) ~~Compliant composite patterns as per section 7.2.4.3.6.~~ << Note: We could debate this..

7.4.11 Receiver Tolerance (Gen1i, Gen2i, Gen1m, Gen2m)

..

The receiver tolerance test shall be conducted over variations in parameters SSC on and off, maximum and minimum rise and fall times, minimum and maximum amplitude, common mode interference over the specified frequency range, the test pattern~~s~~ FCOMP ~~or LBP and the full payload COMP~~ described in section 7.2.4.~~3~~2, and jitter which includes random and deterministic jitter of various types: data dependent, periodic, duty cycle distortion. The receiver tolerance to the impairments is required over all signal variations.

7.4.12 Receiver Tolerance (Gen3i)

..

The receiver tolerance test shall be conducted over variations in parameters SSC on and off, minimum and maximum amplitude, common mode interference over the specified frequency range, the test pattern~~s~~ FCOMP ~~or LBP and the full payload COMP~~ described in section 7.2.4.~~3~~2, and jitter which includes the maximum random and deterministic jitter of various types: data dependent, periodic, duty cycle distortion. The receiver tolerance to the impairments is required over all signal variations.

7.2.4.2 Compliant Frame Patterns

The frame error rates specified in section 7.4.1.2 shall be tested for compliance when subjected to any implementation-determined worst-case compliant patterns, as well as the following set of compliant patterns:

a) FCOMP pattern as per section 7.2.4.3.7
b) Compliant Lone Bit Patterns as per section 7.2.4.3.5.
~~c) Compliant composite patterns as per section 7.2.4.3.6.~~

7.2.4.3.7 Framed Composite Pattern (FCOMP)

The Framed Composite Pattern is equivalent to the COMP pattern in section 7.2.4.3.6 with the following structured changes:

1. In-line with section 7.2.4.2 the COMP pattern is framed. ~~This changes the pattern.~~
2. 2 ALIGN primitives inserted every 256 Dwords.
3. A short Inter Gap region is introduced before and after the SOF/EOF to ensure that when repeated sequentially by a generator the 256 Dword ALIGN primitives are perfectly and uniformly spaced 256 Dwords apart even after wrap-around by the generator.

1.2.1.1.1 Framed Composite Pattern (FCOMP)

Table FF – Framed Composite Pattern (FCOMP)

Transmission Order →

	K28.5(BCh)+		D10.2(4Ah)-			D10.2(4Ah)-			D27.3(7Bh)-		
+	1100	0001	0101	0101	0101	0101	0101	0111	0110	0011	+
	C	1	5	5	5	5	5	7	6	3	
	Above Dword is repeated a total of 2 times. 2 DW ALIGNp.										
	D10.2(4Ah)+		D10.2(4Ah)+			D10.2(4Ah)+			D10.2(4Ah)+		
+	0101	0101	0101	0101	0101	0101	0101	0101	0101	0101	+
	5	5	5	5	5	5	5	5	5	5	
	Above Dword is repeated a total of 7 times. 7 DW HFTP										
	K28.3(7Ch)+		D21.5(B5h)-			D23.2(57h)-			D23.2(57h)+		
+	1100	0011	0010	1010	1010	1110	1001	0100	0101	0101	-
	C	3	2	A	A	E	9	4	5	5	
	X_RDYp with RD+										
	K28.3(7Ch)-		D21.5(B5h)+			D23.2(57h)+			D23.2(57h)-		
-	0011	1100	1110	1010	1010	0001	0101	0111	1010	0101	+
	3	C	E	A	A	1	5	7	A	5	
	Above 2 Dword is repeated a total of 2 times. X_RDYp with RD-										
	K28.3(7Ch)+		D21.5(B5h)-			D23.2(57h)-			D23.2(57h)+		
+	1100	0011	0010	1010	1010	1110	1001	0100	0101	0101	-
	C	3	2	A	A	E	9	4	5	5	
	X_RDYp with RD+ All together 5 DW X_RDYp										
	K28.3(7Ch)-		D21.5(B5h)+			D23.1(37h)+			D23.1(37h)-		
-	0011	1100	1110	1010	1010	0001	0110	0111	1010	1001	+
	3	C	E	A	A	1	6	7	A	9	
	SOFp										

+	D11.6(CBh)+		D22.3(76h)+			D18.6(D2h)+			D3.0(C2h)+		-
	1101	0001	1001	1010	0011	0100	1101	1001	0010	0110	
	D	1	9	A	3	4	D	9	2	6	
	Data FIS Header										
-	D31.3(7Fh)-		D31.3(7Fh)+			D31.3(7Fh)-			D31.3(7Fh)+		-
	1010	1100	1101	0100	1100	1010	1100	1101	0100	1100	
	A	C	D	4	C	A	C	D	4	C	
	Above Dword is repeated a total of 240 times. SSOP										
-	K28.5(BCh)-		D10.2(4Ah)+			D10.2(4Ah)+			D27.3(7Bh)+		-
	0011	1110	1001	0101	0101	0101	0101	0100	1001	1100	
	3	E	9	5	5	5	5	4	9	C	
	Above Dword is repeated a total of 2 times. ALIGNp										
-	D31.3(7Fh)-		D31.3(7Fh)+			D31.3(7Fh)-			D31.3(7Fh)+		-
	1010	1100	1101	0100	1100	1010	1100	1101	0100	1100	
	A	C	D	4	C	A	C	D	4	C	
	Above Dword is repeated a total of 16 times. A total of 256 DW SSOP.										
-	D21.5(B5h)-		D21.5(B5h)-			D21.5(B5h)-			D21.5(B5h)-		-
	1010	1010	1010	1010	1010	1010	1010	1010	1010	1010	
	A	A	A	A	A	A	A	A	A	A	
	Above Dword is repeated a total of 64 times. HTDP										
-	D24.3(78h)-		D24.3(78h)+			D24.3(78h)-			D24.3(78h)+		-
	1100	1100	1100	1100	1100	1100	1100	1100	1100	1100	
	C	C	C	C	C	C	C	C	C	C	
	Above Dword is repeated a total of 64 times. HTDP										
-	D10.2(4Ah)-		D10.2(4Ah)-			D10.2(4Ah)-			D10.2(4Ah)-		-
	0101	0101	0101	0101	0101	0101	0101	0101	0101	0101	
	5	5	5	5	5	5	5	5	5	5	
	Above Dword is repeated a total of 64 times. HTDP										
-	D25.6(D9h)-		D6.1(26h)-			D25.6(D9h)-			D6.1(26h)-		-
	1001	1001	1001	1001	1001	1001	1001	1001	1001	1001	
	9	9	9	9	9	9	9	9	9	9	
	Above Dword is repeated a total of 46 times. HTDP										

-	K28.5(BCh)-		D10.2(4Ah)+			D10.2(4Ah)+			D27.3(7Bh)+		-
	0011	1110	1001	0101	0101	0101	0101	0100	1001	1100	
	3	E	9	5	5	5	5	4	9	C	

Above Dword is repeated a total of 2 times.
ALIGNp

-	D25.6(D9h)-		D6.1(26h)-			D25.6(D9h)-			D6.1(26h)-		-
	1001	1001	1001	1001	1001	1001	1001	1001	1001	1001	
	9	9	9	9	9	9	9	9	9	9	

Above Dword is repeated a total of 18 times.
256DW HTDP (64DW, 64DW, 64DW, 64DW)

-	D17.7(F1h)-		D30.7(FEh)+			D7.1(27h)+			D14.7(EEh)+		-
	1000	1101	1110	0001	1110	0001	1110	0101	1100	1000	
	8	D	E	1	E	1	E	5	C	8	

LTDP

-	D30.7(FEh)-		D7.6(C7h)-			D30.3(7Eh)-			D30.3(7Eh)+		-
	0111	1000	0111	1000	0110	0111	1000	1110	0001	1100	
	7	8	7	8	6	7	8	E	1	C	

LTDP

-	D30.3(7Eh)-		D30.3(7Eh)+			D30.3(7Eh)-			D30.3(7Eh)+		-
	0111	1000	1110	0001	1100	0111	1000	1110	0001	1100	
	7	8	E	1	C	7	8	E	1	C	

Above Dword is repeated a total of 234 times.
LTDP

-	K28.5(BCh)-		D10.2(4Ah)+			D10.2(4Ah)+			D27.3(7Bh)+		-
	0011	1110	1001	0101	0101	0101	0101	0100	1001	1100	
	3	E	9	5	5	5	5	4	9	C	

Above Dword is repeated a total of 2 times.
ALIGNp

-	D30.3(7Eh)-		D30.3(7Eh)+			D30.3(7Eh)-			D30.3(7Eh)+		-
	0111	1000	1110	0001	1100	0111	1000	1110	0001	1100	
	7	8	E	1	C	7	8	E	1	C	

Above Dword is repeated a total of 254 times.
LTDP

-	K28.5(BCh)-		D10.2(4Ah)+			D10.2(4Ah)+			D27.3(7Bh)+		-
	0011	1110	1001	0101	0101	0101	0101	0100	1001	1100	
	3	E	9	5	5	5	5	4	9	C	

Above Dword is repeated a total of 2 times.
ALIGNp

-	D30.3(7Eh)-			D30.3(7Eh)+		D30.3(7Eh)-			D30.3(7Eh)+		-
	0111	1000	1110	0001	1100	0111	1000	1110	0001	1100	
	7	8	E	1	C	7	8	E	1	C	

Above Dword is repeated a total of 21 times.
LTDP

-	D3.7(E3h)-			D28.7(FCh)+		D3.7(E3h)-			D28.7(FCh)+		-
	1100	0111	1000	1110	0001	1100	0111	1000	1110	0001	
	C	7	8	E	1	C	7	8	E	1	

512DW LTDP (1DW, 1DW, 509DW, 1DW)

-	D12.0(0Ch)-			D11.4(8Bh)+		D12.0(0Ch)-			D11.3(6Bh)+		+
	0011	0110	1111	0100	0010	0011	0110	1111	0100	0011	
	3	6	F	4	2	3	6	F	4	3	

LBP

+	D12.0(0Ch)+			D11.4(8Bh)-		D12.0(0Ch)+			D11.3(6Bh)-		-
	0011	0101	0011	0100	1101	0011	0101	0011	0100	1100	
	3	5	3	4	D	3	5	3	4	C	

Above 2 Dwords are repeated a total of 116 times.
LBP

-	K28.5(BCh)-			D10.2(4Ah)+		D10.2(4Ah)+			D27.3(7Bh)+		-
	0011	1110	1001	0101	0101	0101	0101	0100	1001	1100	
	3	E	9	5	5	5	5	4	9	C	

Above Dword is repeated a total of 2 times.
ALIGNp

-	D12.0(0Ch)-			D11.4(8Bh)+		D12.0(0Ch)-			D11.3(6Bh)+		+
	0011	0110	1111	0100	0010	0011	0110	1111	0100	0011	
	3	6	F	4	2	3	6	F	4	3	

LBP

+	D12.0(0Ch)+			D11.4(8Bh)-		D12.0(0Ch)+			D11.3(6Bh)-		-
	0011	0101	0011	0100	1101	0011	0101	0011	0100	1100	
	3	5	3	4	D	3	5	3	4	C	

Above 2 Dwords are repeated a total of 12 times.
256DW LBP ((1DW,1DW) x 128)

-	D20.2(54h)-			D20.2(54h)-		D20.2(54h)-			D20.2(54h)-		-
	0010	1101	0100	1011	0101	0010	1101	0100	1011	0101	
	2	D	4	B	5	2	D	4	B	5	

Above Dword is repeated a total of 230 times.
LFSCP

-	K28.5(BCh)-		D10.2(4Ah)+			D10.2(4Ah)+			D27.3(7Bh)+		-
	0011	1110	1001	0101	0101	0101	0101	0100	1001	1100	
	3	E	9	5	5	5	5	4	9	C	

Above Dword is repeated a total of 2 times.
ALIGNp

-	D20.2(54h)-		D20.2(54h)-			D20.2(54h)-			D20.2(54h)-		-
	0010	1101	0100	1011	0101	0010	1101	0100	1011	0101	
	2	D	4	B	5	2	D	4	B	5	

Above Dword is repeated a total of 25 times.
LFSCP

-	D20.2(54h)-		D20.7(F4h)-			D11.5(ABh)+			D11.5(ABh)+		+
	0010	1101	0100	1011	0111	1101	0010	1011	0100	1010	
	2	D	4	B	7	D	2	B	4	A	

LFSCP

+	D11.5(ABh)+		D11.5(ABh)+			D11.5(ABh)+			D11.5(ABh)+		+
	1101	0010	1011	0100	1010	1101	0010	1011	0100	1010	
	D	2	B	4	A	D	2	B	4	A	

Above Dword is repeated a total of 228 times.
LFSCP

+	K28.5(BCh)+		D10.2(4Ah)-			D10.2(4Ah)-			D27.3(7Bh)-		+
	1100	0001	0101	0101	0101	0101	0101	0111	0110	0011	
	C	1	5	5	5	5	5	7	6	3	

Above Dword is repeated a total of 2 times.
ALIGNp

+	D11.5(ABh)+		D11.5(ABh)+			D11.5(ABh)+			D11.5(ABh)+		+
	1101	0010	1011	0100	1010	1101	0010	1011	0100	1010	
	D	2	B	4	A	D	2	B	4	A	

Above Dword is repeated a total of 27 times.
LFSCP

+	D11.5(ABh)+		D11.7(EBh)+			D20.2.(54h)-			D20.2.(54h)-		-
	1101	0010	1011	0100	1000	0010	1101	0100	1011	0101	
	D	2	B	4	8	2	D	4	B	5	

512DW LFSCP (255DW, 1DW, 255DW, 1DW)

-	D21.5(B5h)-		D21.5(B5h)-			D21.5(B5h)-			D21.5(B5h)-		-
	1010	1010	1010	1010	1010	1010	1010	1010	1010	1010	
	A	A	A	A	A	A	A	A	A	A	

Above Dword is repeated a total of 64 times.
HTDP

-	D24.3(78h)-		D24.3(78h)+			D24.3(78h)-			D24.3(78h)+		
	1100	1100	1100	1100	1100	1100	1100	1100	1100	1100	-
	C	C	C	C	C	C	C	C	C	C	
	Above Dword is repeated a total of 64 times. HTDP										
-	D10.2(4Ah)-		D10.2(4Ah)-			D10.2(4Ah)-			D10.2(4Ah)-		
	0101	0101	0101	0101	0101	0101	0101	0101	0101	0101	-
	5	5	5	5	5	5	5	5	5	5	
	Above Dword is repeated a total of 64 times. HTDP										
-	D25.6(D9h)-		D6.1(26h)+			D25.6(D9h)-			D6.1(26h)+		
	1001	1001	1001	1001	1001	1001	1001	1001	1001	1001	-
	9	9	9	9	9	9	9	9	9	9	
	Above Dword is repeated a total of 34 times. HTDP										
-	K28.5(BCh)-		D10.2(4Ah)+			D10.2(4Ah)+			D27.3(7Bh)+		
	0011	1110	1001	0101	0101	0101	0101	0100	1001	1100	-
	3	E	9	5	5	5	5	4	9	C	
	Above Dword is repeated a total of 2 times. ALIGNp										
-	D25.6(D9h)-		D6.1(26h)+			D25.6(D9h)-			D6.1(26h)+		
	1001	1001	1001	1001	1001	1001	1001	1001	1001	1001	-
	9	9	9	9	9	9	9	9	9	9	
	Above Dword is repeated a total of 30 times. HTDP										
-	D11.6(CBh)-		D18.6(D2h)-			D29.6(DDh)-			D6.4(86h)+		
	1101	0001	1001	0011	0110	1011	1001	1001	1001	0010	-
	D	1	9	3	6	B	9	9	9	2	
	CRC										
-	K28.3(7Ch)-		D21.5(B5h)+			D21.6(D5h)+			D21.6(D5h)+		
	0011	1100	1110	1010	1010	1010	1001	1010	1010	0110	+
	3	C	E	A	A	A	9	A	A	6	
	EOFp										
+	K28.3(7Ch)+		D21.5(B5h)-			D24.2(58h)-			D24.2(58h)+		
	1100	0011	0010	1010	1010	1100	1101	0100	1100	0101	-
	C	3	2	A	A	C	D	4	C	5	
	WTRMp										
-	K28.3(7Ch)-		D21.5(B5h)+			D24.2(58h)+			D24.2(58h)-		
	0011	1100	1110	1010	1010	1100	0001	0111	0011	0101	+
	3	C	E	A	A	C	1	7	3	5	
	Above 2 Dwords are repeated a total of 2 times. WTRMp (4DW)										

+	K28.3(7Ch)+		D21.4(95h)-			D21.5(B5h)+			D21.5(B5h)+		+
	1100	0011	0010	1010	1101	1010	1010	1010	1010	1010	
	C	3	2	A	D	A	A	A	A	A	
	Above Dword is repeated a total of 2 times. SYNCp (2DW)										
+	K28.3(7Ch)+		D10.5(AAh)-			D25.4(99h)-			D25.4(99h)+		-
	1100	0011	0001	0101	1010	1001	1011	0110	0110	0010	
	C	3	1	5	A	9	B	6	6	2	
	CONTp										
-	K28.3(7Ch)-		D10.5(AAh)+			D25.4(99h)+			D25.4(99h)-		+
	0011	1100	1101	0101	1010	1001	1000	1010	0110	1101	
	3	C	D	5	A	9	8	A	6	D	
	CONTp										
+	D10.2(4Ah)+		D10.2(4Ah)+			D10.2(4Ah)+			D10.2(4Ah)+		+
	0101	0101	0101	0101	0101	0101	0101	0101	0101	0101	
	5	5	5	5	5	5	5	5	5	5	
	Above Dword is repeated a total of 214 times. HFTP (214DW) Junk data/fill										

Total: 2304 Dwords total
2DW ALIGNp
7DW HFTP Junk data/fill
5DW X_RDYp
1DW SOFp
1DW Data FIS Header
256DW SSOP with 2DW ALIGNp at
256DW HTDP (64DW, 64DW, 64DW, 64DW)
512DW LTDP (1DW, 1DW, 509DW, 1DW)
256DW LBP ((1DW,1DW) x 128)
512DW LFSCP (255DW, 1DW, 255DW, 1DW)
256DW HTDP (64DW, 64DW, 64DW, 64DW)
CRC (1DW)
EOFp (1DW)
WTRMp (4DW)
SYNCp (2DW)
CONTp (2DW)
HFTP (214DW) Junk data/fill
ALIGNp (16DW inserted in pairs at 256DW interval)