Proposed Draft **Serial ATA International Organization**

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Title : Gen-III (6Gbps) RiseTime Specification Change

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Document History

Version	Date	Comments
0.72	3/31/2011	Initial release.
0.9	4/13/2011	Updated with Waveform Data – S.Bedwani, John Calvin

1 Introduction

- **Problem Statement:** With the advent of significantly more FR4 signaling loss at 6Gbps, given the I/O congestion at the SATA 6Gbps Host-Controller (Platform-Controller Hub), and given the customer demands for desktop/server usage models requiring 6-inches of FR4-trace from the SATA 6Gbps-Host interface to the SATA connectors, the loss profiles at 6Gbps make it impossible to achieve edge-rates of 68ps.
  - As the rise-time is compromised by longer traces dictated by the above usage models, even with a 35-38ps edge-rate at the component, we are unable to meet the current 68ps iSATA maximum (6Gbps) at the Tx-Compliance point, even for a shorter than required 4-in trace-length.
  - Despite this inability to meet the 68ps Max.RiseTime requirement for 6Gbps iSATA, using optimized signaling de-emphasis techniques, the transmitter circuits under worst-case physical scenarios (process, voltage, temperature, and Impedance combinations) are able to guarantee the minimum signaling levels after the Compliance-Interconnect-Connect (CIC) to satisfy the iSATA requirements of 200mV at the Device Rx-Compliance Point.
  - Assumptions that there is no implementation required use of Tx de-emphasis to meet iSATA signaling criteria at 6Gbps are incorrect, thus enforcement of the max rise-time limit of 68ps for product is not possible for the market required intended usage models.
  - As described, it is important to acknowledge that Tx de-emphasis increased ratios (Transition-Bits to Non-Transition-Bit amplitudes) more than compensate for the attenuated energy, or slower risetime at the compliance points. Thus, de-emphasis levels become the dominating factor required for reducing ISI, optimizing amplitude, thru the various interconnect segments making up the iSATA 6Gbps interface.

Remedy: We are requesting that maximum Tx Risetime iSATA signaling levels at the iSATA Rx-Compliance point for the Device-side be relaxed from 68ps to 80ps

2.0 Specification Engineering Change Notice

2.1 Description of Change

Section 7.2.1 Physical Layer Requirements Tables

Table 31 – Transmitted Signal Requirements

Parameter	Units	Limit	Electrical Specification							Detail Cross-Ref Section	Measurement Cross-Ref Section
			Gen1i	Gen1m	Gen1x	Gen2i	Gen2m	Gen2x	Gen3i		
V_{diffTX}, TX Differential Output Voltage	mVppd	Min	400	400	400	400	400	400	-	7.2.2.2.7	7.4.5
		Min	-	-	-	-	-	-	240		7.4.3
		Nom	500		-	-			-		7.4.5
		Max	600		1600	700		1600	-		
		Max	-		-	-		-	900		7.4.3
UI_{VminTX}, TX Minimum Voltage Measurement Interval	UI		0.45-0.55		0.5	0.45-0.55		0.5	-	7.2.2.2.8	7.4.5
			-		-	-		-	0.50		7.4.3.2
$t_{20-80TX}$, TX Rise/Fall Time	ps (UI)	Min 20-80%	100 (.15)		67 (.10)	67 (.20)			33 (0.20)	7.2.2.2.9	7.4.4
		Max 20-80%	273 (.41)		273 (.41)	136 (.41)			~~68 (0.41)~~ 80		
t_{skewTX}, TX Differential Skew	ps	Max	20			20		15	20	7.2.2.2.10	7.4.15
$V_{cm,acTX}$, TX AC Common Mode Voltage	mVp-p	Max	-			50		-	-	7.2.2.2.11	7.4.20

Additional Details & Background Material

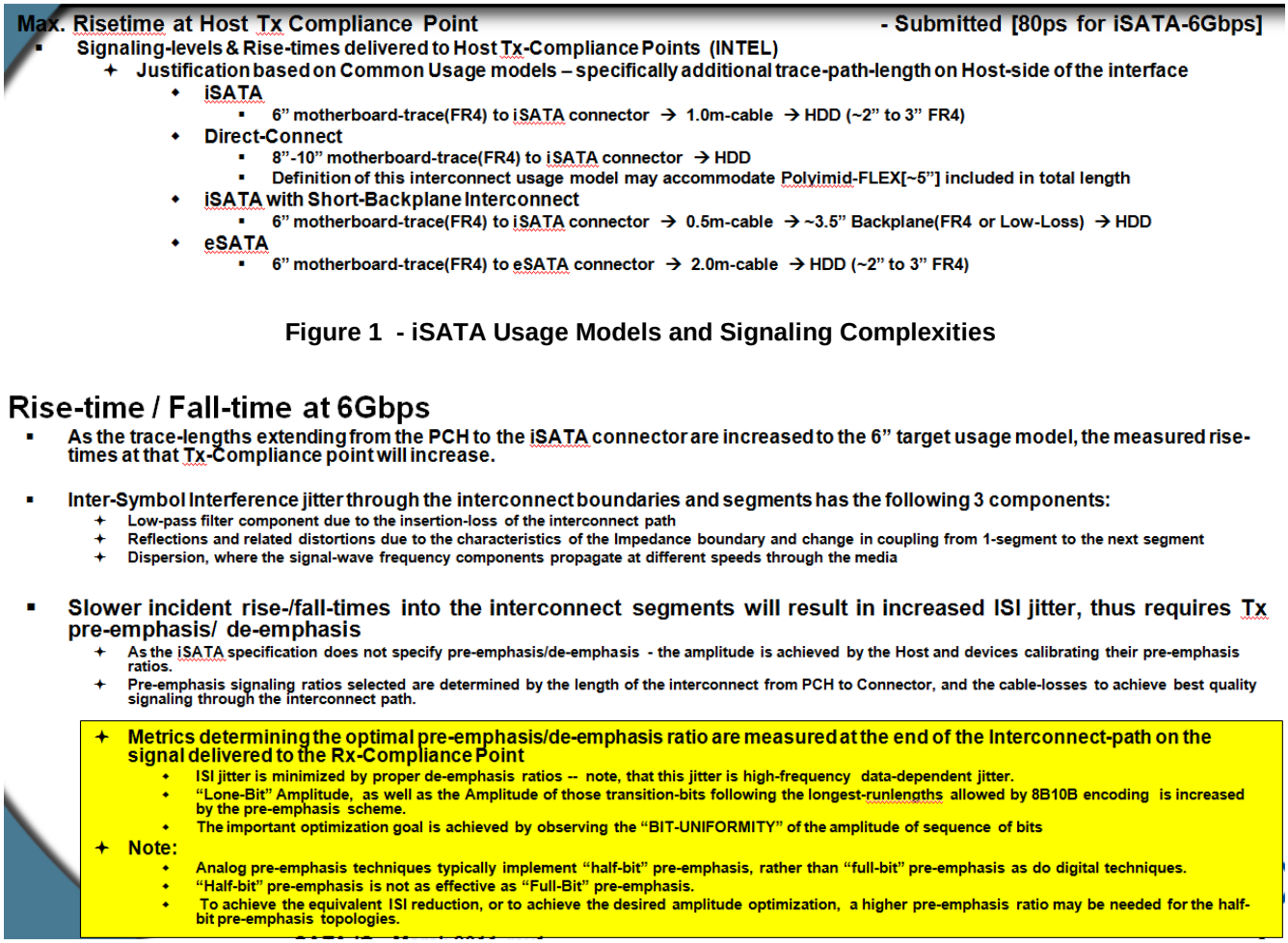

Figure 1 - iSATA Usage Models and Signaling Complexities

Rise-time / Fall-time at 6Gbps

- As the trace-lengths extending from the PCH to the iSATA connector are increased to the 6" target usage model, the measured rise-times at that Tx-Compliance point will increase.
- Inter-Symbol Interference jitter through the interconnect boundaries and segments has the following 3 components:
  - Low-pass filter component due to the insertion-loss of the interconnect path
  - Reflections and related distortions due to the characteristics of the Impedance boundary and change in coupling from 1-segment to the next segment
  - Dispersion, where the signal-wave frequency components propagate at different speeds through the media
- Slower incident rise-/fall-times into the interconnect segments will result in increased ISI jitter, thus requires Tx pre-emphasis/ de-emphasis
  - As the iSATA specification does not specify pre-emphasis/de-emphasis - the amplitude is achieved by the Host and devices calibrating their pre-emphasis ratios.
  - Pre-emphasis signaling ratios selected are determined by the length of the interconnect from PCH to Connector, and the cable-losses to achieve best quality signaling through the interconnect path.
  - Metrics determining the optimal pre-emphasis/de-emphasis ratio are measured at the end of the Interconnect-path on the signal delivered to the Rx-Compliance Point
    - ISI jitter is minimized by proper de-emphasis ratios -- note, that this jitter is high-frequency data-dependent jitter.
    - "Lone-Bit" Amplitude, as well as the Amplitude of those transition-bits following the longest-runlengths allowed by 8B10B encoding is increased by the pre-emphasis scheme.
    - The important optimization goal is achieved by observing the "BIT-UNIFORMITY" of the amplitude of sequence of bits
  - Note:
    - Analog pre-emphasis techniques typically implement "half-bit" pre-emphasis, rather than "full-bit" pre-emphasis as do digital techniques.
    - "Half-bit" pre-emphasis is not as effective as "Full-Bit" pre-emphasis.
    - To achieve the equivalent ISI reduction, or to achieve the desired amplitude optimization, a higher pre-emphasis ratio may be needed for the half-bit pre-emphasis topologies.

Board Name	Speed	VT Corner	Pattern	Port	Cable	BoardZ	Trace Length	RiseTime_Max	FallTime_Max
Rose City	6 Gbps	Slow	LFTP	0	0m	LowZ	4044 MIL	77.68	75.5
Meridian	6 Gbps	Low	LFTP	0	0m	LowZ	5997MIL	77.21	76.92

Figure 2 - Illustrates "Bit-Uniformity" Adjustment - De-Emphasis Optimization minimizing ISI

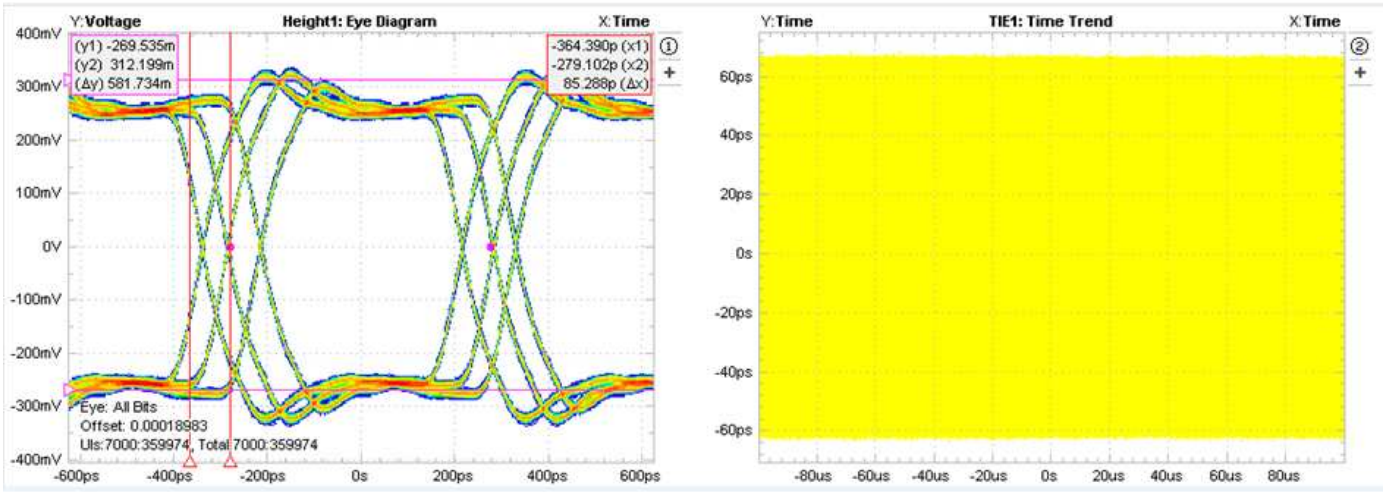

Figure 3 - 6Gbps LFTP Waveform 6-in

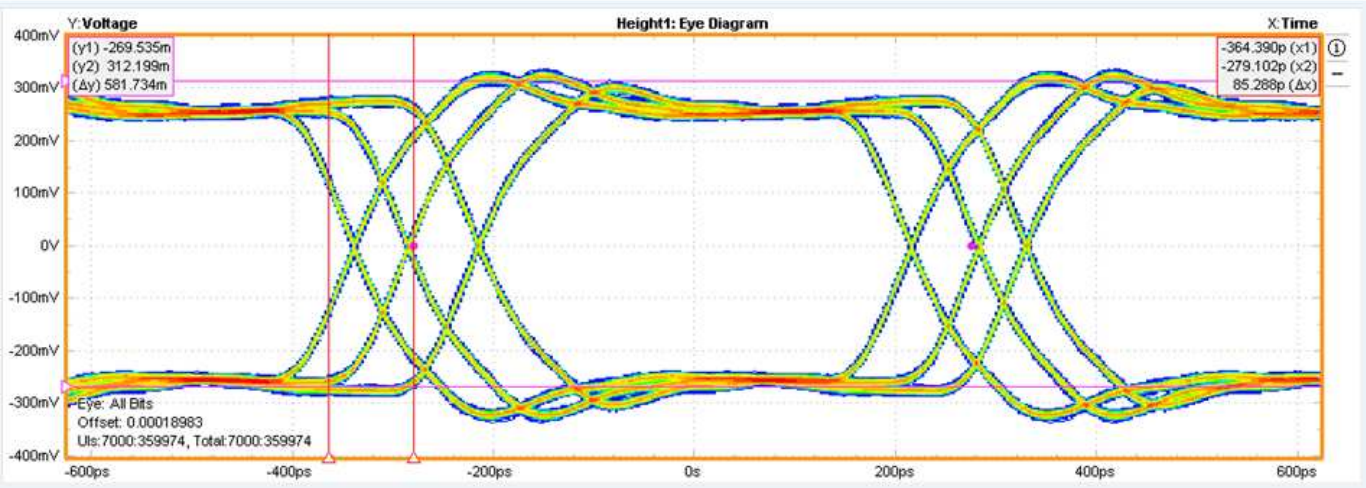

Figure 4 – 6Gbps LFTP Waveform 6-in (Zoom)

Measurement Results

Description	Mean	Std Dev	Max	Min	p-p	Population	Max-cc	Min-cc
TIE1, Math1	-420.83fs	50.796ps	68.518ps	-63.909ps	132.43ps	359614	128.54ps	-74.571ps
Current Acquisition	-420.83fs	50.796ps	68.518ps	-63.909ps	132.43ps	359614	128.54ps	-74.571ps
Height1, Math1	467.07mV	0.0000V	467.07mV	467.07mV	0.0000V	1	0.0000V	0.0000V
Current Acquisition	467.07mV	0.0000V	467.07mV	467.07mV	0.0000V	1	0.0000V	0.0000V
TJ@BER1, Math1	135.60ps	0.0000s	135.60ps	135.60ps	0.0000s	1	0.0000s	0.0000s
Current Acquisition	135.60ps	0.0000s	135.60ps	135.60ps	0.0000s	1	0.0000s	0.0000s
Rise Time1, Math1	70.321ps	1.8419ps	77.127ps	64.309ps	12.819ps	179806	10.128ps	-8.7025ps
Current Acquisition	70.321ps	1.8419ps	77.127ps	64.309ps	12.819ps	179806	10.128ps	-8.7025ps
Fall Time1, Math1	70.216ps	1.5676ps	76.373ps	63.983ps	12.390ps	179806	8.8641ps	-8.7888ps
Current Acquisition	70.216ps	1.5676ps	76.373ps	63.983ps	12.390ps	179806	8.8641ps	-8.7888ps
Cycle Pk-Pk1, Math1	626.17mV	11.075mV	665.60mV	596.00mV	69.600mV	359972	37.600mV	-42.400mV
Current Acquisition	626.17mV	11.075mV	665.60mV	596.00mV	69.600mV	359972	37.600mV	-42.400mV
Rise Slew Rate1, Math1	4.3300V/ns	113.17mV/ns	4.7315V/ns	3.9451V/ns	786.38mV/ns	179987	526.73mV/ns	-634.10mV/ns
Current Acquisition	4.3300V/ns	113.17mV/ns	4.7315V/ns	3.9451V/ns	786.38mV/ns	179987	526.73mV/ns	-634.10mV/ns
Fall Slew Rate1, Math1	-4.3356V/ns	96.532mV/ns	-3.9841V/ns	-4.7555V/ns	771.49mV/ns	179987	553.07mV/ns	-537.78mV/ns
Current Acquisition	-4.3356V/ns	96.532mV/ns	-3.9841V/ns	-4.7555V/ns	771.49mV/ns	179987	553.07mV/ns	-537.78mV/ns

Figure 5 - 6Gbps LFTP Waveform 6-in (Measurement Results)