Proposed **Serial ATA**

Draft **International Organization**

Version 0

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ECN067v0_SATA31_PMSignatureforSWReset_SetDeviceBitsFISDescription_NCQQueueMgmtCommandResponse_GSCRTypoError

Title: Port Multiplier Signature for Software Reset, Description of I field of Set Device Bits FIS, NCQ Queue Management Subcommand response, Typo Error in GSCR Reference

Proposed correction to Serial ATA Revision 3.1

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Document History

Version	Date	Comments
0	1/14/2013	Initial draft

1 Introduction

ITEM A: Port Multiplier Signature for Software Reset

There is an error in the description paragraph of Software Reset (Page# 609, Section# 13.16.2.2).

The Port Multiplier is supposed to respond with Register Device to Host FIS, but in the description it is mistakenly written as “Register Host to Device FIS”. The portion with issue is highlighted in the SATA Gold 3.1 Specification’s snippet pasted below:

13.16.2.2 Software Reset

When the host issues a software reset to the control port, two Register Host to Device FISes are sent to the control port as a result. In the first Register Host to Device FIS, the SRST bit in the Device Control register is set to one. In the second Register Host to Device FIS, the SRST bit in the Device Control register is cleared to zero.

Upon receiving the Register Host to Device FIS with the SRST bit asserted, the Port Multiplier shall wait for the Register Host to Device FIS that has the SRST bit cleared to zero before issuing a Register Device to Host FIS with the Port Multiplier signature to the host. The Port Multiplier’s behavior shall be consistent with the Software reset protocol described in section 11.3. The values to be placed in the Register Host to Device FIS are listed in Figure 278.

Register	7	6	5	4	3	2	1	0
Error	00h							
Count(7:0)	01h							
Count(15:8)	00h							
LBA(7:0)	01h							
LBA(31:24)	00h							
LBA(15:8)	69h							
LBA(39:32)	00h							
LBA(23:16	96h							
LBA(47:40)	00h							
Device	na							
Status	BSY	DRDY	DF	na	DRQ	0	0	ERR

Figure 278 – Software reset to control port result values

ITEM B: Description of I field of Set Device Bits FIS

The error is in the description of I bit of Set Device Bits FIS (Page# 420, Section# 10.3.6).

The names of the Tagged Queued Commands are incorrect, as shown in the highlighted region in snippet below:

10.3.6 Set Device Bits - Device to Host FIS

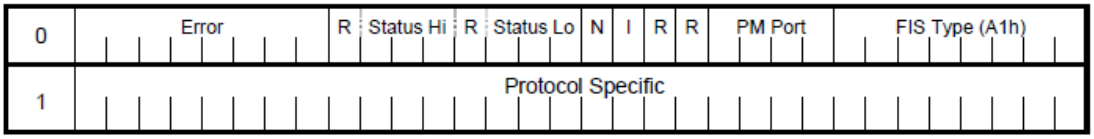

Figure 215 – Set Device Bits - Device to Host FIS layout

Field Definitions

FIS Type – Set to a value of A1h. Defines the rest of the FIS fields. Defines the length of the FIS as two Dwords.

I – Interrupt Bit. This bit signals the host adapter to enter an interrupt pending state. If the host is executing tagged queued commands (READ FPDMA QUEUED, WRITE FPDMA QUEUED) with the device, the host should only enter the interrupt pending state if both the BSY bit and the DRQ bit in the shadow Status register are zero when the frame is received. If the host is executing native queued commands (READ FPDMA QUEUED, WRITE FPDMA QUEUED, NCQ QUEUE MANAGEMENT, RECEIVE FPDMA QUEUED, or SEND FPDMA QUEUED) with the device, the interrupt pending state is entered regardless of the current state of the BSY bit or the DRQ bit in the shadow Status register. Devices shall not modify the behavior of this bit based on the state of the nIEN bit received in Register Host to Device FISes.

ITEM C: Abort NCQ Subcommand response

There is an error in the contents of the response values to the ABORT NCQ QUEUE Subcommand (Page# 557, Section# 13.6.5.1.1) and Deadline Handling Subcommand(Page# 560, Section# 13.6.5.1.3.1).

There is a contradiction between the value of Status Field shown in the Figure 235 and its description. Similar issue is with the Figure 239 and the description of its fields. The conflicting regions are highlighted in the snippets below:

13.6.5.1.1 Success Outputs

If a supported Abort Type parameter is specified, then the device shall indicate success, even if the command results in no commands being aborted.

When an Abort NCQ Queue command completes successfully, a Set Device Bits FIS shall be sent to the host to complete the Abort subcommand and commands that were aborted as a consequence of the Abort subcommand by setting the ACT bits for those commands to one. This SDB FIS may also indicate other completed commands.

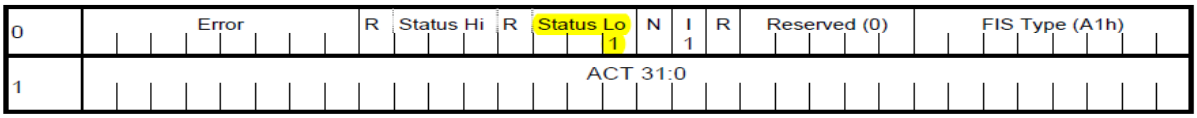

Figure 235 – NCQ QUEUE MANAGEMENT, Abort NCQ Queue - Successful completion

ACT	The ACT field of the Set Device Bits FIS communicates completion notification for each of up to 32 commands. The field is bit-significant and the device sets bit positions to one for each command tag it is indicating completion notification for. The device may set more than one bit to one if it is explicitly aggregating successful status returns. The device shall set the appropriate bit to one for each queued command that has been aborted, and shall set to one the bit associated with the TAG value for the Abort NCQ Queue command.
Error Status	The Error register shall contain 00h. As defined in 10.3.6. The ERR bit shall be cleared to zero indicating successful command completion. Bit 4 may be set to one.

13.6.5.1.3.1 Success Outputs

If this Deadline Handling Subcommand command is supported, the device shall return command completed with no error.

When an Deadline Handling Subcommand command completes successfully, a Set Device Bits FIS shall be sent to the host to complete the Deadline Handling subcommand. This SDB FIS may also indicate other completed commands.

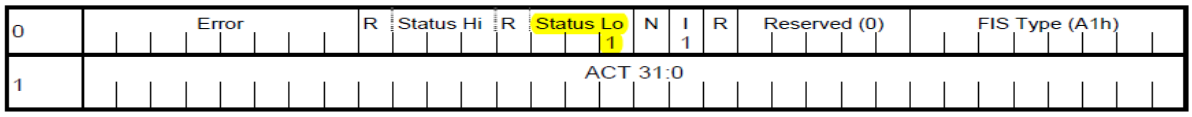

Figure 239 – NCQ QUEUE MANAGEMENT, Deadline Handling - Successful completion

ACT	The ACT field of the Set Device Bits FIS communicates completion notification for each of up to 32 commands. The field is bit-significant and the device sets bit positions to one for each command tag it is indicating completion notification for. The device may set more than one bit to one if it is explicitly aggregating successful status returns. The device shall set to one the bit associated with the TAG value for the Deadline Handling command.
Error Status	The Error register shall contain 00h. As defined in 10.3.6. The ERR bit shall be cleared to zero indicating successful command completion. Bit 4 may be set to one.

ITEM D: Typo in GSCR reference

There is a typo error in Page# 640, Section# 16.3.3.9. The term GSCR[64] is mistakenly written as GCSR[64]. Please see the snippet below for reference.

16.3.3.9 BIST Support

A Port Multiplier may optionally support BIST. A Port Multiplier that supports BIST shall only support BIST in a point-to-point manner. A Port Multiplier that supports BIST shall not propagate a BIST Activate FIS received on one port over another port. The host determines that a Port Multiplier supports BIST by checking GCSR[64], defined in section 16.4.1.3.

2 Summary of the problem

ITEM A: Port Multiplier Signature for Software Reset

The highlighted region demonstrates the contents of Port Multiplier Signature that comes in a Register Device to Host FIS. This is mistakenly written as Register Host to Device FIS in specs.

ITEM B: Description of I field of Set Device Bits FIS

The highlighted region contains the wrong list of commands in the said protocol type. The List of the commands that are mentioned for “tagged queued commands” comes under the category of Native Queued Commands.

ITEM C: Abort NCQ Subcommand response

The content of the Status field shown in the Figures is in conflict with the description of the field. The description of the field recommends the value of ‘0’, while the figure demonstrates the value as ‘1’.

ITEM D: Typo in GSCR reference

This is a typo error. GSCR is written as GCSR

3 Proposed corrections

ITEM A: Port Multiplier Signature for Software Reset

13.16.2.2 Software Reset

When the host issues a software reset to the control port, two Register Host to Device FISes are sent to the control port as a result. In the first Register Host to Device FIS, the SRST bit in the Device Control register is set to one. In the second Register Host to Device FIS, the SRST bit in the Device Control register is cleared to zero.

Upon receiving the Register Host to Device FIS with the SRST bit asserted, the Port Multiplier shall wait for the Register Host to Device FIS that has the SRST bit cleared to zero before issuing a Register Device to Host FIS with the Port Multiplier signature to the host. The Port Multiplier's behavior shall be consistent with the Software reset protocol described in section 11.3. The values to be placed in the ~~Register Host to Device FIS~~ Register Device to Host FIS are listed in Figure 278.

ITEM B: Description of I field of Set Device Bits FIS

10.3.6 Set Device Bits - Device to Host FIS

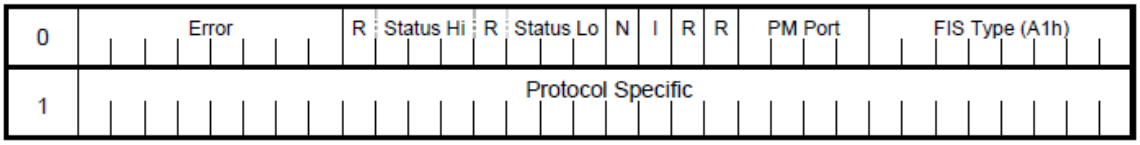

Figure 215 – Set Device Bits - Device to Host FIS layout

Field Definitions

FIS Type – Set to a value of A1h. Defines the rest of the FIS fields. Defines the length of the FIS as two Dwords.

I – Interrupt Bit. This bit signals the host adapter to enter an interrupt pending state. If the host is executing tagged queued commands ~~(READ FPDMA QUEUED, WRITE FPDMA QUEUED)~~ (READ DMA QUEUED, WRITE DMA QUEUED , READ DMA QUEUED EXT , WRITE DMA QUEUED EXT or WRITE DMA QUEUED FUA EXT) with the device, the host should only enter the interrupt pending state if both the BSY bit and the DRQ bit in the shadow Status register are zero when the frame is received. If the host is executing native queued commands (READ FPDMA QUEUED, WRITE FPDMA QUEUED, NCQ QUEUE MANAGEMENT, RECEIVE FPDMA QUEUED, or SEND FPDMA QUEUED) with the device, the interrupt pending state is entered regardless of the current state of the BSY bit or the DRQ bit in the shadow Status register. Devices shall not modify the behavior of this bit based on the state of the nIEN bit received in Register Host to Device FISes.

ITEM C: Abort NCQ Subcommand response

13.6.5.1.1 Success Outputs

If a supported Abort Type parameter is specified, then the device shall indicate success, even if the command results in no commands being aborted.

When an Abort NCQ Queue command completes successfully, a Set Device Bits FIS shall be sent to the host to complete the Abort subcommand and commands that were aborted as a consequence of the Abort subcommand by setting the ACT bits for those commands to one. This SDB FIS may also indicate other completed commands.

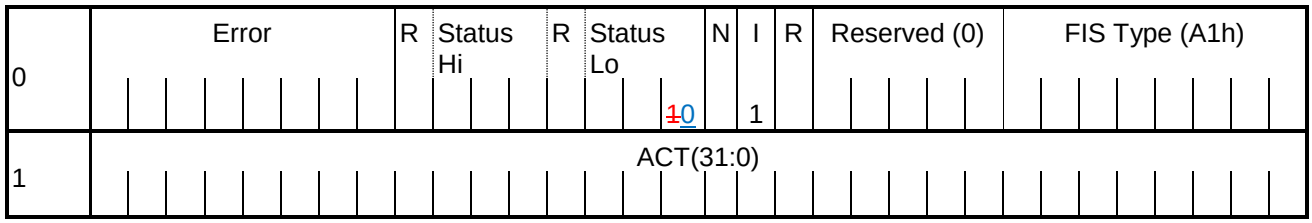

Figure 235 – NCQ QUEUE MANAGEMENT, Abort NCQ Queue - Successful completion

13.6.5.1.3.1 Success Outputs
If this Deadline Handling Subcommand command is supported, the device shall return command completed with no error.

When an Deadline Handling Subcommand command completes successfully, a Set Device Bits FIS shall be sent to the host to complete the Deadline Handling subcommand. This SDB FIS may also indicate other completed commands.

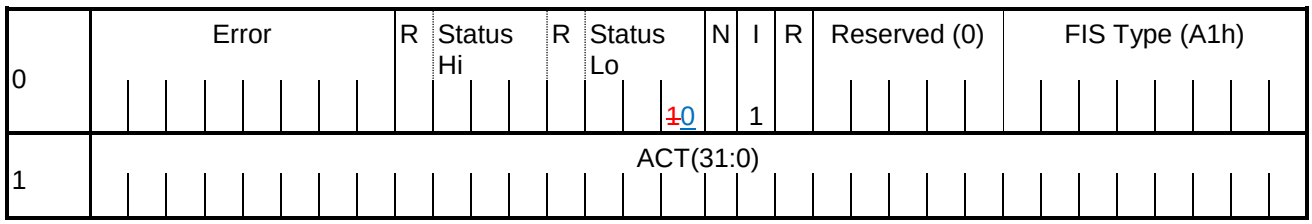

Figure 239 – NCQ QUEUE MANAGEMENT, Deadline Handling- Successful completion

ITEM D: Typo in GSCR reference

16.3.3.9 BIST Support
A Port Multiplier may optionally support BIST. A Port Multiplier that supports BIST shall only support BIST in a point-to-point manner. A Port Multiplier that supports BIST shall not propagate a BIST Activate FIS received on one port over another port. The host determines that a Port

Multiplier supports BIST by checking ~~GCSR~~ GSCR [64], defined in section 16.4.1.3.