Proposed Draft **Serial ATA International Organization**

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ECN068v2_SATA31_Device_Sleep_Voltage_Spec_Adjustment

Title: Device Sleep Voltage Spec Adjustment

Sponsors: SanDisk, Intel

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Document History

Version	Date	Comments
00	02/21/2013	Initial release.
01	03/27/2013	Changed 2.1V to VHin maximum value in IHVAssert description (Table zz) Changed uSSD to MicroSSD in Tables yy and zz.
02	05/01/2013	Ratified

1 Introduction

This ECN modifies the electrical specification for host input voltages for DEVSLP for the M.2 and uSSD form factors, in order to be better compatible with lower power hosts. The max host input tolerance and asserted voltage are adjusted to be 1.89 V (1.8 V + 5%), from the currently specified max of 2.1 V.

2 Technical Specification Changes

The following additions are based on the content of Serial ATA Technical Proposal #038, Device Sleep, 24-October-2011. Proposed additions are marked in blue. Proposed deletions are marked in ~~red~~. Black text is original text.

3 [8.new.2] DEVSLP Signal Electrical Characteristics

The DEVSLP signal shall be implemented with the electrical constraints in table yy and table zz. DEVSLP is a level triggered signal, asserted high.

The device shall tolerate the DEVSLP signal being shorted to ground. The device shall tolerate a no-connect floating DEVSLP signal.

Figure yy is an example of a DEVSLP implementation for illustrative purposes. Note that the host should not rely on particular device resistor values.

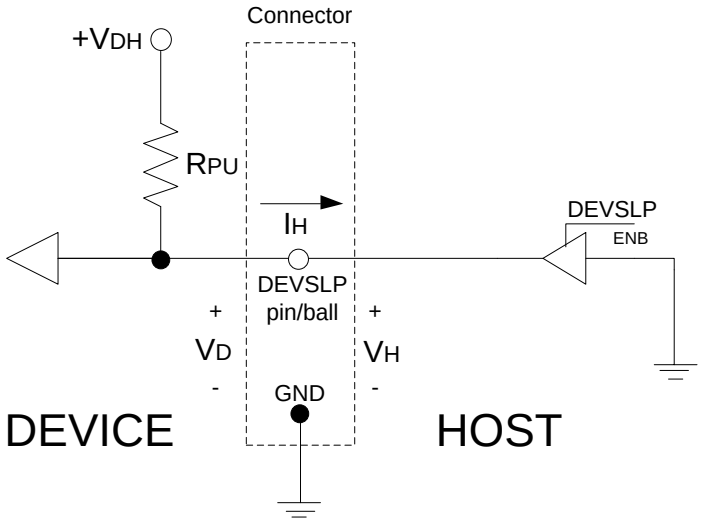

Figure yy – Example DEVSLP electrical block diagram

All voltage references in table yy and table zz are to ground pin on the host connector.
All voltages and currents in table yy and table zz are measured at DEVSLP pin on the host connector.

~~Table yy – Device side DEVSLP Electrical Parameters~~

~~Parameter~~	~~Min value~~	~~Max value~~	~~Description & Conditions~~
~~V_{DIn}~~	~~-0.5 V~~	~~3.6 V~~	~~Tolerated input voltage~~
~~$V_{HAssert}$~~		~~2.1 V~~	~~Voltage presented to host when signal not driven low. Value specified for all allowable $I_{HAssert}$~~
~~$I_{HNegate}$~~		~~100 uA~~	~~Device current delivered to host when host driving signal low. Value specified at $V_{HNegate}$ voltage of 0 V~~

~~Table zz – Host side DEVSLP Electrical Parameters~~

~~Parameter~~	~~Min value~~	~~Max value~~	~~Description & Conditions~~
~~V_{HIn}~~	~~-0.5 V~~	~~2.1 V~~	~~Tolerated input voltage~~
~~$I_{HAssert}$~~	~~-1 uA~~	~~10 uA~~	~~Host leakage current when signal not driven. Value specified for all voltages between 0 V and $V_{HAssert}$ of 2.1 V~~
~~$V_{HNegate}$~~	~~0 V~~	~~0.225 V~~	~~Host voltage presented to device when the signal driven low Value specified for all allowable $I_{HNegate}$~~

Table yy – Device side DEVSLP Electrical Parameters

		SATA, mSATA		M.2, MicroSSD	
Parameter	**Description & Conditions**	**Min value**	**Max value**	**Min value**	**Max value**
V_{DIn}	Tolerated input voltage	-0.5 V	3.6 V	-0.5 V	3.6 V
$V_{HAssert}$	Voltage presented to host when signal not driven low. Value specified for all allowable $I_{HAssert}$		2.1 V		~~2.1~~1.89 V
$I_{HNegate}$	Device current delivered to host when host driving signal low. Value specified at $V_{HNegate}$ voltage of 0 V		100 uA		100 uA

Table zz – Host side DEVSLP Electrical Parameters

		SATA, mSATA		M.2, MicroSSD	
Parameter	**Description & Conditions**	**Min value**	**Max value**	**Min value**	**Max value**
V_{HIn}	Tolerated input voltage	-0.5 V	2.1 V	-0.5 V	~~2.1~~1.89 V
$I_{HAssert}$	Host leakage current when signal not driven. Value specified for all voltages between 0 V and $V_{HAssert}$ of ~~2.1 V~~VHin maximum value.	-1 uA	10 uA	-1 uA	10 uA
$V_{HNegate}$	Host voltage presented to device when the signal driven low. Value specified for all allowable $I_{HNegate}$	0 V	0.225 V	0 V	0.225 V