Proposed Draft

Serial ATA International Organization

Revision 03 05/14/2013

ECN071v3_SATA31_DEVSLP_Bit_Interlock

Title: DEVSLP Bit Interlock Sponsors: SanDisk, Seagate

This is an internal working document of the Serial ATA International Organization. As such, this is not a completed standard and has not been approved. The Serial ATA International Organization may modify the contents at any time. This document is made available for review and comment only.

Permission is granted to the Promoters, Contributors and Adopters of the Serial ATA International Organization to reproduce this document for the purposes of evolving the technical content for internal use only without further permission provided this notice is included. All other rights are reserved and may be covered by one or more Non Disclosure Agreements including the Serial ATA International Organization participant agreements. Any commercial or for-profit replication or republication is prohibited. Copyright © 2000 to 2013 Serial ATA International Organization. All rights reserved.

This Draft Specification is NOT the final version of the Specification and is subject to change without notice. A modified, final version of this Specification ("Final Specification") when approved by the Promoters will be made available for download at this Web Site: http://www.sata-io.org.

THIS DRAFT SPECIFICATION IS PROVIDED "AS IS" WITH NO WARRANTIES WHATSOEVER, INCLUDING ANY WARRANTY OF MERCHANTABILITY, NON-INFRINGEMENT, FITNESS FOR ANY PARTICULAR PURPOSE OR ANY WARRANTY OTHERWISE ARISING OUT OF ANY PROPOSAL, SPECIFICATION, OR SAMPLE. Except for the right to download for internal review, no license, express or implied, by estopple or otherwise, to any intellectual property rights is granted or intended hereunder.

THE PROMOTERS DISCLAIM ALL LIABILITY, INCLUDING LIABILITY FOR INFRINGEMENT OF ANY PROPRIETARY RIGHTS, RELATING TO USE OF INFORMATION IN THIS DRAFT SPECIFICATION. THE PROMOTERS DO NOT WARRANT OR REPRESENT THAT SUCH USE WILL NOT INFRINGE SUCH RIGHTS.

THIS DOCUMENT IS AN INTERMEDIATE DRAFT FOR COMMENT ONLY AND IS SUBJECT TO CHANGE WITHOUT NOTICE.

Copyright © 2005 to 2013 Serial ATA International Organization. All rights reserved.

^{*} Other brands and names are the property of their respective owners.

Author Information

Author Name	Company	Email address
Dave Landsman	SanDisk	dave.landsman@sandisk.com
Jim Hatfield	Seagate	james.c.hatfield@seagate.com

Workgroup Chair Information

Workgroup (Phy, Digital, etc)	Chairperson Name	Email address
Digital	Jim Hatfield	james.c.hatfield@seagate.com

Document History

Version	Date	Comments	
00	04/24/2013	Initial release.	
01	05/13/2013	Updated to reflect SATA 3.2 draft 17	
02	05/13/2013	Updated to reflect SATA 3.2 draft 20	
03	05/14/2013	Member review	

1 Introduction

This ECN clarifies the interlocking behavior of bits associated with the Device Sleep feature. The ECN is intended as editorial only.

2 Technical Specification Changes

The following additions are based on the content of:

- a) Serial ATA Specification Rev. 3.1 Gold;
- b) TPR038 Device sleep;
- c) TPR044 Synch with ACS-3; and
- d) TPR046 Transitional energy reporting.

Proposed additions are marked in <u>blue</u>. Proposed deletions are marked in <u>red</u>. Black text is original text.

2.1.1.1.1 [Editor's note: 13.7.9.2.22] DEVICE SLEEP SUPPORTED bit

If the DEVICE SLEEP SUPPORTED bit is set to one, then:

- a) the device supports the Device Sleep feature:
- b) the device shall support the Identify Device data log; and
- c) the DEVSLP TIMING VARIABLES <u>SUPPORTED</u> field-VALID bit <u>(see Editor's note 13.7.7.4.new)</u> shall be set to one 1.

If the DEVICE SLEEP SUPPORTED bit is cleared to zero, then:

a) the device does not support the Device Sleep feature.

IDENTIFY DEVICE Word 78 bit 8 is a copy of this field.

Note: If the DEVICE SLEEP SUPPORTED bit is cleared to zero, then the host ignores the DEVSLEEP TO REDUCEDPWRSTATE CAPABILITY SUPPORTED bit and the DEVSLET TIMING VARIABLES SUPPORTED bit.

2.1.1.1.2 [Editor's note: 13.7.9.2.23] DEVSLEEP_TO_REDUCEDPWRSTATE CAPABILITY SUPPORTED bit

If the DEVSLEEP_TO_REDUCEDPWRSTATE CAPABILITY SUPPORTED bit is set to one, then:

- a) the device supports remembering whether it was in Partial or Slumber after detection of assertion, and subsequent detection of negation, of DEVSLP; and
- b) the DEVICE SLEEP SUPPORTED bit shall be set to one.

If the DEVSLEEP_TO_REDUCEDPWRSTATE CAPABILITY SUPPORTED bit is cleared to zero, then the device does not support remembering whether it was in Partial or Slumber after detection of assertion, and subsequent detection of negation, of DEVSLP.

IDENTIFY	DEVICE	Word 77	bit 7	is a	сору	of this	field.

Editor's note: TPR038 SATA 31 Device sleep added DEVSLP Timing Variables.

Editor's note: TPR044v17 SATA 31 Transitional Energy Reporting changed offset from hex to decimal.

Editor's note: TPR046v17 SATA 31 Transitional Energy Reporting added DEVSLP SUPPORTED.

2.1.1.1 [editor's note: 13.7.7.1] Serial ATA Settings (page 08h)

Table 95 - Serial ATA (page 08h)

Offset	Type	Content	
4855	QWord	DEVSLP TIMING VARIABLES	
		Bit	Meaning
		63	DEVSLP TIMING VARIABLES SUPPORTED (see TPR046 13.7.7.4.new)
		62:16	Reserved
		15:8	DEVSLEEP EXIT TIMEOUT (DETO) (see TPR044 13.7.7.4.1)
		7:5	Reserved
		4:0	MINIMUM DEVSLP ASSERTION TIME (MDAT) (see TPR 044 13.7.7.4.2)

Editor's note: TPR044 added 13.7.7.4 DEVSLP TIMING VARIABLES and TPR046 added DEVSLP SUPPORTED bit.

2.1.1.2 [Editor's note: 13.7.7.4] DEVSLP TIMING VARIABLES

2.1.1.2.1 [Editor's note: 13.7.7.4.new] DEVSLP TIMING VARIABLES SUPPORTED bit

If the DEVSLP <u>TIMING VARIABLES</u> SUPPORTED bit is set to one, then the device supports DEVSLP TIMING VARIABLES.