

**Proposed  
Draft**

**Serial ATA  
International Organization**

**Version 2  
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**Serial ATA Revision 3.2 ECN074  
Title : SATA Express Pin Sequencing**

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## Document History

Version	Date	Comments
0	September 3, 2013	Initial release.
1	September 4, 2013	CabCon meeting updates
2	September 25, 2013	ECN C101 changed to ECN074 for member review

# **1 Introduction**

## **1.1 Problem Statement**

The pin sequencing listed in Table 31 is inconsistent with the physical dimension of the pins in Figure 131 and Figure 132.

The standard SATA device plug Figure 32 section lines B and D are reversed relative to the section views found in Figure 33.

The pin sequencing listed in Table 32 is inconsistent with the physical dimension of the pins in Figure 135, Figure 136, and Figure 137.

## **1.2 Solution Summary**

Update Table 31 and Table 32 to match physical pin sequencing.

Swap section line B and D in Figure 32.

## **1.3 Background (optional)**

## 2 Technical Specification Changes

### 2.1 <Title of section being changed>

[editor note: Existing text is black. New text is marked as underlined in blue color. Material to be deleted ~~is red with strikethrough markings.~~ ]

### 2.2 <6.10> SATA Express connector

#### 2.2.1 <6.10.5> SATA Express signal list

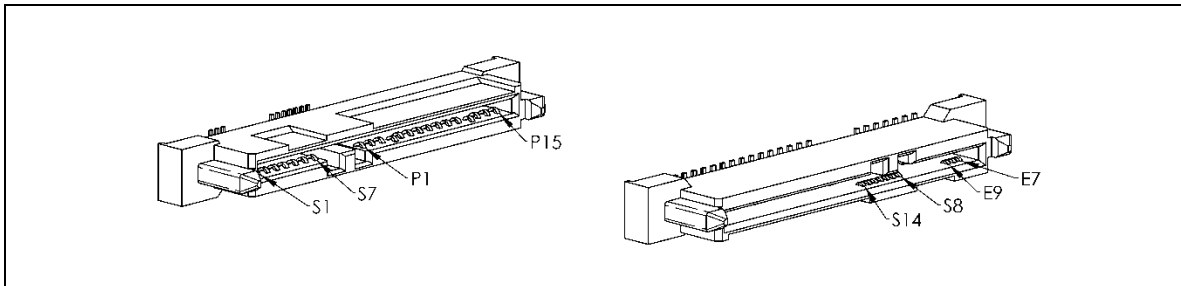


Figure 128 – SATA Express pinout for host receptacle connectors

Table 30 – SATA Express signal pin list for host receptacle and device plug connectors

Pin position	Name <sup>a</sup>	Signal Description <sup>a</sup>	Usage	Signal Direction	Mating Sequence <sup>c</sup>
S1	GND	Ground	PCIe/SATA		Second
S2	PETp0/A+	PCIe Lane 0 Host Tx / SATA Tx pair <sup>b</sup>	PCIe/SATA	Host Output	Third
S3	PETn0/A-				
S4	GND	Ground	PCIe/SATA		Second
S5	PERn0/B-	PCIe Lane 0 Host Rx / SATA Rx pair <sup>b</sup>	PCIe/SATA	Input to Host	Third
S6	PERp0/B+				
S7	GND	Ground	PCIe/SATA		Second
S8	GND	Ground	PCIe only		Second
S9	PETp1	PCIe Lane 1 Host Tx pair	PCIe only	Host Output	Third
S10	PETn1				
S11	GND	Ground	PCIe only		Second
S12	PERn1	PCIe Lane 1 Host Rx pair	PCIe only	Input to Host	Third
S13	PERp1				
S14	GND	Ground	PCIe only		Second

<sup>a</sup> The "Name" and "Signal Description" columns are relative to the host, as defined by each protocol specification.

<sup>b</sup> Muxing of the PCIe and SATA lanes is required for the host. Only the PCIe Lane 0 is required to mux with the SATA lane for the host receptacle connector since the client SATA device has only a single lane. For the host plug connector, both PCIe lanes (0 and 1) shall be muxed with SATA. This allows connections to two separate SATA devices via independent cables.

<sup>c</sup> Mating sequence defined here is for the host receptacle connector and device plug connector. The mating sequence for the cabled case is defined in 6.10.10.

**Table 31 – SATA Express power pin list for host receptacle and device plug connectors**

Pin position	Name <sup>a</sup>	Signal Description <sup>a</sup>	Usage	Signal Direction	Mating Sequence <sup>c</sup>
P1	Reserved <sup>d</sup>	Reserved for future use	PCIe/SATA		Third
P2	PERST# <sup>d</sup>	PCIe reset	PCIe only	Host Output	<del>Second</del> Third
P3	CLKREQ# / DEVSLP <sup>d</sup>	L1 PM substate / Device sleep	PCIe/SATA	Host Output	<del>Third</del> Second
P4	IFDet <sup>e</sup>	Interface (PCIe/SATA) detect	PCIe/SATA	Input to Host	First
P5	GND	Ground	PCIe/SATA		Second
P6	GND	Ground	PCIe/SATA		Second
P7	V5 <sup>b</sup>	5 V power, pre-charge	PCIe/SATA	Host Output	Second
P8	V5 <sup>b</sup>		PCIe/SATA	Host Output	Third
P9	V5 <sup>b</sup>		PCIe/SATA	Host Output	Third
P10	GND	Ground	PCIe/SATA		Second
P11	DAS/DSS	Device Activity Signal / Disable Staggered Spinup	SATA only	Bi-directional	Third
P12	GND	Ground	PCIe/SATA		First
P13	V12 <sup>b</sup>	12 V power, pre-charge	PCIe/SATA	Host Output	Second
P14	V12 <sup>b</sup>	12 V power	PCIe/SATA	Host Output	Third
P15	V12 <sup>b</sup>	12 V power	PCIe/SATA	Host Output	Third
E7	RefClk+ <sup>g</sup>	PCIe common RefClk	PCIe only, optional <sup>f</sup>	Host Output	Third
E8	RefClk- <sup>g</sup>				
E9	ClkDet <sup>h</sup>	PCIe RefClk detect	PCIe only, optional	Input to Host	Second

<sup>a</sup> The "Name" and "Signal Description" columns are relative to the host, as defined by each protocol specification.

<sup>b</sup> The power pins on the PCIe device shall be bused together for each supply voltage, in the same way as defined in the legacy SATA specification.

<sup>c</sup> Mating sequence defined here is for the host receptacle connector and device plug connector. The mating sequence for the cabled case is defined in Editor's note 6.10.10.

<sup>d</sup> Pins P1, P2, and P3 were defined as the 3.3 V pins in previous versions of this specification (i.e., SATA rev 3.1) and have since been retired. Pins P1, P2, and P3 are repurposed to be PERST# and other signals in SATA Express. To avoid damage to a PCIe device, the components that connect to those pins shall be able to tolerate the application of 3.3 V. If CLKREQ#/DEVSLP is not implemented, then P3 should be a no connect.

<sup>e</sup> Pin P4 is a GND in previous revisions of this specification (i.e., SATA rev 3.1). It is named IFDet for interface detect in SATA Express. The detail interface detect mechanism is discussed in Editor's note 7.3.3.

<sup>f</sup> The RefClk pins E7 and E8 are defined following SFF-8639. Support of the common RefClk is optional. Management of system compatibility with PCIe devices requiring the common RefClk is beyond the scope of SATA Express.

<sup>g</sup> For cabled applications, there is no reference clock (RefClk) included in the host cable plug connector (see Editor's note 6.10.10), requiring an SRIS architecture. Requirements associated with the separate RefClk with independent SSC are defined in the PCIe Base Specification 3.0 ECN- Separate RefClk Independent SSC Architecture.

<sup>h</sup> ClkDet (i.e., pin E9) is used by the host to detect the device RefClk type. If a SATA Express device requires the common RefClk, then the device shall ground pin E9. If a SATA Express device supports SRIS, then the device shall not ground pin E9.

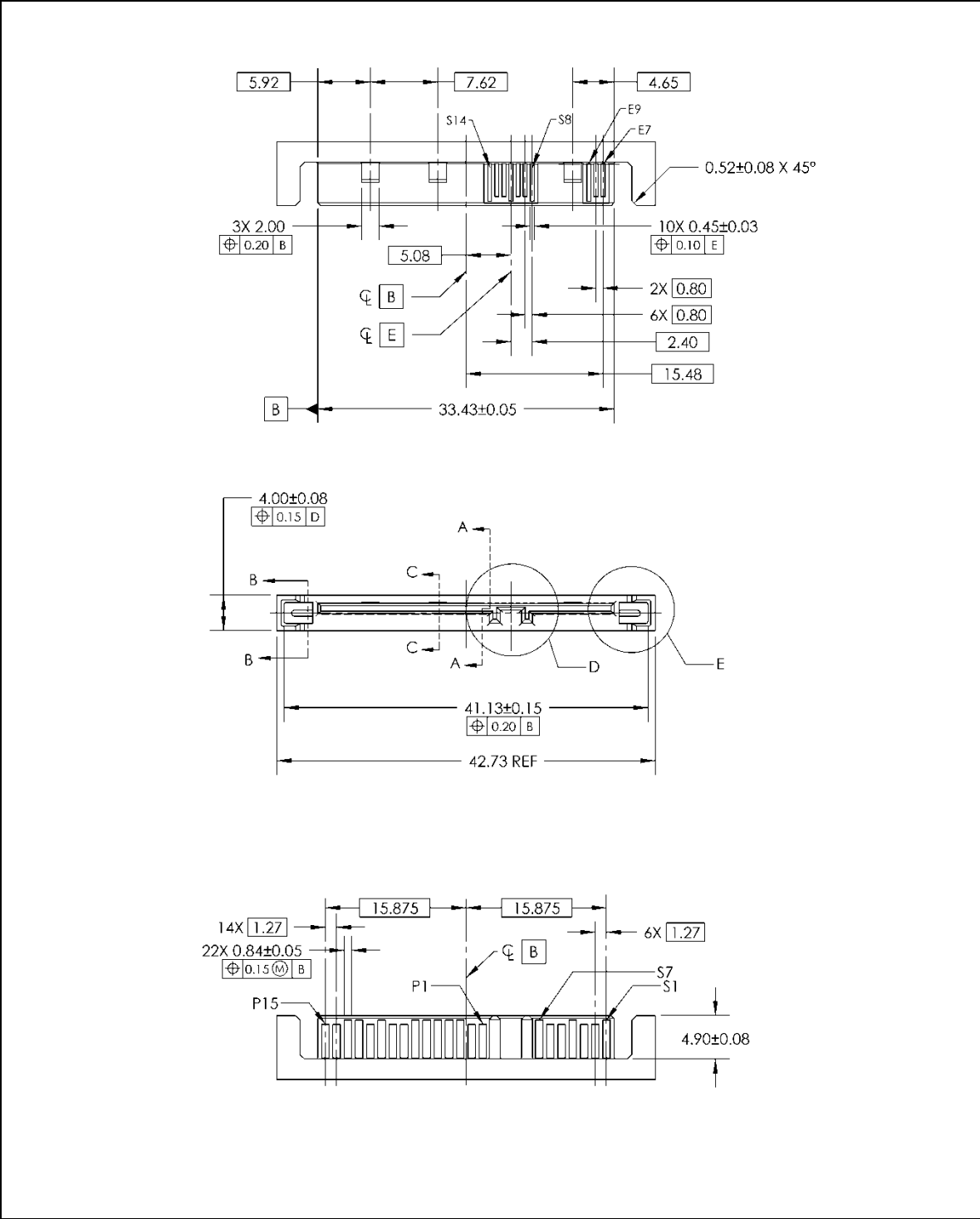


Figure 131 – SATA Express device plug connector drawing  
 (part 1 of 2)

Editor's note: The long pin in section C-C should be dimensioned  $4.40 \pm 0.15$  LONG CONTACT as seen in Figure 33.

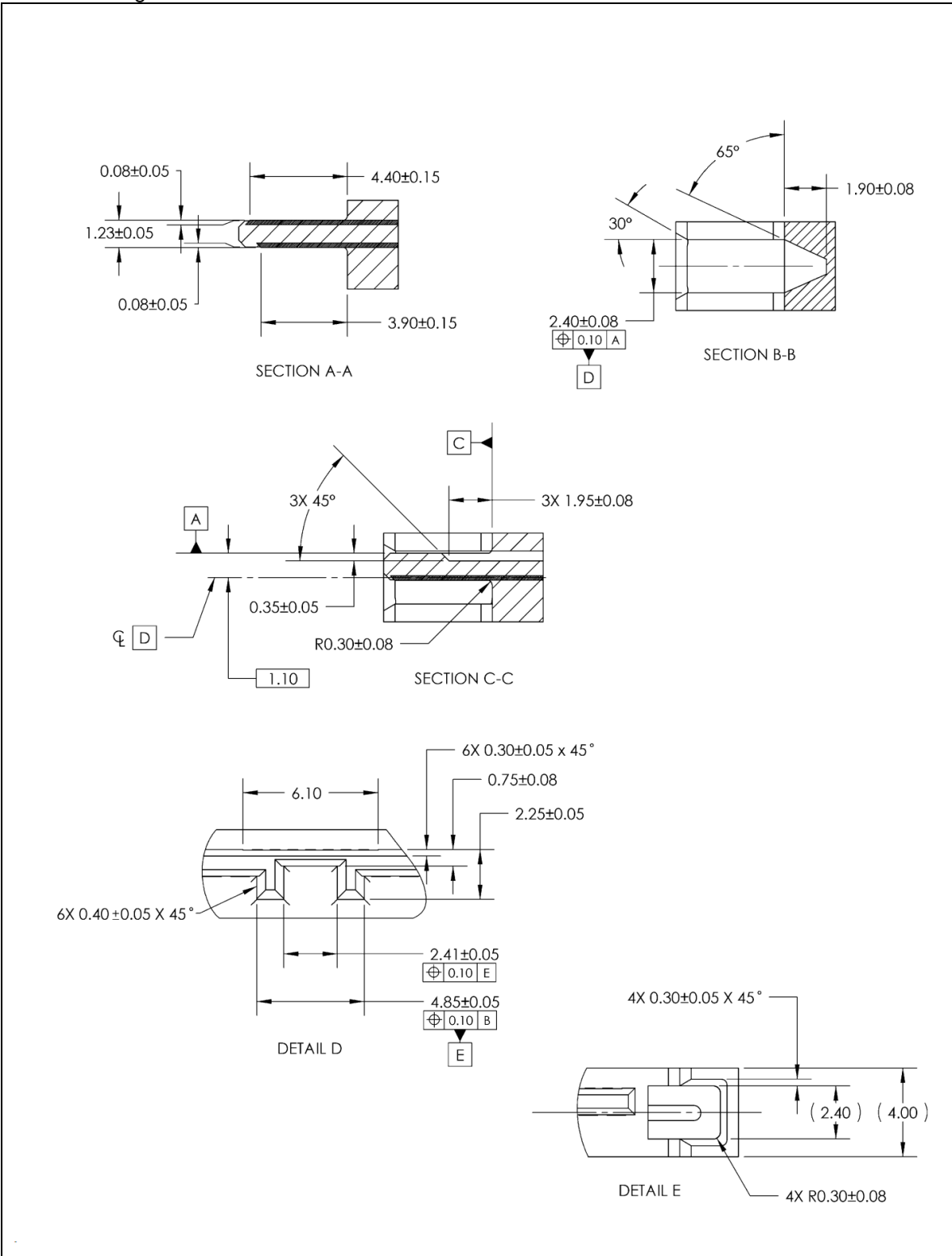


Figure 131 – SATA Express device plug connector drawing (part 2 of 2)



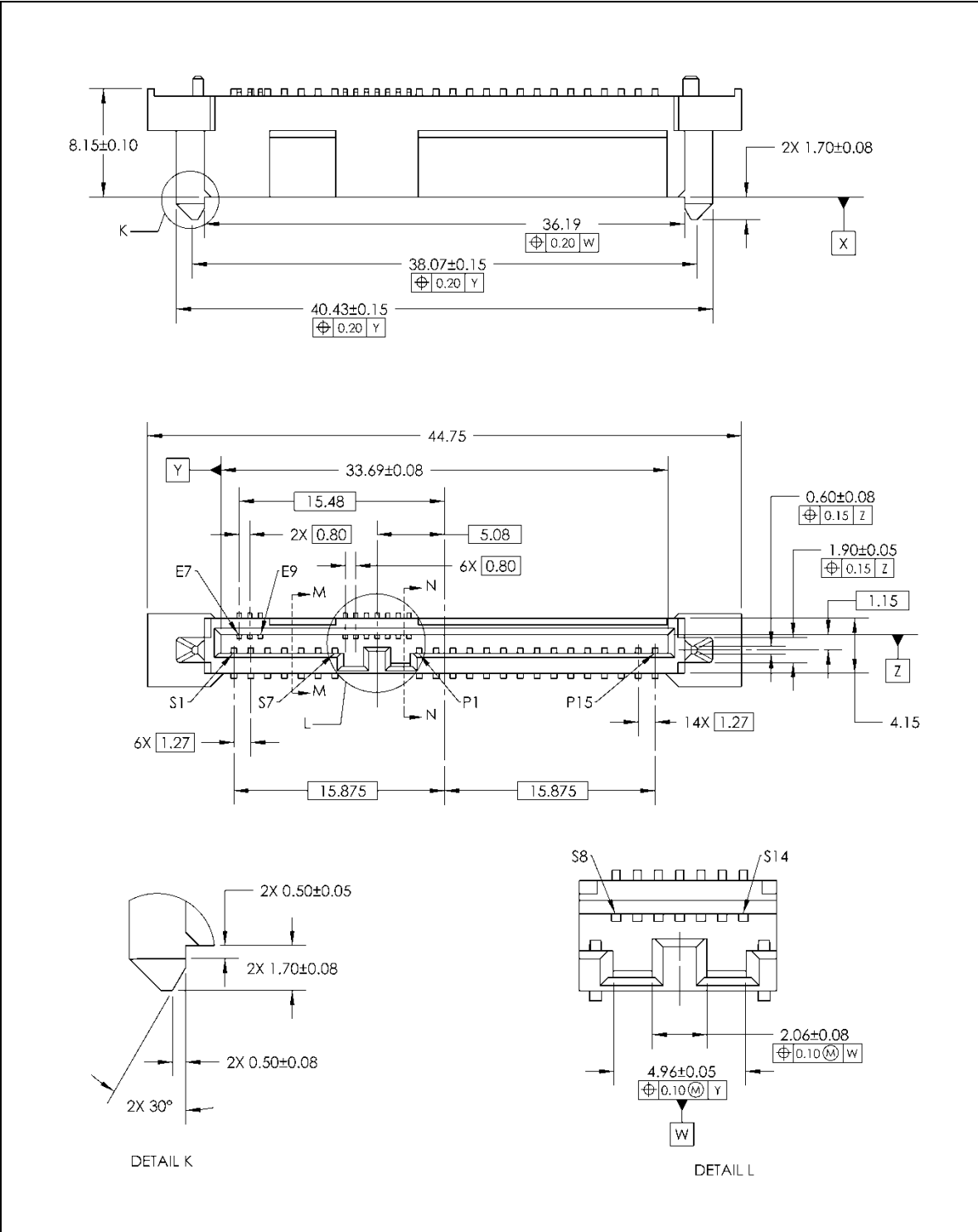


Figure 132 – SATA Express host receptacle connector drawing

(part 1 of 2)

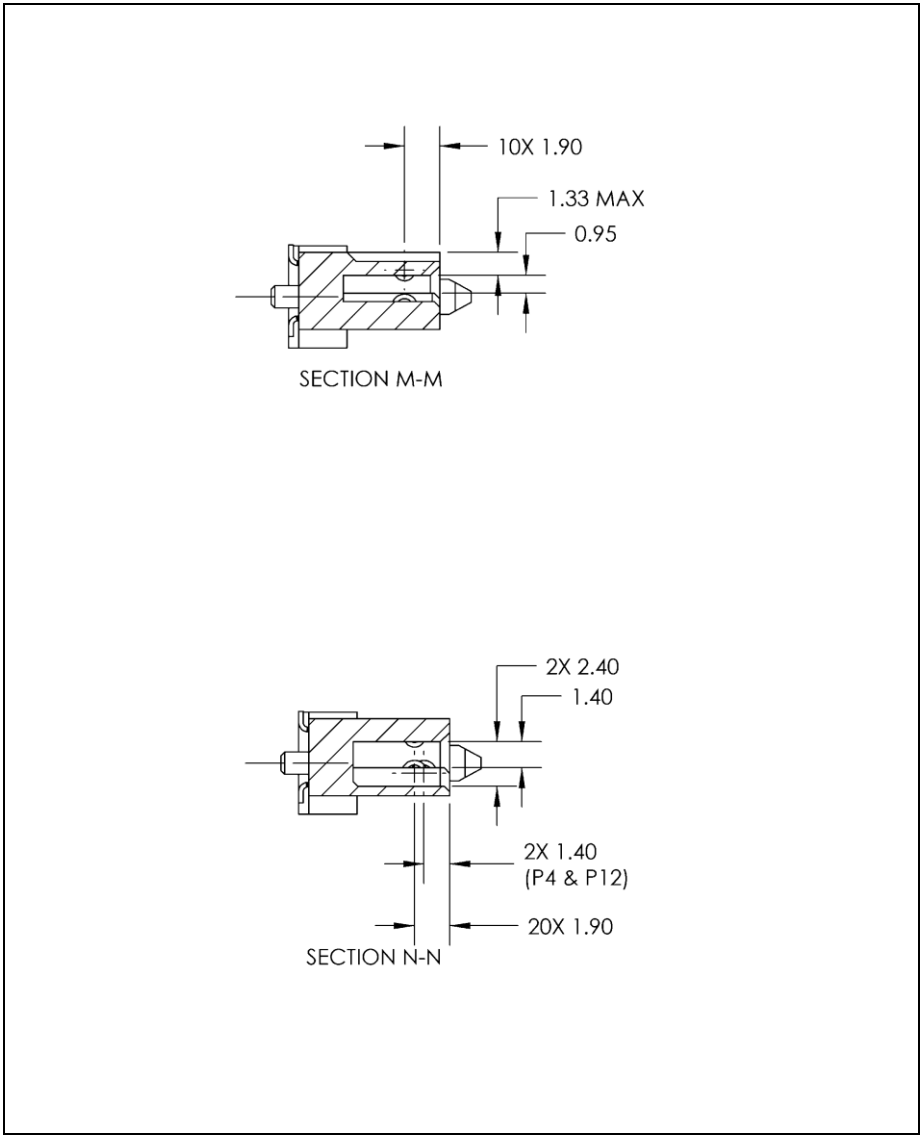


Figure 132 – SATA Express host receptacle connector drawing (part 2 of 2)

## 2.2.2 <6.10.10> SATA Express host plug connector

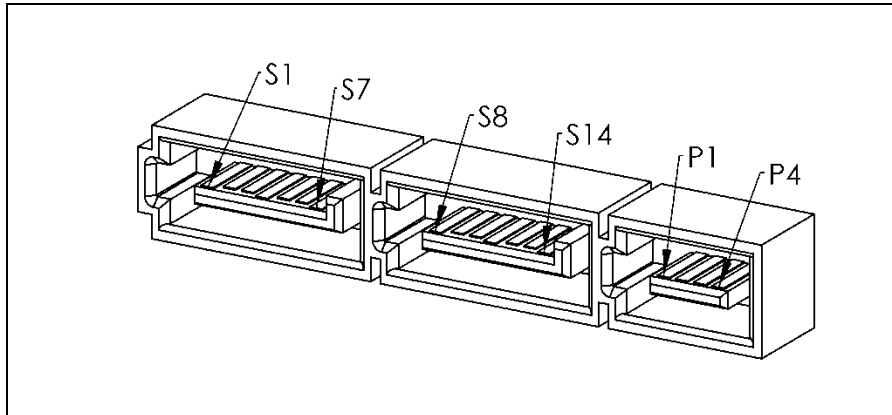
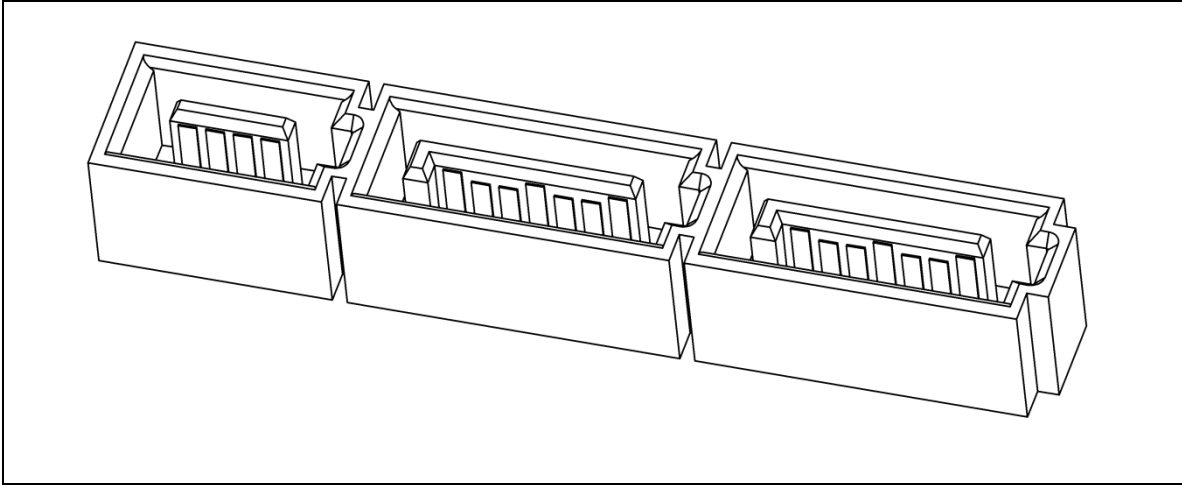


Figure 135 – SATA Express host plug connector pinout (isometric view)

Table 32 – SATA Express host plug connector pin list

Pin position	Name	Signal Description	Usage	Signal Direction	Mating
S1	GND	Ground	PCIe/SATA		First
S2	PETp0 / A0+	PCIe Lane 0 Tx / SATA Port 0 Tx pair	PCIe/SATA	Host Output	Second
S3	PETn0 / A0-				
S4	GND	Ground	PCIe/SATA		First
S5	PERn0 / B0-	PCIe Lane 0 Rx / SATA Port 0 Rx pair	PCIe/SATA	Input to Host	Second
S6	PERp0 / B0+				
S7	GND	Ground	PCIe/SATA		First
S8	GND	Ground	PCIe/SATA		First
S9	PETp1 / A1+	PCIe Lane 1 Tx / SATA Port 1 Tx pair	PCIe/SATA	Host Output	Second
S10	PETn1 / A1-				
S11	GND	Ground	PCIe/SATA		First
S12	PERn1 / B1-	PCIe Lane 1 Rx / SATA Port 1 Rx pair	PCIe/SATA	Input to Host	Second
S13	PERp1 / B1+				
S14	GND	Ground	PCIe/SATA		First
P1	Reserved	Reserved for future use	PCIe/SATA		Second First
P2	PERST#	PCIe reset	PCIe only	Host Output	Second First
P3	CLKREQ# / DEVSLP	PCIe L1 PM Substate / SATA device sleep	PCIe/SATA		Second First
P4	IFDet	Interface detect	PCIe/SATA	Input to Host	First



**Figure 136 – SATA Express host plug connector isometric drawing**

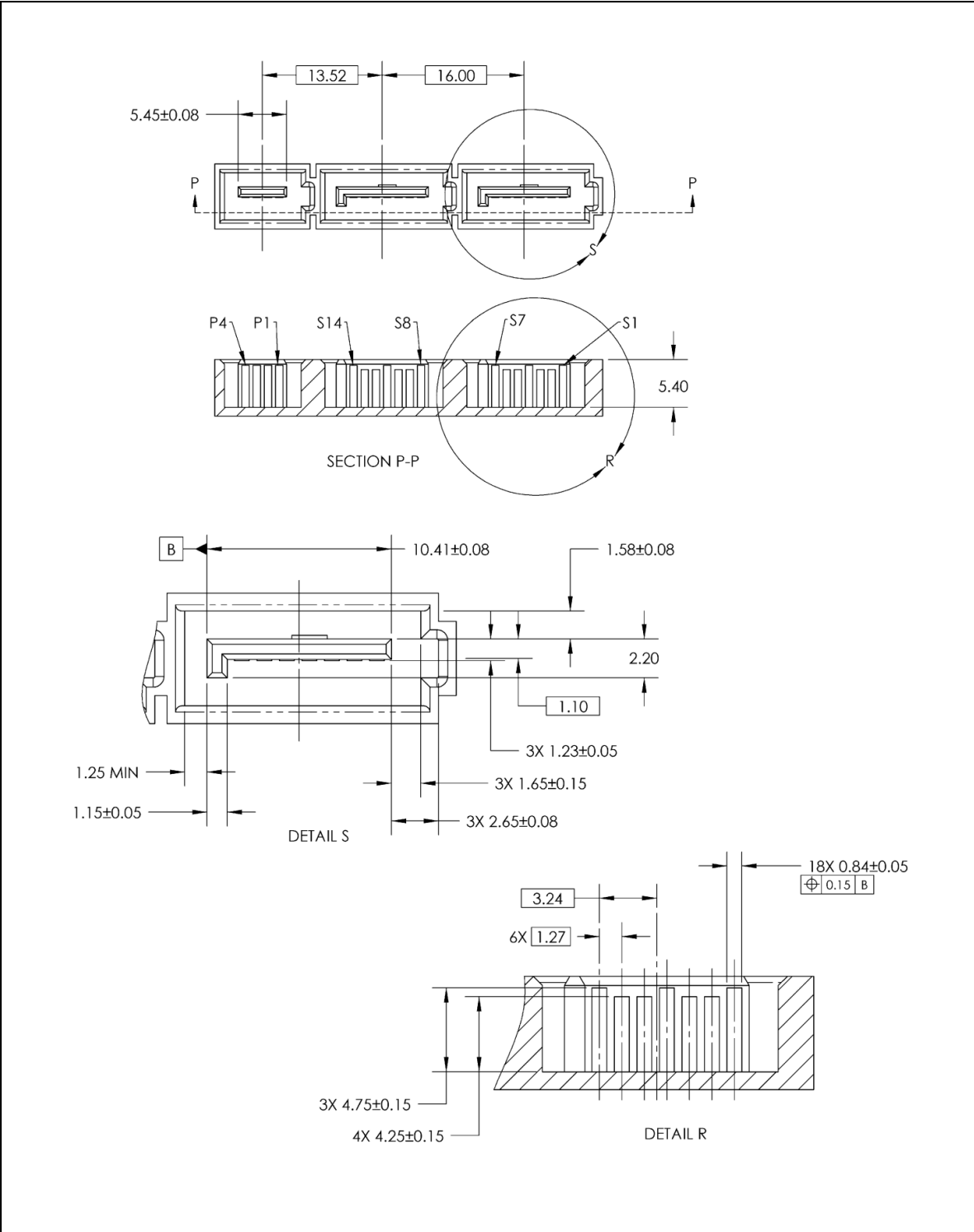


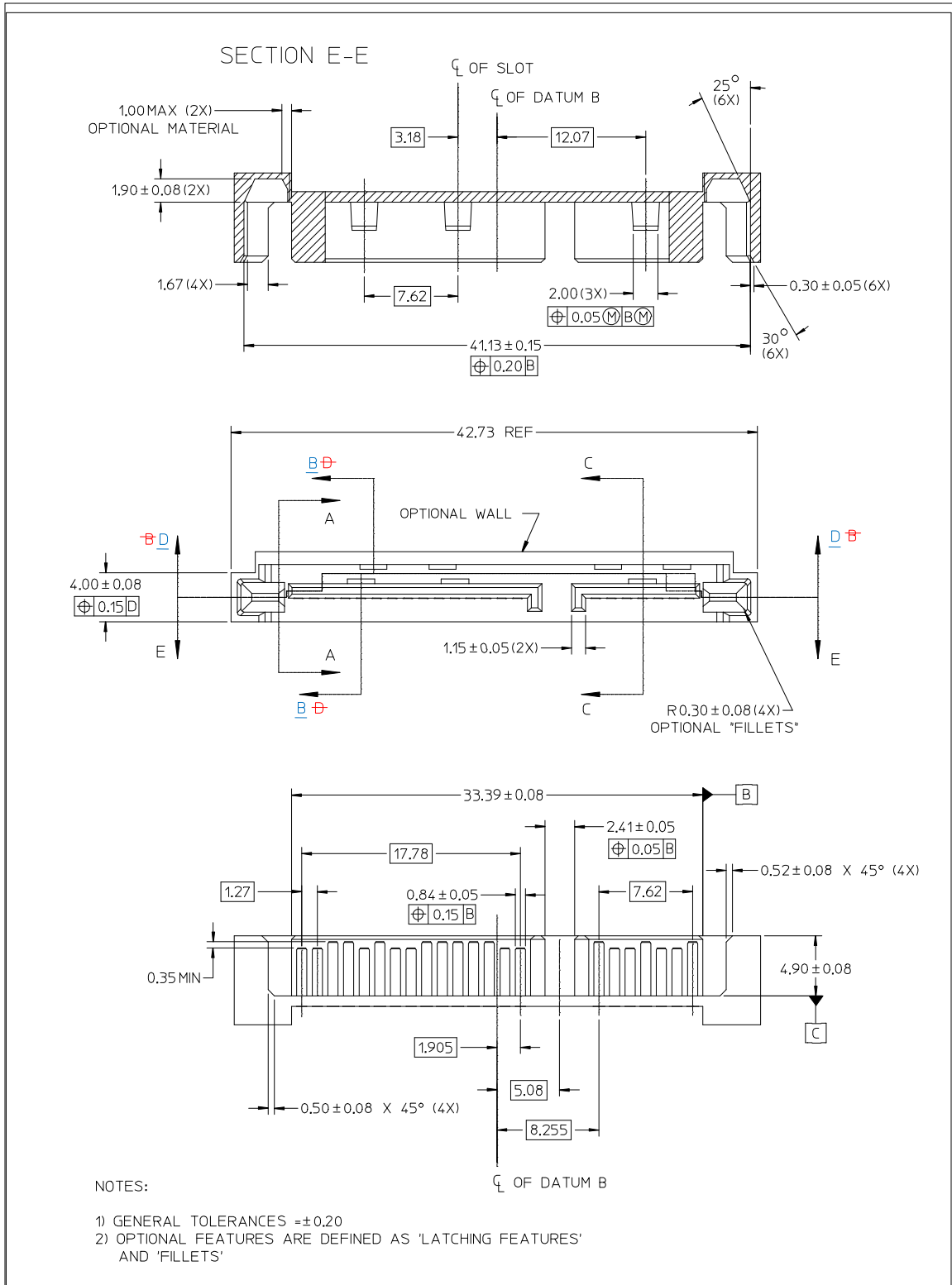
Figure 137 – SATA Express host plug connector drawing

## **2.3 <6.2> Internal cables and connectors**

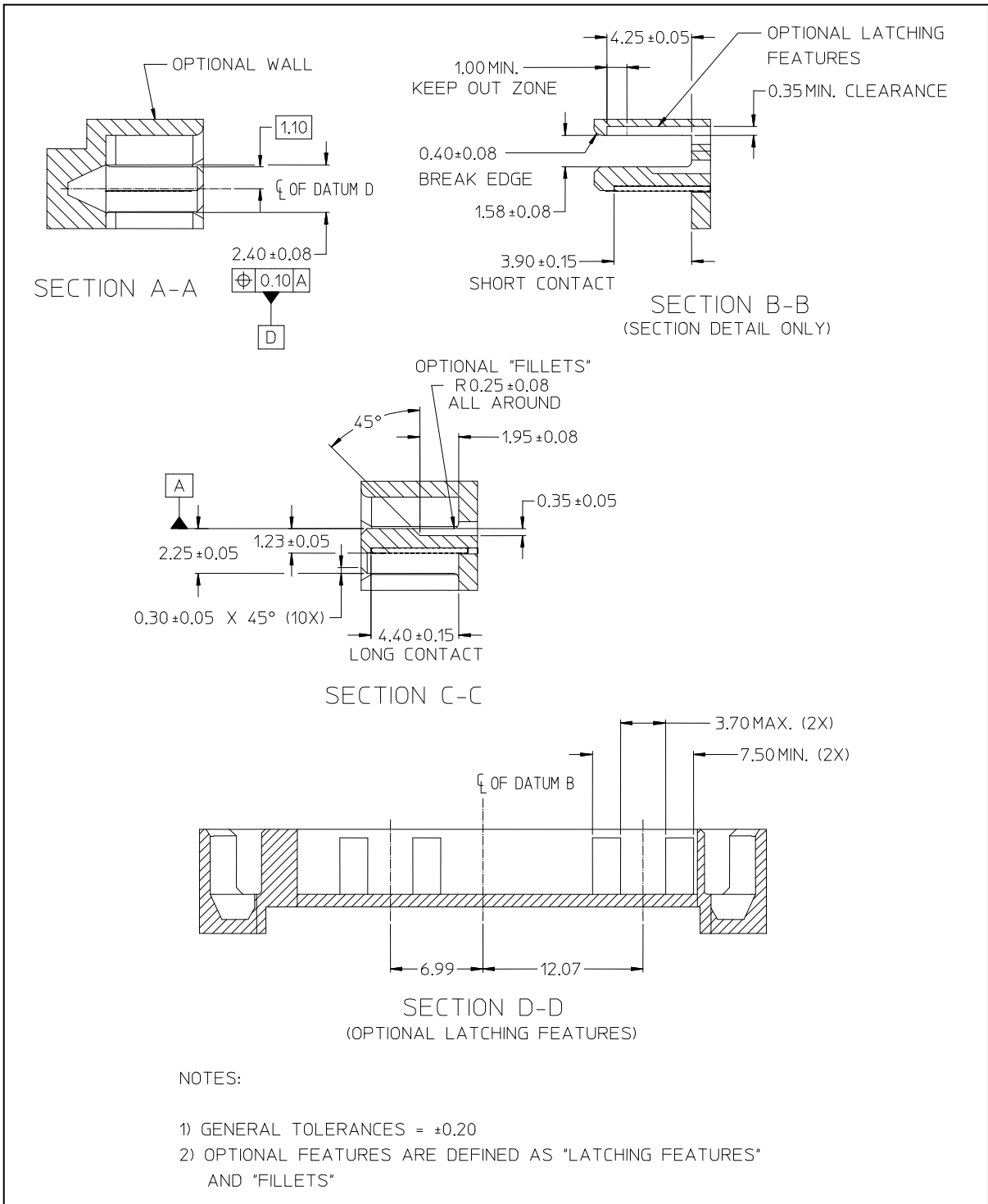
### **2.3.1 <6.2.3>Mating interfaces**

#### **2.3.1.1 <6.2.3.1> Device plug connector**

Editor's note: The standard SATA device plug Figure 32 section lines B and D are reversed relative to the section views found in Figure 33.



**Figure 32 – Device plug connector**



**Figure 33 – Device plug connector (additional views)**