Proposed Draft **Serial ATA International Organization**

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Title : Queued Error I-bit Correction

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Document History

Version	Date	Comments
0	02/03/2014	Initial release.
1	02/11/2014	Changed D180 to TPR078 for Member review

1 Introduction

1.1 Problem Statement

After an error occurs in the FPDMA QUEUED command protocol, the host is obligated to send a command to read the Queued Error log (10h). At the end or processing that command, the device sends an SDB FIS.

There is a conflict between what state DPFDMAQ14 (e.g., a figure) requires for the value of the Interrupt bit, and what the READ FPDMA QUEUED command requires (e.g., text).

In addition, the SATA-IO InterOp specification (Rev 1.4), for both tests NCQ-03 and NCQ-04, the Interrupt bit shall be set to '0' in a SDB FIS in a Queue Abort condition. Products cannot get SATA-IO Certification if the Interrupt bit is set to '1' for a queue abort case.

DFPDMAQ13: WaitforClear	Wait for host to either issue a command to read the Queued Error Log or issue SRST		
	1. READ LOG EXT command with Queued Error Log received	→	DFPDMAQ14: SendQueue_ CleanACK
	2. READ LOG DMA EXT command with Queued Error Log received [a].	→	DFPDMAQ15: SendQueue_ CleanACKDMA
	3. SRST received	→	DSR0: Software_reset_ asserted
	4. Any other command received	→	DFPDMAQ12: BrokenHost_ ClearBusy
	[a] See 13.7		

DFPDMAQ14: SendQueue_CleanACK	Discard all commands in the pending device queue. Transmit Set Device Bits FIS with ERR in Status field cleared to zero, Error field set to 00h, ACT field = FFFF FFFFh, and Interrupt bit cleared to zero.		
	1. Set Device Bits FIS transmission complete	→	DPIOI0: PIO_in

DFPDMAQ15: SendQueue_ CleanACKDMA	Discard all commands in the pending device queue. Transmit Set Device Bits FIS with ERR in Status field cleared to zero, Error field set to 00h, ACT field = FFFF FFFFh, and Interrupt bit cleared to zero.		
	1. Set Device Bits FIS transmission complete	→	DDMAI0: DMA_in

Figure 332 – Device command layer FPDMA queued state machine (part 3 of 3)

13.6.4.4 Queue abort

Following transmission of the Register Device to Host FIS or Set Device Bits FIS in response to an NCQ error condition, the device shall stop processing any outstanding or new commands until the Queued Error Log (see 13.7) is read using the GPL feature set.

If a command to read the Queued Error Log is received, the device shall perform any necessary cleanup before returning detailed error information for the last failed command including the tag value for the failed command as described in 13.7.

In response to a received command to read the Queued Error Log the device shall transmit a Set Device Bits FIS (see Figure 340) to the host with all the bits in the ACT field set to one. This policy avoids the host inadvertently completing a failed command with successful status. The exception to this policy is if the host reads the Queued Error Log for information that is not directly tied to a specific error reported by the device. In the case where a device receives a command to read the Queued Error Log that is not in direct response to an error reported by the device as well as no queued commands being outstanding, it is not required that a Set Device Bits FIS is delivered in response as it is not a necessity to abort any commands at that time.

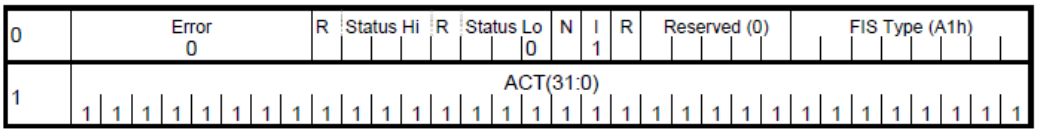

Figure 340 – Set Device Bits FIS aborting all outstanding commands

ACT	The entire ACT field shall be set to one as an indication that all outstanding commands are being aborted.
Error	The Error register shall be cleared to zero.
Status	As defined in 10.5.7. The ERR bit shall be cleared to zero indicating clean up of all previously outstanding commands. Bit 4 may be set to one.
I	Interrupt bit. The interrupt bit shall be set to one.

All other fields as defined in 10.5.7.

If an error is indicated, the host shall treat any outstanding commands that do not have their corresponding SActive register bit cleared to zero as failed.

1.2 Background

SATA-IO InterOp specification (Rev 1.4), for both tests NCQ-03 and NCQ-04, the Interrupt bit shall be set to '0' in a SDB FIS in a Queue Abort condition. Products cannot get SATA-IO Certification if the Interrupt bit is set to '1' for a queue abort case.

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editor note 1: Existing text is black. New text is marked is underlined in blue color. Material to be deleted is ~~red with strikethrough markings~~.

2 Technical Specification Changes

2.1.1.1 <13.6.4.4> Queue abort

Following transmission of the Register Device to Host FIS or Set Device Bits FIS in response to an NCQ error condition, the device shall stop processing any outstanding or new commands until the Queued Error Log (see 13.7) is read using the GPL feature set.

If a command to read the Queued Error Log is received, the device shall perform any necessary cleanup before returning detailed error information for the last failed command including the tag value for the failed command as described in 13.7.

In response to a received command to read the Queued Error Log the device shall transmit a Set Device Bits FIS (see Figure 340) to the host with all the bits in the ACT field set to one. This policy avoids the host inadvertently completing a failed command with successful status. The exception to this policy is if the host reads the Queued Error Log for information that is not directly tied to a specific error reported by the device. In the case where a device receives a command to read the Queued Error Log that is not in direct response to an error reported by the device as well as no queued commands being outstanding, it is not required that a Set Device Bits FIS is delivered in response as it is not a necessity to abort any commands at that time.

0	Error								R	Status Hi				R	Status Lo					N	I	R	Reserved (0)						FIS Type (A1h)							
	0																0				~~1~~ 0													
1	ACT(31:0)																																	
	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Figure 340 – Set Device Bits FIS aborting all outstanding commands

ACT The entire ACT field shall be set to one as an indication that all outstanding commands are being aborted.

Error The Error register shall be cleared to zero.

Status As defined in 10.5.7. The ERR bit shall be cleared to zero indicating clean up of all previously outstanding commands. Bit 4 may be set to one.

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All other fields as defined in 10.5.7.

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