Proposed Draft

Serial ATA International Organization

Revision 6 08/11/2015

Serial ATA ECN: SATA32_ECN089 Title : DAS/DSS support clarifications Sponsors: Micron

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ECN089v6_SATA32_DSS_DAS_SupportClarifications

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Document History

Version	Date	Comments	
0	7/1/2015	 Initial presentation. Two version of v0 were released, this is the latest, and the only one presented. The next version will be v2 	
2	7/7/2015	 Editorial & format changes requested in 07/06/2015 digital meeting Editorial changes requested by Harvey Newman Added changes to 13.7.9.2.19 HARDWARE FEATURE CONTROL SUPPORTED bit 	
3	7/8/2015	Editorial changes requested by Harvey NewmanAdded 13.3.9 (sigh)	
4	7/31/2015	 Editorial changes requested in 07/27 digital meeting Additional bit/field and smallcap cleanup. Reworded table 104 introduction Changed multiple IDENTIFY WORD bit descriptions to point to Identify Device Log Page bits Added 13.7.9.3.12 and 13.7.9.3.13 	
5	8/3/2015	 Incorporated editorial changes from Harvey Newman. Renamed Table 104. Additional field and smallcap cleanup. 	
6	8/11/2015	Member review, changed D201 to ECN089.	

1 Introduction

There has been some confusion if DSS and DAS may be supported when Hardware Feature Control is not supported.

This lack of clarity is exacerbated by the historical intent of not reporting the enabled condition or the support of DSS and/or DAS. This ECN does not change this.

There are several places where the Serial ATA Revision 3.2 specification and the text of ratified TPR058v3_SATA32 could be clearer that the intent of the SET FEATURES Hardware Feature Control subcommands is that:

- a) the SET FEATURES Hardware Feature Control Enable subcommand enables the defined extended behavior of the pin(s); and
- b) the SET FEATURES Hardware Feature Control Disable subcommand disables the extended behavior (and does not affect the defined default behavior).

Efforts have been made to only change text, without changes to command names or field names.

2 Technical Specification Changes Documention

The following additions are based on the content of Serial ATA Revision 3.2 and ratified TPR058v3_SATA32. Proposed additions to Serial ATA Revision 3.2 text are marked in <u>blue underline</u>. Proposed deletions to Serial ATA Revision 3.2 text are marked in <u>red strikethrough</u>. Black text is the original Serial ATA Revision 3.2 text. Section headers correspond to the section in Serial ATA Revision 3.2 into which the proposed text is to be inserted.

The changes (with context) are:

4.1.1.66 Hardware Feature Control pin(s)

For the LIF-SATA connector, Hardware Feature Control (See 13.10) are connector pins P8 and P21. For the 1.8 inch Micro SATA connector, Hardware Feature Control is connector pin P7. For all other connectors Hardware Feature Control is connector pin P11.

6.13 Hardware Feature Control (optional)

6.13.1 Behavior

6.13.1.1 Behavior overview

Prior to processing a SET FEATURES Enable Hardware Feature Control (see 13.3.9) subcommand, the Hardware Feature Control <u>pin(s)</u> (see 4.1.1.66) operate operates using the default behavior in accordance with 6.13.1.2. Otherwise the Hardware Feature Control <u>pin(s)</u> operate operates using the extended behavior in accordance with 6.13.1.3.

6.13.1.2 Default behavior

There are two hardware control features listed as:

- a) Disable Staggered Spinup (DSS); and
- b) Device Activity Signal (DAS) (e.g., light emitting diode (LED)).

<Editor's Note: TPR058v3 addition of 'and Table 123' is included in black below.>

Due to various hardware issues, these features are mapped onto different physical pins depending on the connecter type as indicated in Table 41 and Table 123. Not all features are defined for all connecter types.

Standard Connector (3.5 inch & 2.5 inch)	1.8 inch Micro SATA Connector ^a	LIF-SATA Connector		
Pin 11:	Pin 7:	Pin 8:		
a) DSS; <u>or<mark>and</mark></u>	a) DAS <u>.</u>	a) DSS; <u>orand</u>		
b) DAS.	-	b) DAS.		
^a DSS is not defined for 1.8 inch Micro SATA Connector.				

Table 41 – <u>Default uses of DSS and DAS for various connectors</u>

The <u>A</u> Hardware Feature Control <u>pin</u>, (i.e., <u>pins P11, P7, or P8 depending upon connectorsee Table 41</u>) may be used by the device to provide the host with an activity indication and it may be used by the host to indicate whether staggered spinup should be used. To accomplish both of these goals, <u>the a</u> Hardware Feature Control_<u>pin (see Table 41)</u> acts as an input from the host to the device prior to PHYRDY for staggered spinup control and then acts as an output from the device to the host after PHYRDY for activity indication. The activity indication provided is primarily for use in backplane applications. See 13.15 for information on activity LED generation for desktop applications.

<Editor's Note: TPR058v3 addition of 'host or' is included in black below>

A host or device may optionally support activity indication, staggered spinup control, or both features. If neither feature is supported, then pin P11, P7, or P8 depending upon connector is a no connect at the device as specified in Table 5.

6.13.1.3 Extended behavior

The Hardware Feature Control pin(s) may be used by the device for one of the following:

- a) default use of the Hardware Feature Control pin(s) (see 6.13.1.2);
- b) Direct Head Unload (DHU) (see 6.13.2, 13.10, and 13.19); or
- c) vendor specific use (see 13.10).

13.3.9 Enable Hardware Feature Control

A <u>Count_COUNT field (7:0)</u> value of 08h is used by the host to enable <u>the extended uses of the Hardware</u> Feature Control_<u>pin(s)</u>. See <u>13.10</u> for additional information about Hardware Feature Control.

The extended uses of the Hardware Feature Control pin(s) shall be disabled by power-on reset.

LBA(15:0) contains a function identifier (see Table 104) Table 104 defines function identifiers used to enable specific extended uses of the Hardware Feature Control pin(s) in the LBA field (15:0) of the Enable Hardware Feature Control command.

LBA(15:0)Function Identifier	Description	Preserved Across Software Reset	Preserved Across COMRESET
0000h	Reserved	na	na
0001h	Direct Head Unload (DHU) (see 13.19)	Y	Yes, regardless of SSP setting
0002h to EFFFh	Reserved	na	na
F000h to FFFFh	Vendor specific	Vendor specific	Vendor specific

Table 104 –	Extended Use	es of the	Hardware Feature	Control pin(s)	definitions
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On successful completion of this command:

a) <u>the CURRENT HARDWARE FEATURE CONTROL IDENTIFIER</u> Current Hardware Feature Control Identifier <u>field</u> (see 13.7.9) shall be set to the value in <u>the LBA field</u> (15:0);

- b) the HARDWARE FEATURE CONTROL ENABLED bit (see 13.7.9.3.6) IDENTIFY DEVICE data Word 79, bit 5 shall be set to one; and
- c) the behavior of Hardware Feature Control <u>pin(s)</u> is specified by Table 104.

The device shall return command aborted if:

- a) the HARDWARE FEATURE CONTROL SUPPORTED bit (see 13.7.9.2.19) IDENTIFY DEVICE data Word 78 bit 5 is cleared to zero;
- b) the value in the LBA field (15:0) is not equal to the <u>SUPPORTED HARDWARE FEATURE CONTROL</u> <u>IDENTIFIER field</u>Supported Hardware Feature Control Identifier (see 13.7.9.3.13); or
- c) the <u>CURRENT HARDWARE FEATURE CONTROL IDENTIFIER field</u>Current Hardware Feature Control Identifier (see 13.7.9.3.12) is non-zero.

13.7.9.2.19 HARDWARE FEATURE CONTROL SUPPORTED bit

If the HARDWARE FEATURE CONTROL SUPPORTED bit is set to one, then the device supports <u>the extended</u> <u>uses of the</u> Hardware Feature Control <u>pin(s)</u> (see 6.13) (see 13.10). If the HARDWARE FEATURE CONTROL SUPPORTED bit is cleared to zero, then <u>the extended uses of the</u> Hardware Feature Control <u>pin(s) are is</u> not supported and the HARDWARE FEATURE CONTROL ENABLED bit is <u>shall be</u> cleared to zero (see 13.10).

IDENTIFY DEVICE data Word 78 bit 5 is a copy of this bitfield.

13.7.9.3.6 HARDWARE FEATURE CONTROL ENABLED bit

If the HARDWARE FEATURE CONTROL ENABLED bit is set to one, then device support for the <u>extended uses of</u> the Hardware Feature Control <u>feature_pin(s)</u> (see 13.10) is are enabled. If the HARDWARE FEATURE CONTROL ENABLED bit is cleared to zero, then:

- a) the extended uses of the Hardware Feature Control pin(s) are is-disabled; and
- b) the default uses of the Hardware Feature Control pin(s) are not affected (see 13.10).

IDENTIFY DEVICE data Word 79 bit 5 is a copy of this bitfield.

13.7.9.3.12 CURRENT HARDWARE FEATURE CONTROL IDENTIFIER bitfield

If the CURRENT HARDWARE FEATURE CONTROL IDENTIFIER <u>bit field</u> is non-zero, then Table 104 describes the curent Hardware Feature Control behavior. If the CURRENT HARDWARE FEATURE CONTROL IDENTIFIER <u>field</u> is cleared to zero, then the current Hardware Feature Control behavior shall be <u>either_DSS_ or_DAS_ or neither</u>.

13.7.9.3.13 SUPPORTED HARDWARE FEATURE CONTROL IDENTIFIER bitfield

The SUPPORTED HARDWARE FEATURE CONTROL IDENTIFIER bit-field (see Table 104) indicates the value that is permitted for the <u>CURRENT HARDWARE FEATURE CONTROL IDENTIFIER</u> Current Hardware Feature Control Identifier field.

13.10 Hardware Feature Control (optional)

In Serial ATA Revision 3.0 and previous specifications, <u>a</u> Hardware Feature Control <u>pin</u> is defined only for these uses:

- a) Disable Staggered Spinup (i.e., DSS) (see 6.13.1.2 and 13.11); and
- b) Activity indication LED (i.e., DAS) (see 6.13.1.2 and 13.15).

This specification defines additional uses for the Hardware Feature Control pin(s) (see 6.13). Table 123 specifies the pin(s) used by Hardware Feature Control for various connectors.

<Editor's Note: TPR058v3 addition of tablenote b is included in black below>

Standard Connector (3.5 inch & 2.5 inch)	1.8 inch Micro SATA Connector ^a	LIF-SATA Connector		
Pin P11: a) DSS; b) DAS ^b ; c) DHU ^b ; or d) other vendor specific.	Pin P7: a) DAS ^b ; b) DHU ^b ; or c) other vendor specific.	Pin P8: a) DSS; b) DAS; or c) other vendor specific. Pin P21: a) DHU.		
^a DSS is not defined for 1.8 inch Micro SATA Connector. ^b Concurrent support of both DAS and DHU on the same pin is not permitted.				

Table 123 – Pin(s) used by Hardware Feature Control

If the extended uses of the Hardware Feature Control pin(s) are is supported, then:

- a) IDENTIFY DEVICE data Word 78 bit 5 (see 13.2.2.19) shall be set to one;
- b) the SET FEATURES <u>Enable</u>Select Hardware Feature Control subcommand shall be supported (see 13.3.9);
- c) page 08h of the Identify Device Data log (see 13.7.9) shall be supported;
- d) on processing a power on reset, then:
 - A) IDENTIFY DEVICE data Word 79 bit 5 (see 13.2.2.20) shall be cleared to zero;
 - B) the <u>CURRENT HARDWARE FEATURE CONTROL IDENTIFIER</u><u>Current Hardware Feature Control</u> <u>Identifier</u> <u>field (see 13.7.9.3.12)</u> in the Identify Device Data log shall be cleared to zero; and
 - C) <u>See see 6.13.1.2</u> for requirements of the <u>default uses of the</u> Hardware Feature Control pin(s);

and

- e) after processing a SET FEATURES Enable Hardware Feature Control subcommand with no error, then:
 - A) IDENTIFY DEVICE data Word 79 bit 5 (see 13.2.2.20) shall be set to one;
 - B) the <u>CURRENT HARDWARE FEATURE CONTROL IDENTIFIER</u>Current Hardware Feature Control Identifier field (see 13.7.9.3.12) in the Identify Device Data log shall be non-zero;
 - C) the <u>SUPPORTED HARDWARE FEATURE CONTROL IDENTIFIER</u>Supported Hardware Feature Control Identifier field (see 13.7.9.3.13) in the Identify Device Data log shall be non-zero; and
 - D) the behavior of the Hardware Feature Control pin(s) areis specified by the SET FEATURES Enable Hardware Feature Control subcommand.

If the extended uses of the Hardware Feature Control pin(s) are is not supported, then:

- a) IDENTIFY DEVICE data Word 79 bit 5 (see 13.2.2.20) shall be cleared to zero;
- b) the SET FEATURES <u>Enable</u>Select Hardware Feature Control subcommand shall not be supported (see 13.3.9);
- c) the <u>SUPPORTED HARDWARE FEATURE CONTROL IDENTIFIER</u> Supported Hardware Feature Control Identifier field (see 13.7.9.3.13) in the Identify Device Data log shall be cleared to zero;
- d) the <u>CURRENT HARDWARE FEATURE CONTROL IDENTIFIER</u>Current Hardware Feature Control Identifier field (see 13.7.9.3.12) in the Identify Device Data log shall be cleared to zero; and
- e) Seesee 6.13.1.2 for requirements of the default uses of the Hardware Feature Control pin(s).