

**Proposed  
Draft**

**Serial ATA  
International Organization**

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**Serial ATA Revision 3.3 ECN 091  
Title : Correction to Power Disable**

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## Document History

Version	Date	Comments
0	11/11/2016	Initial release.

## 1 Introduction

A definition was removed from "SATA31\_TPR\_C116 Enable new Power Disable feature on standard SATA connector P3" between revision 9 and revision 10. Revision 10 was ratified and included in SATA Revision 3.2.

This ECN replaces the definition for a timing parameter  $T_{DS}$  that was removed for an unknown reason.

## 2 Technical Specification Changes

[editor's note: make the following modifications]

[editors note: blue underscore is text to be inserted. ~~red strikethru~~ text is to be deleted. black text is unchanged.]

## 8.6 Power Disable signal protocol and timing

The Power Disable feature, if supported and enabled, may be used to disable power to the device circuitry.

Since the Power Disable feature and the Device Sleep feature (see **Error! Reference source not found.**) both use pin P3, these features are mutually exclusive.

If the Power Disable feature is supported, then the device shall set IDENTIFY DEVICE data Word 78 bit 12 to one.

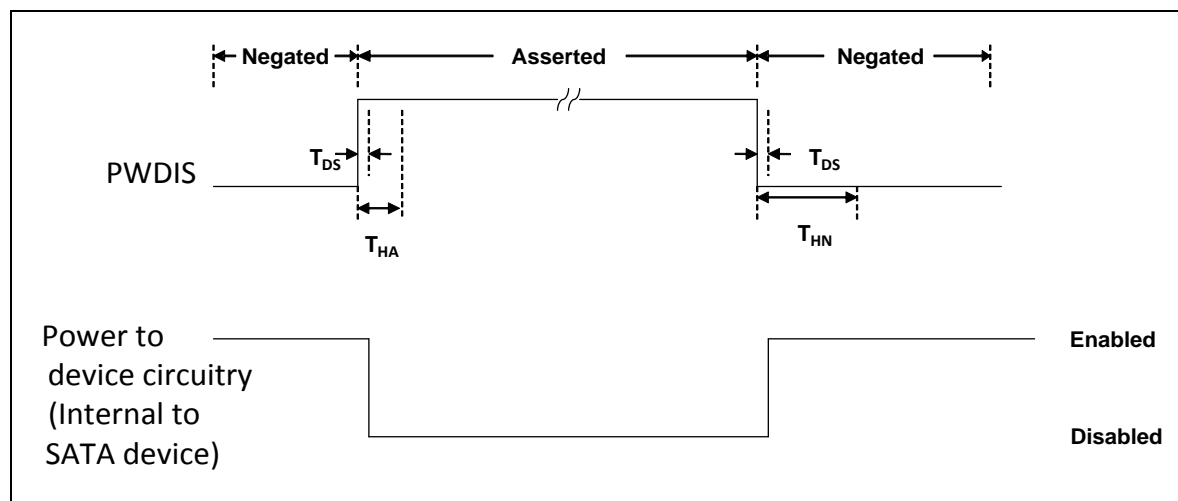
If the Power Disable feature is supported and the POWER DISABLE FEATURE ALWAYS ENABLED bit (see **Error! Reference source not found.**):

- a) is set to one, then the Power Disable feature is always enabled; or
- b) is cleared to zero, then the Power Disable feature:
  - A) shall be disabled as a result of processing a power on reset;
  - B) shall not be affected as a result of processing a hardware reset or a software reset; and
  - C) may be enabled as a result of processing a SET FEATURES Enable/Disable Power Disable Feature subcommand (see **Error! Reference source not found.**).

If the Power Disable feature is supported and enabled, then the device shall:

- a) allow power to be applied to the device circuitry if the PWDIS signal is not connected on the host connector;
- b) allow power to be applied to the device circuitry if the PWDIS signal is negated as defined in Table 1;
- c) disable power applied to the device circuitry if:
  - 1) the minimum negated hold time in Table 1 is met; and
  - 2) the PWDIS signal is asserted as defined in Table 1;
- d) perform the actions defined for a power on reset if:
  - 1) the minimum negated hold time in Table 1 is met;
  - 2) the PWDIS signal is asserted as defined in Table 1; and
  - 3) the PWDIS signal transitions from asserted to negated;and
- e) not respond to a change of the PWDIS signal from negated to asserted or asserted to negated until the PWDIS signal is held at the asserted or negated level for a minimum of 1 us [as defined by  \$T\_{DS}\$  in table 82.](#)

Figure 1 provides an overview of the Power Disable protocol. See **Error! Reference source not found.** for additional requirements.



**Figure 1 – Power Disable protocol overview**

All voltages and currents in Table 1 are measured at the PWDIS pin (i.e., P3) on the device connector.

**Table 1 – Characteristics of the PWDIS signal applied to the device**

Parameter	Characteristic	Units	Minimum	Maximum
$V_{DIn}$	Absolute maximum voltage input range	V	-0.5	3.6
$V_{HNegate}$	Negated voltage (power enabled) <sup>a b</sup>	V	-0.5	0.7
$V_{HAssert}$	Asserted voltage (power disabled) <sup>c</sup>	V	2.1	3.6
$A_{DSSCC}$	Driver sink/source current capability <sup>b c</sup>	uA	100	-
$T_{DS}$	<a href="#">Device response time to a change in the PWDIS signal.</a>	us	1.0	-
$T_{HA}$	PWDIS asserted hold time <sup>d e</sup>	s	5.0	-
$T_{HN}$	PWDIS negated hold time <sup>d e</sup>	s	30.0	-

<sup>a</sup> The device shall allow power to be applied to the device **circuitry** if P3 is not connected on the host connector.

<sup>b</sup> The PWDIS signal shall be actively negated.

<sup>c</sup> The PWDIS signal shall be actively asserted.

<sup>d</sup> The hold time is the length of time the PWDIS signal is asserted or negated. The length of time after the PWDIS signal is asserted or negated until the disabling or allowing of power to the device circuitry is vendor specific.

<sup>e</sup> The PWDIS signal should not transition from negated to asserted or asserted to negated for the negated hold time:

- after power is applied to the host connector; or
- after the detection of a hot plug event.