

**Proposed
Draft**

**Serial ATA
International Organization**

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Title : Clarification of Speed Negotiation**

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Document History

Version	Date	Comments
1	4 February 2010	Initial release.
2	17 February 2010	Added transition out of HP6 to clarify asynchronous reset
3	24 February 2010	Add another transition out of HP6 to clarify optional reset for speed negotiation
4	3 March 2010	Remove additional transitions out of HP6. Edit note 6 on HP6.
5	17 March 2010	Further edits on note 6, get diagrams edited from rev 3.0 and vote approval.

1 Introduction

1.1 Problem Statement

Documentation of existing methods of speed negotiation.

1.2 Solution Summary

1. Make more clear the spec allows an alternate method for Hosts to change speed (during HR_Reset), avoiding the 53.3nS limitation.

1.3 Background (optional)

The scope of the process of speed negotiation has grown beyond what was originally intended in response to implementation issues

The specification places a higher burden on Hosts than Devices in that 1) Hosts must determine the speed of incoming Aligns 2) Hosts must switch their speed in 53.3nS and 3) Hosts must not induce a condition where Device receivers cannot reacquire. Host designers have met these burdens by different means.

The process of changing speed can involve a simple switching of clocks and thus achieve the 53.3nS, or it may require changing a PLL which may need 100uS or more to change. Device designers are allowed 375uS (indirectly set by a 874uS timeout) which allows the PLLs. However, Host designers faced with a 53.3nS limitation, implemented a reset based scheme to allow them enough time to change speed. This is currently allowed by the spec.

The spec currently allows a speed negotiation scheme using a COMRESET command to achieve software control of the speed negotiation process.

2 Technical Specification Changes

Table 51 – State Diagram Host Phy Initialization State Machine

HP6: HR_AwaitAlign	Host transmits D10.2 characters at lowest supported rate ^{2,5}	
1. ALIGN _P ₃ detected from device (at any supported speed) ³ .	→	HR_AdjustSpeed
2. ALIGN _P not detected from device ⁶ and 873.8 us (32768 Gen1 Dwords) has elapsed since entry to HR_AwaitAlign.	→	HR_Reset ^{1,4}
3. ALIGN _P not detected from device and less than 873.8 us (32768 Gen1 Dwords) has elapsed since entry to HR_AwaitAlign.	→	HR_AwaitAlign
<p>NOTES:</p> <ol style="list-style-type: none"> Host retries the power-on sequence indefinitely unless explicitly turned off by the Application layer. Host shall start transmitting D10.2 characters no later than 533 ns (20 Gen1 Dwords) after COMWAKE is negated as specified in the OOB signaling section. Host designers should be aware that the device is allowed 53.3 ns (2 Gen1 Dwords) after releasing COMWAKE (by holding the idle condition for more than 175 ns) to start sending characters. Until this occurs, the bus is at an idle condition and may be susceptible to crosstalk from other devices. Care should be taken so that crosstalk during this window doesn't result in a false detection of an ALIGN_P. For example: a compliant host may detect the negation of COMWAKE in as little as 112 ns, such a host should wait at least 116.3 ns (175+53.3-112) after detecting the release of COMWAKE to start looking for ALIGN_P primitives. The Host Phy Initialization state machine may use the transition to HR_Reset as a method of speed negotiation. The Device may respond with D10.2 when out of lock (see DR_SendAlign). If ALIGN_P is detected at a lower speed, the host may (optionally) transition to HR_Reset before the 873.8us timeout thus reducing the time for speed negotiation. 		

