Deleted: 1
Deleted: 4
Deleted: 006
Deleted: 001
Deleted: 5.doc

**Proposed Draft**

**Serial ATA International Organization**

**Version 5**
**October 1, 2008**

# Technical Proposal TPD_019_20081114_v08 Title: $HOLD_P$/$HOLDA_P$ Protocol Change for 6G SATA

Deleted: 1
Deleted: 14
Deleted: 006
Deleted: 001
Deleted: 5

Deleted: 1
Deleted: 4
Deleted: 006
Deleted: 001
Deleted: 5
Deleted: .doc

This Draft Specification is NOT the final version of the Specification and is subject to change without notice. A modified, final version of this Specification ("Final Specification") when approved by the Promoters will be made available for download at this Web Site: http://www.serialata.org.

THIS DRAFT SPECIFICATION IS PROVIDED "AS IS" WITH NO WARRANTIES WHATSOEVER, INCLUDING ANY WARRANTY OF MERCHANTABILITY, NON-INFRINGEMENT, FITNESS FOR ANY PARTICULAR PURPOSE OR ANY WARRANTY OTHERWISE ARISING OUT OF ANY PROPOSAL, SPECIFICATION, OR SAMPLE. Except for the right to download for internal review, no license, express or implied, by estopple or otherwise, to any intellectual property rights is granted or intended hereunder.

THE PROMOTERS DISCLAIM ALL LIABILITY, INCLUDING LIABILITY FOR INFRINGEMENT OF ANY PROPRIETARY RIGHTS, RELATING TO USE OF INFORMATION IN THIS DRAFT SPECIFICATION. THE PROMOTERS DO NOT WARRANT OR REPRESENT THAT SUCH USE WILL NOT INFRINGE SUCH RIGHTS.

THIS DOCUMENT IS AN INTERMEDIATE DRAFT FOR COMMENT ONLY AND IS SUBJECT TO CHANGE WITHOUT NOTICE.

* Other brands and names are the property of their respective owners.

Deleted: 1
Deleted: 4
Deleted: 006
Deleted: 001
Deleted: 5
Deleted: .doc

## Author Information


| Author Name | Company | Email address |
|---|---|---|
| Joseph Chen<br>Mladen Luksic | Samsung<br>Western Digital | joseph.chen@samsung.com<br>mladen.luksic@wdc.com |


## Workgroup Chair Information

| Workgroup (Phy, Digital, etc…) | Chairperson Name | Email address |
|---|---|---|
| Digital | Mladen Luksic | mladen.luksic@wdc.com |

### Document History

| Version | Date | Comments |
|---|---|---|
| 0 | 6/30/2008 | Initial presentation of the issue |
| 1 | 7/7/2008 | Propagation delay table |
| 2 | 7/14/2008 | Proposed text change |
| 3 | 10/1/2007 | Discussion, no changes |
| 4 | 9/30/2008 | Removed text “additional data” from the proposed text change |
| 5 | 10/2/2008 | In the proposal format |
| 6 | 10/23/2008 | Editorial text change |
| 7 | 11/05/2008 | Only uses “Dword” in the text; changes in Table 1to include any fraction of Dword; editorial changes; added the remainder of the text in section 9.4.7 from the Revision 2.6. |
| 8 | 11/14/2008 | Removed “primitive” after $HOLD_P$ and $HOLD_P$. |

Deleted: 1
Deleted: 4
Deleted: 006
Deleted: 001
Deleted: 5
Deleted: .doc

## 1. Introduction

With the introduction of 6G SATA, it becomes necessary to account in the flow control for latencies that are caused by delays due to the propagation of signals through the cable. Assuming a 5 nsec/m propagation delay, a round trip DWord propagation delay for a given transfer speed relative to the length of the cable is given in **Table 1**.

**Table 1:**

| 5 ns/m | 1m (5 ns one way) | | 2m (10 ns one way) | |
|---|---|---|---|---|
| | One way | Round | One way | Round |
| Gen1 (26.6 ns) | 0.188 (0) | (1) | 0.376 (1) | (2) |
| Gen2 (13.3 ns) | 0.375 (0) | (1) | 0.75 (1) | (2) |
| Gen3 (6.7 ns) | 0.75 (1) | (2) | 1.5 (2) | (4) |

Deleted: 0
Deleted: 0
Deleted: 1

The 1m cable length is characteristic of the SATA "i" mode. The 2m cable length is characteristic of the SATA "m" mode. The SATA-IO has already specified Gen3i mode (6G SATA "i" mode), and is in the process of defining the Gen3m mode (6G SATA "m" mode). For this reason, it is proposed here to modify the text that describes the required $HOLD_P$/$HOLDA_P$ behavior as stated in section 1.1.

## 1.1 Proposed change

The following changes shall be included in the Section **9.4.7 Flow control Signaling Latency** in the *Serial ATA Revision 2.6* specification document

There is a finite pipeline latency in a round-trip handshake across the Serial ATA interface. In order to avoid buffer overflow in flow control situations, the maximum tolerable latency from when a receiver sends a $HOLD_P$ until it receives the $HOLDA_P$ from the transmitter is specified. This allows the high-water mark to be set in the receive FIFO so as to avoid buffer overflow while avoiding excessive buffering/FIFO space.

In the case where the receiver wants to flow control the incoming traffic, it transmits $HOLD_P$ on the back channel. Some number of received DWords later, $HOLDA_P$ is received. The larger the latency between transmitting $HOLD_P$ until receiving $HOLDA_P$, the larger the receive FIFO needs to be. Within a single $HOLD_P$/ $HOLDA_P$ sequence, there shall be a maximum allowed latency from the time the MSB of the initial $HOLD_P$ is on the wire, until the MSB of the initial $HOLDA_P$ is on the wire. The LSB is transmitted first.

When operating at Gen1 and Gen2 transfer speeds, a receiver shall be able to accommodate reception of 20 DWords after the time it transmits $HOLD_P$ to the transmitter, and the transmitter shall respond with $HOLDA_P$ in response to receiving $HOLD_P$ within 20 DWords. The 20 DWord latency is not applicable to any subsequent transmissions of $HOLD_P$ within the same sequence. Upon each new instantiation of a $HOLD_P$/ $HOLDA_P$ sequence, the receiver and transmitter operating at Gen1 or Gen2 transfer speeds shall meet the 20 DWord latency specification.

When operating at Gen3 transfer speed, a receiver shall be able to accommodate reception of 24 DWords after the time it transmits $HOLD_P$ to the transmitter, and the transmitter shall respond with $HOLDA_P$ in response to receiving $HOLD_P$ within 20 DWords. This DWord latency is not applicable to any subsequent transmissions of $HOLD_P$ within the same sequence. Upon each new instantiation of a $HOLD_P$/ $HOLDA_P$ sequence, the receiver and transmitter operating at Gen3 transfer speed shall meet this DWord latency specification."

Deleted: second paragraph of
Deleted: issues
Deleted: signal
Deleted: signal
Deleted: "
Deleted: data
Deleted: characters
Deleted: valid data ceases, and
Deleted: characters
Deleted: are
Deleted: shall be no more than 20 DWord times.
Deleted: A receiver shall be able to accommodate reception of 20 DWords of additional data after the time it transmits the $HOLD_P$ flow control character to the transmitter, and the transmitter shall respond with a $HOLDA_P$ in response to receiving a $HOLD_P$ within 20 DWord times. The 20 DWord latency specification is not applicable to any subsequent transmissions of the $HOLD_P$ flow control character within the same sequence. Upon each new instantiation of a $HOLD_P$/ $HOLDA_P$ sequence, the receiver and transmitter shall meet the 20 DWord latency specification.
Deleted: "
Deleted: ¶

Deleted: 1
Deleted: 4
Deleted: 006
Deleted: 001
Deleted: 5
Deleted: .doc
Deleted: figure

There is no reference design in this specification. The specified maximum latency is based on the layers and states described throughout this document. It is recognized that the Link layer may have two separate clock domains -- transmit clock domain, and the receive clock domain. It is also recognized that a Link state machine could run at the Dword clock rate, implying synchronizers between three potential clock domains. In practice more efficient implementations would be pursued and the actual latencies may be less than indicated here. The figures represent an almost literal interpretation of the spec into logic design. A synchronizer is assumed to be a worst case of 2.99 clocks of any clock domain and is rounded to three whole clocks. The Serial ATA cable contains less than half of a Dword of content at Gen1i and Gen2i speeds with 1m internal cables, and is therefore negligible. For longer cable lengths, the effect of the cable should not be ignored. Two Dwords of pipeline delay are assumed for the Phy, and the FIFO is assumed to run at the Link state machine rate. No synchronization is needed between the two.

Deleted: HIGH SPEED SERIALIZED AT ATTACHMENT¶
Serial ATA International Organization¶
Serial ATA Revision 2.6 309

The following figure outlines the origin of the 20 Dword latency specification. The example illustrates the components of a round trip delay when the receiver transmits HOLDP on the link until reception of the HOLDAP from the transmitter. This corresponds to the number of Dwords that the receiver shall be able to accept after transmitting a HOLDP.

**Table 63 – Example of Components of a Round Trip Delay**

**Receiver Sends HOLDP**
1 Dword Convert to 40 bit data.
1 Dword 10b/8b conversion.
1 Dword De-scrambling.
3 Dwords Synchronization between receive clock, and Link state machine clock.
1 Dword Link state machine is notified that primitive has been received.
1 Dword Link state machine takes action.
1 Dword FIFO is notified of primitive reception.
1 Dword FIFO stops sending data to Link layer.
1 Dword Link is notified to insert HOLDAP.
1 Dword Link acts on notification and inserts HOLDAP into data stream.
1 Dword Scrambling.
1 Dword 8b/10b conversion.
1 Dword Synchronize to transmit clock (3 transmit clocks, which are four times the Link state machine rate)
1 Dword Convert to 10 bit data
2 Dwords Phy, transmit side
**HOLDAP on the Cable**