

**Proposed  
Draft**

**Serial ATA  
International Organization**

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**Serial ATA Technical Proposal: SATA3.2 TPR056**  
**Title: Enable new Power Disable feature on standard SATA connector P3**  
**Sponsors: HGST, Seagate**

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## Document History

Version	Date	Comments
01	01/17/2013	Initial release.
02	02/08/2013	Pull down resistor implementation scheme. Hard wired for SATA Power Disable feature.
03	02/18/2013	Updates.
04	03/26/2013	More updates, to make this proposal more clear, remove Set Feature.
05	03/26/2013	Major editorial revisions to physical section and introduction.
06	04/02/2013	More updates: not using "power-on-reset", move T10 material to the introduction section, update Figure yy
07	04/03/2013	Editorial change in Introduction, to remove power saving, modified Figure 266+1
08	07/31/2013	Synced with T10/13-174r1 and SAS3r05d: 1) split power disable hold time into separate minimum hold times for asserted and negated, changed $T_{HH}$ to $T_{HA}$ and $T_{HN}$ ; 2) split into two subtypes: (always enabled) and (enabled by command); 3) added SET FEATURES command; 4) added 'enabled' bit in IDENTIFY DEVICE data log; and 5) updated reference to SAS-3 table.
09	11/12/2013	Synced with SAS3r06 (final, forwarded to INCITS): 1) removed example circuit diagram; 2) requires host to actively negate; and 3) simplifies the definition.
10	12/03/2013	Changes made include: 1) indicate that Power Disable and DevSleep are mutually exclusive; 2) indicate interactions of the Power Disable Enabled bit with various resets; and 3) change the bit assignments to avoid conflict with ECN 174.
11	12/16/2013	Changes made include: 1) Misc editorial (grammar, style guide) corrections from the Technical Editor; 2) changed table 5 footnotes to match the style guide requirements; 3) added: if devsleep supported, then power disable feature always enabled shall be cleared to zero; and 4) added: if power disable feature always enabled is set to one, then devsleep supported shall be cleared to zero.
12	12/18/2013	Member Review. Changed TPR C116 to TPR056.
13	03/03/2014	Member review comment resolution.

## Introduction

Seagate introduced a new device power management feature, Power Disable, in T10. This new T10 feature enables the initiator or expander to disable power to the SAS device circuitry within the SAS device. The Power Disable signal is on pin P3.

If the storage device has encountered a hung interface condition, then the device Power Disable feature provides the host system a “power-off” control without having to support independent supply voltage switching to every receptacle connector or require physical removal and insertion of the device from the connector. Since many SATA storage devices, especially high capacity ones deployed in storage systems, are installed in SAS backplanes, it is important that this T10 Power Disable feature also be standardized and available for SATA devices to implement.

Currently the SATA pin P3 is defined as the DEVSLP signal, an optional host controlled signal to the SATA device requesting the SATA device to enter the lowest possible power state. For some applications it is important for the SATA device to be able to support the Power Disable feature.

There are several differences between Device Sleep and Power Disable. A significant difference is that when host is asserting Device Sleep control signal to the SATA device, some power is still applied to the SATA device circuitry and recovery does not include a complete power-on sequence. Recovery from Power Disable initiates a power-on sequence.

Since SATA pin P3 is currently defined for the DEVSLP signal, this proposal defines an alternate use of pin P3 for the Power Disable control signal (PWDIS). Since Power Disable and Device Sleep are asserted by the same voltage level on P3, these two features are mutually exclusive.

This Technical Proposal defines two versions of this feature:

a) ~~1~~ always enabled:

- A) ~~a~~ indicates “supported” in the IDENTIFY DEVICE data log at power on reset;
- B) ~~b~~ indicates “enabled” in the IDENTIFY DEVICE data log at power on reset; and
- C) ~~c~~ does not provide an option to turn off the function or support DEVSLP;

and

b) ~~2~~ enabled by command:

- A) ~~a~~ has the same device internal pull-up that the DevSleep feature specifies;
- B) ~~b~~ indicates “supported” in the IDENTIFY DEVICE data log at power on reset;
- C) ~~c~~ indicates “disabled” in the IDENTIFY DEVICE data log at power on reset; and
- D) ~~d~~ may be enabled via a new SET FEATURES subcommand.

## Background T10 material

Refer to SAS-3 revision 6, section 5.10.

## Technical Specification Changes

The following additions are based on the content of Serial ATA Revision 3.2 Gold. Proposed additions to SATA 3.2 text are marked in blue underline. Proposed deletions to SATA 3.2 text are marked in ~~red strikethrough~~. Black text is the original SATA 3.2 text. Section headers correspond to the section in SATA 3.2 into which the proposed text is to be inserted.

## ■ <4> Definitions, abbreviations, and conventions

[Editor's note: Please add this definition and abbreviation to subclause 4.1.1]

### 4.1.1.1 <4.1.1.101> port address

### 4.1.1.2 <4.1.1.101+1> [Power Disable](#)

[Feature that disables power to the SATA device circuitry within the SATA device when power is present at the SATA device power connector.](#)

### 4.1.1.3 <4.1.1.105> protocol-based port selection

### 4.1.1.4 <4.1.1.105+1> [PWDIS](#)

[Power Disable control signal.](#)

## ■ <5> General overview

## ■ <6> Cables and Connectors

### 6.1 <6.1> Cables and Connectors overview

### 6.2 <6.2> Internal cables and connectors

### ■ <6.2.3> Mating interfaces

#### 6.2.1.1 <6.2.3.2> Standard SATA connector (3.5 inch & 2.5 inch HDD)

[Editor's note: Please make these changes to Table 5]

**Table 5 4– Standard SATA connector (3.5 inch & 2.5 inch HDD)**

	Name	Type	Description	Cable Usage <sup>b c</sup>	Backplane Usage <sup>c</sup>
Signal Segment Key					
Signal Segment	S1	GND		1 <sup>st</sup> Mate	2 <sup>nd</sup> Mate
	S2	A+	Differential Signal Pair A	2 <sup>nd</sup> Mate	3 <sup>rd</sup> Mate
	S3	A-		2 <sup>nd</sup> Mate	3 <sup>rd</sup> Mate
	S4	GND		1 <sup>st</sup> Mate	2 <sup>nd</sup> Mate
	S5	B-	Differential Signal Pair B	2 <sup>nd</sup> Mate	3 <sup>rd</sup> Mate
	S6	B+		2 <sup>nd</sup> Mate	3 <sup>rd</sup> Mate
	S7	GND		1 <sup>st</sup> Mate	2 <sup>nd</sup> Mate
Signal Segment "L"					
Central Connector Gap <sup>d</sup>					
Power Segment "L"					
Power Segment	P1	Retired <sup>e†</sup>		2 <sup>nd</sup> Mate	3 <sup>rd</sup> Mate
	P2	Retired <sup>e†</sup>		2 <sup>nd</sup> Mate	3 <sup>rd</sup> Mate
	P3	<a href="#">PWDIS<sup>e g/</sup></a> <a href="#">DEVSLP<sup>e†</sup></a>	<a href="#">Enter/Exit Power Disable/</a> <a href="#">Enter/Exit DevSleep</a>	1 <sup>st</sup> Mate	2 <sup>nd</sup> Mate
	P4	GND		1 <sup>st</sup> Mate	1 <sup>st</sup> Mate
	P5	GND		1 <sup>st</sup> Mate	2 <sup>nd</sup> Mate
	P6	GND		1 <sup>st</sup> Mate	2 <sup>nd</sup> Mate
	P7	V <sub>5</sub>	5 V Power, Pre-charge	1 <sup>st</sup> Mate	2 <sup>nd</sup> Mate
	P8	V <sub>5</sub>	5 V Power	2 <sup>nd</sup> Mate	3 <sup>rd</sup> Mate
	P9	V <sub>5</sub>	5 V Power	2 <sup>nd</sup> Mate	3 <sup>rd</sup> Mate
	P10	GND		1 <sup>st</sup> Mate	2 <sup>nd</sup> Mate
	P11	DAS/DSS/DHU	Device Activity Signal / Disable Staggered Spinup/ Direct Head Unload / Vendor Specific <sup>a</sup>	2 <sup>nd</sup> Mate	3 <sup>rd</sup> Mate
	P12	GND		1 <sup>st</sup> Mate	1 <sup>st</sup> Mate
	P13	V <sub>12</sub>	12 V Power, Pre-charge	1 <sup>st</sup> Mate	2 <sup>nd</sup> Mate
	P14	V <sub>12</sub>	12 V Power	2 <sup>nd</sup> Mate	3 <sup>rd</sup> Mate
	P15	V <sub>12</sub>	12 V Power	2 <sup>nd</sup> Mate	3 <sup>rd</sup> Mate
Power Segment Key					
<p><sup>a</sup> For specific optional usage of pin P11 (see 6.13).</p> <p><sup>b</sup> Although the mate order is shown, hot plugging is not supported when using the cable connector receptacle.</p> <p><sup>c</sup> All mate sequences assume zero angular offset between connectors.</p> <p><sup>d</sup> The signal segment and power segment may be separate.</p> <p><sup>e</sup> Previous versions of this specification assigned 3.3 V to pins P1, P2, and P3. In addition, device plug pins P1, P2, and P3 were required to be bused together.</p> <p><sup>f</sup> <a href="#">If using DEVSLP, it is recommended to have P1 and P2 tied together for purpose of legacy functionality. Pin P3 should be a no-connect if DEVSLP is not implemented.</a></p> <p><sup>g</sup> <a href="#">If using PWDIS, it is recommended to have P1 and P2 tied together for the purpose of legacy functionality.</a></p>					

## **<7> Phy layer**

## **<8> OOB and phy power states**

[Editor's note: Modify section 8.5.1.2 as noted below]

### **8.5.1.2 Device requirements for DEVSLP**

If the Device Sleep feature is supported (i.e., IDENTIFY DEVICE data Word 78 bit 8 is set to one), then the requirements specified in this sub-clause shall apply.

Since the Power Disable feature (see 8.6) and the Device Sleep feature both use pin P3, these features are mutually exclusive.

After power up, the device shall ignore DEVSLP until the Device Sleep feature is enabled by a SET FEATURES command from the host (see 13.3).

...  
...

[Editor's note: Add this new section 8.6 to clause 8]

## **8.1 <8.6> Power Disable Signal Protocol and Timing**

### **<8.6.1> Power Disable Feature Overview**

The Power Disable feature, if supported and enabled, may be used to disable power to the device circuitry.

Since the Power Disable feature and the Device Sleep feature (see 8.5) both use pin P3, these features are mutually exclusive.

If the Power Disable feature is supported, then the device shall set IDENTIFY DEVICE data Word 78 bit 12 to one.

If the Power Disable feature is supported and the POWER DISABLE FEATURE ALWAYS ENABLED bit (see 13.7.9.2.28):

- a) is set to one, then the Power Disable feature is always enabled; or
- b) is cleared to zero, then the Power Disable feature:
  - A) shall be disabled as a result of processing a power on reset;
  - B) shall not be affected as a result of processing a hardware reset or a software reset; and
  - C) may be enabled as a result of processing a SET FEATURES Enable/Disable Power Disable Feature subcommand (see 13.3.12).

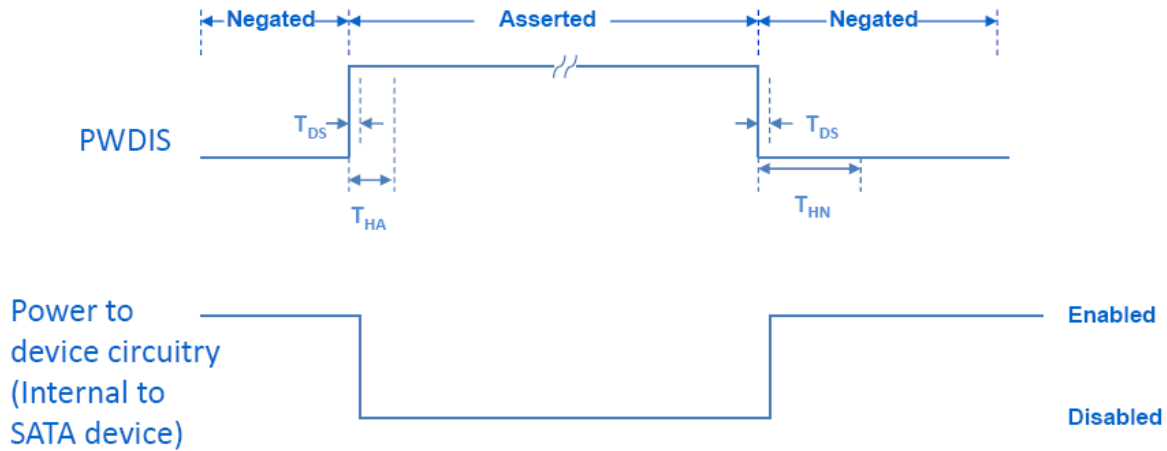
If the Power Disable feature is supported and enabled, then the device shall:

- a) ~~set IDENTIFY DEVICE data Word 78 bit 12 to one to indicate that the Power Disable feature is supported;~~
- b) allow power to be applied to the device circuitry if the PWDIS signal is not connected on the host connector;
- c) allow power to be applied to the device circuitry if the PWDIS signal is negated as defined in Table 81+1;
- d) disable power applied to the device circuitry if:
  - 1) the minimum negated hold time in Table 81+1 is met; and
  - 2) the PWDIS signal is asserted as defined in Table 81+1;
- e) perform the actions defined for a power on reset if:

- 1) the minimum negated hold time in Table 81+1 is met;
  - 2) the PWDIS signal is asserted as defined in Table 81+1; and
  - 3) the PWDIS signal transitions from asserted to negated;
- and
- f) not respond to a change of the PWDIS signal from negated to asserted or asserted to negated until the PWDIS signal is held at the asserted or negated level for a minimum of 1 us.



Figure 266+1 provides an overview of the Power Disable protocol. See 6.2.3.2-6.1.3.2 for additional requirements.



**Figure 266+1 – POWER DISABLE PROTOCOL OVERVIEW**

All voltages and currents in Table 81+1 are measured at the PWDIS pin (i.e., P3) on the device connector.

Table 81+1 - Characteristics of the PWDIS signal applied to the device

Parameter	Characteristic	Units	Minimum	Maximum
$V_{DIn}$	Absolute maximum voltage input range.	V	-0.5	3.6
$V_{HNegate}$	Negated voltage (power enabled) <sup>a b</sup>	V	-0.5	0.7
$V_{HAssert}$	Asserted voltage (power disabled) <sup>c</sup>	V	2.1	3.6
$A_{DSSCC}$	Driver sink/source current capability <sup>b c</sup>	uA	100	-
$T_{HA}$	PWDIS asserted hold time <sup>d e</sup>	s	5.0	-
$T_{HN}$	PWDIS negated hold time <sup>d e</sup>	s	30.0	-

<sup>a</sup> The device shall allow power to be applied to the device circuitry if P3 is not connected on the host connector.  
<sup>b</sup> The PWDIS signal shall be actively negated.  
<sup>c</sup> The PWDIS signal shall be actively asserted.  
<sup>d</sup> The hold time is the length of time the PWDIS signal is asserted or negated. The length of time after the PWDIS signal is asserted or negated until the disabling or allowing of power to the device circuitry is vendor specific.  
<sup>e</sup> The PWDIS signal should not transition from negated to asserted or asserted to negated for the negated hold time:  
 a) after power is applied to the host connector; or  
 b) after the detection of a hot plug event.

## █ <9> Link layer

## █ <10> Transport layer

## █ <11> Device command layer protocol

## █ <12> Host command layer protocol

## █ <13> Application Layer

### 13.1 <13.2> IDENTIFY (PACKET) DEVICE

#### █ <13.2.2> IDENTIFY DEVICE

##### 13.1.1.1 <13.2.2.1> IDENTIFY DEVICE information

[Editor's note: Make the following changes to words 77, 78, and 79 of the IDENTIFY DEVICE data]

**Table 100 – IDENTIFY DEVICE information**

(part 2 of 4) and (part 3 of 4)

Word	O/M	F/V	
...	...	...	...
77	O	R F	Serial ATA Additional capabilities 15.. <del>8</del> <u>9</u> Reserved <u>8</u> <a href="#">Power Disable feature always enabled</a>
78	O	R F	Serial ATA features supported 15.. <del>12</del> <u>13</u> Reserved <u>12</u> <a href="#">Supports Power Disable feature</a>
79	O	R V R/V	Serial ATA features enabled 15..12 Reserved 11 Rebuild Assist enabled 10 <del>Reserved</del> <a href="#">Power Disable feature enabled</a>
Key: M = Support of the word is mandatory. O = Support of the word is optional. F = the content of the bit, field, or word is fixed and does not change. For removable media devices, these values may change when media is removed or changed. V = the contents of the bit, field, or word is variable and may change depending on the state of the device or the commands executed by the device. R = the content of the bit, field, or word is reserved and shall be zero.			

**13.1.1.2 <13.2.2.18> Word 77: Serial ATA Additional Capabilities**

Word 77 reports additional optional capabilities supported by the device. Support for this Word is optional and if not supported, the Word shall be cleared to zero indicating the device has no support for Serial ATA additional capabilities.

....

Bits 15:~~8~~9 are reserved.

Bit 8 is a copy of the POWER DISABLE FEATURE ALWAYS ENABLED bit (see 13.7.9.2~~3~~.28).

...

**13.1.1.3 <13.2.2.19> Word 78: Serial ATA Features Supported**

...

Bits 15:~~12~~13 are reserved.

Bit 12 is a copy of the POWER DISABLE FEATURE SUPPORTED bit (see 13.7.9.2.27).

...

**13.1.1.4 <13.2.2.20> Word 79: Serial ATA features enabled**

....

Bits 15:12 are reserved.

Bit 11 is a copy of REBUILD ASSIST ENABLED bit (see 13.7.9.3.11).

Bit 10 is ~~reserved~~ a copy of the POWER DISABLE FEATURE ENABLED bit (see 13.7.9.3.14).

...

[Editor's note: make the following changes to SET FEATURES, subclause 13.3 ]

## 13.2 <13.3> SET FEATURES

### <13.3.1> SET FEATURES overview

....

[Editor's note: Make the following changes to SET FEATURES, Table 103]

**Table 103 – Feature identification values**

Count(7:0) Value	Description
00h	Reserved
01h	Non-zero buffer offset in DMA Setup FIS
02h	DMA Setup FIS Auto-Activate optimization
03h	Device-initiated interface power state transitions
04h	Guaranteed In-Order Data Delivery
05h	Asynchronous Notification
06h	Software Settings Preservation
07h	Device Automatic Partial to Slumber transitions
08h	Enable Hardware Feature Control
09h	Enable DevSleep
0Ah	Enable/Disable Hybrid Information
0Bh	<a href="#">Enable/Disable Power Disable feature</a>
<del>0Ch..0Bh</del> –FFh	Reserved for future Serial ATA definition

....

[Editor's note: Modify section 13.3.10 as noted below ]

### 13.3.10 Enable/disable Device Sleep

A Count(7:0) value of 09h is used by the host to enable or disable Device Sleep. If the value in Features(7:0) is set to 10h, then the device shall set IDENTIFY DEVICE data Word 79, bit 8, to one. If the value in Features (7:0) is set to 90h, then the device shall clear IDENTIFY DEVICE data Word 79, bit 8, to zero. As a result of processing a power on reset, the Device Sleep feature shall be disabled.

If:

- a) the host attempts to enable or disable the Device Sleep feature; and
- b) the Device Sleep feature is not supported (i.e., IDENTIFY DEVICE data Word 78 bit 8 is cleared to zero),

then the device shall return command aborted.

If the host attempts to enable Device Sleep and the Power Disable feature is:

- a) enabled (i.e., IDENTIFY DEVICE data Word 79 bit 10 is set to one); or
- b) always enabled (i.e., IDENTIFY DEVICE data Word 77 bit 8 is set to one).

then the device shall return command aborted.

[Editor's note: Add the following new section to subclause 13.3 ]

### **<13.3.12> Enable/Disable Power Disable Feature**

A Count(7:0) value of 0Bh is used by the host to enable or disable the Power Disable feature (see 8.6).

If the POWER DISABLE FEATURE SUPPORTED bit (see 13.7.9.2.27) is cleared to zero, then the device shall return command aborted.

If the host specified that the Power Disable feature is to be:

- a) enabled and the Device Sleep feature is enabled; or
- b) disabled and the POWER DISABLE FEATURE ALWAYS ENABLED bit (see 13.7.9.2.28) is set to one,  
then the device shall return command aborted.

If the host specified that the Power Disable feature is to be:

- a) disabled and the POWER DISABLE FEATURE ENABLED bit (see 13.7.9.3.14) is cleared to zero;
- b) enabled and the POWER DISABLE FEATURE ENABLED bit is set to one; or
- c) enabled and the POWER DISABLE FEATURE ALWAYS ENABLED bit is set to one,  
then the device shall return command completion with no error.

If the host specified that the Power Disable feature is to be enabled and the POWER DISABLE FEATURE ENABLED bit is cleared to zero, then the device shall:

- 1) enable the Power Disable feature;
- 2) set the POWER DISABLE FEATURE ENABLED bit to one; and
- 3) return command completion with no error.

[\[Editor's note: Modify the IDENTIFY DEVICE Data Log as noted below\]](#)

**13.7.9.1 Serial ATA settings (page 08h)**

The Serial ATA log page (see Table 118) provides information about the Serial ATA Transport.

**Table 118 – Serial ATA (page 08h)**

Offset	Type			
...				
8..15	QWord	SATA Capabilities		
		Bit	Meaning	
		63	Shall be set to one	
		62: <del>29</del> 32	Reserved	
		31	<a href="#">POWER DISABLE FEATURE ALWAYS ENABLED (see 13.7.9.2.28)</a>	
		30	<a href="#">POWER DISABLE FEATURE SUPPORTED (see13.7.9.2.27)</a>	
		29	<a href="#">REBUILD ASSIST SUPPORTED (see 13.7.9.2.26)</a> <a href="#">Editor's note: ECN075 assigned bit 29 to REBUILD ASSIST SUPPORTED.</a>	
		28	DIPM SSP PRESERVATION SUPPORTED (see 13.7.9.2.25)	
		27	<a href="#">HYBRID INFORMATION SUPPORTED (see 13.7.9.2.24)</a> <a href="#">Editor's note: ECN075 assigned bit 27 to HYBRID INFORMATION SUPPORTED.</a>	
		26	DEVSLEEP TO REDUCEDPWRSTATE CAPABILITY SUPPORTED (see 13.7.9.2.23)	
		25	DEVICE SLEEP SUPPORTED (see 13.7.9.2.22)	
		...		
		16..23	QWord	Current SATA Settings
Bit	Meaning			
63	Shall be set to one			
62: <del>4</del> 12	Reserved			
11	<a href="#">POWER DISABLE FEATURE ENABLED (see 13.7.9.3.14)</a>			
10	DEVICE SLEEP ENABLED (see 13.7.9.3.9)			
...				

.....

### 13.2.2.1 <13.7.9.2> SATA capabilities

#### 13.2.2.1.1 <13.7.9.2.22> DEVICE SLEEP SUPPORTED bit

If the DEVICE SLEEP SUPPORTED bit is set to one, then:

- a) the device supports the Device Sleep feature;
- b) the device shall support the Identify Device data log; ~~and~~
- c) the DEVSLP TIMING VARIABLES SUPPORTED bit (see 13.7.9.4.1) shall be set to one; ~~and~~
- d) the POWER DISABLE FEATURE ALWAYS ENABLED bit (see 13.7.9.2.28) shall be cleared to zero.

If the DEVICE SLEEP SUPPORTED bit is cleared to zero, then:

- a) the device does not support the Device Sleep feature.

IDENTIFY DEVICE data Word 78 bit 8 is a copy of this field.

NOTE 71 – If the DEVICE SLEEP SUPPORTED bit is cleared to zero, then the host ignores the DEVSLEEP TO REDUCEDPWRSTATE CAPABILITY SUPPORTED bit and the DEVSLP TIMING VARIABLES SUPPORTED bit.

#### 13.2.2.1.2 <13.7.9.2.27> POWER DISABLE FEATURE SUPPORTED bit

If the POWER DISABLE FEATURE SUPPORTED bit is set to one, then the device supports Power Disable (see 8.6).

If the POWER DISABLE FEATURE SUPPORTED bit is cleared to zero, then:

- a) the device does not support the Power Disable feature;
- b) the POWER DISABLE FEATURE ALWAYS ENABLED bit (see 13.7.9.2.28) shall be cleared to zero; and
- c) the POWER DISABLE FEATURE ENABLED bit (see 13.7.9.3.14) shall be cleared to zero.

IDENTIFY DEVICE data Word 78 bit 12 is a copy of this field.

#### 13.2.2.1.3 <13.7.9.2.28> POWER DISABLE FEATURE ALWAYS ENABLED bit

If the POWER DISABLE FEATURE ALWAYS ENABLED bit is set to one, then:

- a) the Power Disable feature is always enabled (see 8.6);
- b) the DEVICE SLEEP SUPPORTED bit (see 13.7.9.2.22) shall be cleared to zero;
- c) the POWER DISABLE FEATURE ENABLED bit (see 13.7.9.3.14) shall be set to one; and
- d) the value of the POWER DISABLE FEATURE ALWAYS ENABLED bit and the value of the POWER DISABLE FEATURE ENABLED bit shall persist across all resets.

If the POWER DISABLE FEATURE ALWAYS ENABLED bit is cleared to zero and the POWER DISABLE FEATURE SUPPORTED bit (see 13.7.9.2.27) is set to one, then the Power Disable feature may be enabled using the SET FEATURES Enable/Disable Power Disable Feature subcommand (see 13.3.12).

IDENTIFY DEVICE data Word 79 bit 10 is a copy of this field.

### 13.2.2.2 <13.7.9.3> Current SATA Settings

#### 13.2.2.2.1 <13.7.9.3.14> POWER DISABLE FEATURE ENABLED bit

If the POWER DISABLE FEATURE ENABLED bit is set to one, then the Power Disable feature is enabled (see 8.6).

If the POWER DISABLE FEATURE ENABLED bit is cleared to zero, then the Power Disable feature is disabled.

If the POWER DISABLE FEATURE ALWAYS ENABLED bit is cleared to zero, after processing:

- a) a power-on reset, the value of the POWER DISABLE FEATURE ENABLED bit shall be cleared to zero;
- b) a hardware reset, the value of the POWER DISABLE FEATURE ENABLED bit shall not be changed; and
- c) a software reset, the value of the POWER DISABLE FEATURE ENABLED bit shall not be changed.

IDENTIFY DEVICE data Word 77 bit 8 is a copy of this field.