

**Proposed
Draft**

**Serial ATA
International Organization**

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**Serial ATA Technical Proposal TPR_059
Title: Emphasis Control for SATA Interface**

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Document History

Version	Date	Comments
0	5/16/2014	Initial release.
1	5/23/2014	Changed some paragraph headings to comply with Style Guide requirements. Added another figure so that there are now separate figures for host and device test setups
2	6/3/2014	Constrained the proposal to make clear that it does not apply to applications using certain connectors/interfaces. Reiterated that the host requirement applies with all interconnects in place between the host and device
3	6/5/2014	Identified as TPR_059. Added a heading to show where the proposed changes section begins. Added changes to 5.3.11.1 and 7.2.4. Added Internal 4-lane cable to the list of excluded applications. Measurement made at the mated device connector, but not necessarily on the device side of the connector. In 7.6.33.3, A, B, C, and D are all = x^x , instead of just C and D.
4	6/10/2014	Deleted extraneous wording in the introduction. Corrected some MS Word formatting. Added informative 0dB nominal host emphasis for Gen1 and Gen2 to Table 54. Clarified that informative Gen1 and Gen2 emphasis is also measured at the device connector. Revised the measurement method to get a better measurement of the emphasized bit. Removed final two sentences from Section 7.6.33.3 as they are not applicable.
5	6/20/2014	Added clarification to 7.4.3.3.14 that the Tx emphasis requirement does not apply at intermediate compliance points within the usage model channel (e.g., the internal 4-lane cable connector). Added Gen "u" applications. Added requirement to Table 55 to account for added Gen "u" apps. Changed measurement to a combination HFTP/LFTP method. Changed maximum host emphasis to 1dB to account for the new method.
6	6/25/2014	Changed maximum host emphasis to 1.5dB. Added reference to Table 55 in 7.6.33.1 and 7.6.33.2.1. Changed reference to MFTP in 7.6.33.2.1 to instead reference HFTP/LFTP. Clarified that inequalities in 7.6.33.3, Step 5, are all "or equal to".
7	6/25/2014	Reordered the wording in Table 54, footnote 2, to be more grammatically correct. Removed "internal 4-lane cable connector" from the list in 7.4.3.3.14 since it is already discussed in the text preceding the list.
8	8/4/2014	Made editorial corrections to various typos, placement of text, and grammatical mistakes. No changes made to the intent or substance of the proposal.
9	8/25/2014	Changed Device emphasis limits in Table 54. Changed the Host TX requirement for cabled applications to include the CIC

Introduction

The SATA spec does not specify Tx emphasis. The realities of today's marketplace dictate that this shortcoming be rectified due to the recent introduction of extremely challenging host architectures equipped with chipsets providing extensive programmability of both Tx emphasis and Rx equalization, accompanied by confusion on the part of implementers as to how this emphasis and equalization should be programmed. A standardized solution is needed. The proposed approach is to specify Tx emphasis in the SATA specification. The compliance point is proposed to be the device connector. The proposed target value for Gen3 device Tx emphasis is 2 dB \pm 1 dB at the device connector. The proposed target value for Gen3 host Tx emphasis is 0 dB +1.5 dB/-2 dB at the device connector. Gen1 and Gen2 device emphases are not specified, but instead have informative recommended values.

This proposal is being presented by Western Digital, Seagate, and Intel.

Make the following Changes to SATA 3.2. Added text is in blue underline. Deleted text is in ~~red~~ ~~strikeout~~. Existing text is in black.

5.3.11.1 Mobile applications overview

Applications and compliance points for Serial ATA devices within or connected to mobile computers are not defined in this document, except where otherwise specified. If any proprietary cables/connectors or electrical specifications are developed for this application, the system shall be designed so as to prevent connection with standard SATA components. If standard cables/connectors/electrical interfaces are used within the mobile computer, within the docking bay or to external storage components, these shall comply with the applicable requirements in this specification and interoperate properly with Serial ATA components.

7.2.4 Compliance testing

This specification provides electrical specifications that if met by hosts, devices, and interconnects, satisfy the link performance specifications if combined into a system. This section provides an overview of how to determine whether a Host, Device, or Interconnect is compliant to the specifications of this specification.

Each electrical specification requires a specific measurement, test setup and data patterns. This section ties all of these requirements together to aid the reader in understanding what is needed for compliance testing.

Table 52, Table 53, Table 54, Table 55, Table 56, Table 57, Table 58, and Table 59 detail the electrical requirements for SATA compliance. Each requirement as defined in 7.4.3. Jitter as defined in 7.5. Measurement methods for each specification with details as given in 7.6. See 7.7 discuss Interface States relating to OOB and power management. See 6.12 describe the Interconnect requirements.

The Phy layer is divided into a transmitter, interconnect, and a receiver.

The SATA link is a full duplex point to point link as continuous data activity exists on each direction. For purposes of compliance testing of Hosts and Devices, the full duplex link is broken into two simplex links, one for the Host transmitting to the Device and the other for the Device transmitting to the Host. Each link is tested for compliance separately.

Each transmitter to receiver Link contains the following elements:

- a) transmitter (IC/PCB/SATA Connector);
- b) interconnect (Connector/Cable or PCB/Connector); and
- c) receiver (SATA Connector / PCB / IC).

In testing the compliance of SATA components that make up a system there are five Compliance Areas to be measured:

a) "Transmitted Signal"— examine the transmitted signal quality at the compliance point for the Host/Device into a Laboratory Load. Electrical specifications include amplitude, rise/fall time, frequency, jitter, etc. The Electrical specifications apply to the signal output from the Transmitter-Under-Test at the mated connector when driving a Laboratory Load. Unless a particular measurement requirement states otherwise, no attempt has been made to specify the signal while attached to a cable, backplane or directly into another Device. Actual signals "In-System" may vary;

b) "Transmitter" examine all specified characteristics of the Transmitter from the compliance point. This includes specifications for differential and common-mode impedance. The "Transmitter" includes the IC that incorporates the transmitter, the PCB, the SATA connector as well as any additional components between the IC and the SATA connector;

c) "Receiver" examine all specified characteristics of the Receiver from the compliance point. This includes specifications for differential and common-mode impedance. The "Receiver" includes the SATA connector, the PCB and the IC that incorporates the receiver as well as any additional components between the IC and the SATA connector;

d) "Receiver Tolerance" The Receiver is presented with a worst-case "lab-sourced signal", and operating with its active transmitter, shall meet the specified Frame Error Rates. This requires carefully controlled signal sources in order to generate a worst-case signal;and

e) "Interconnect" examine all specified characteristics of the interconnect, using test equipment. The interconnect includes SATA connector pairs at each end. The testing requirements and procedures according to 6.12.

In order to determine compliance to this specification, measurements shall be performed separately (unless otherwise specified) with Host, Device, or Interconnect being tested when connected to test equipment. Compliance tests are not done with a Host, Device, or Interconnect connected together unless required by a particular measurement. Unless otherwise specified, all compliance measurements shall be taken through the mated connector pair.

NOTE 20 - The electrical specifications in the Receiver Tolerance Table do not describe the characteristics of the received signal; these describe the lab-sourced signal calibrated into a Laboratory Load and subsequently applied to the Receiver. The Receiver Tolerance Table does not describe the characteristics of a signal from a Transmitter through an Interconnect into a Laboratory Load. Received signals in a system are potentially worse due to the non-ideal impedance match of the transmitter and the receiver.

(Editor's note: add the following to Table 54)

Parameter	Units	Limit	Gen1i	Gen1m	Gen2i	Gen2m	Gen3i	Detail Cross-Ref Section	Measurement Cross-Ref Section
V _{EmphasisDevice} Device TX Emphasis ^{a, b}	dB	Min	-	-	-	-	0.5	7.4.3.3.14	7.6.33
		Nom	-	-	-	-	2		
		Max	-	-	-	-	2.5		
V _{EmphasisHost} Host TX Emphasis ^{a, c}	dB	Min	-	-	-	-	-2	7.4.3.3.14	7.6.33
		Nom	0	-	0	-	0		
		Max	-	-	-	-	1.5		

^a TX emphasis is measured at the mated Serial ATA connector at the device. Unless otherwise specified, no CIC is used for this measurement.

^b The TX emphasis requirement does not apply to the Internal 4-lane cable mated to a backplane or devices using the Internal LIF-SATA connector, the SATA MicroSSD interface, or the Internal M.2 connector. Tx emphasis for these cases is vendor specific.

^c This measurement includes the channel between the host IC and the device connector (e.g., motherboard, backplane, cable, and connectors). For internal 1 m cabled host to device applications (see section 5.3.2), the CIC is substituted for the actual system cable.

(Editor's note: add the following to Table 55)

Parameter ¹	Units	Limit	Gen1u	Gen2u	Gen3u ³	Detail Cross-Ref Section ^{2,3}	Measurement Cross-Ref Section ^{2,3}
V _{EmphasisHost} Host TX Emphasis	dB	Min	-	-	-2	7.4.3.3.14	7.6.33
		Nom	0	0	0		
		Max	-	-	1.5		

7.4.3.3.14 Tx emphasis

7.4.3.3.14.1 Tx emphasis (Gen3i, Gen3u)

The emphasis measured at the transmitter shall comply with the respective electrical specifications as defined in Table 54 and Table 55.

For both host and device, Tx emphasis is measured at the mated Serial ATA connector at the device (unless otherwise specified). The Tx emphasis requirement does not apply at intermediate compliance points within the usage model channel (e.g., the internal 4-lane cable connector). Unless otherwise specified, no CIC is used for this measurement.

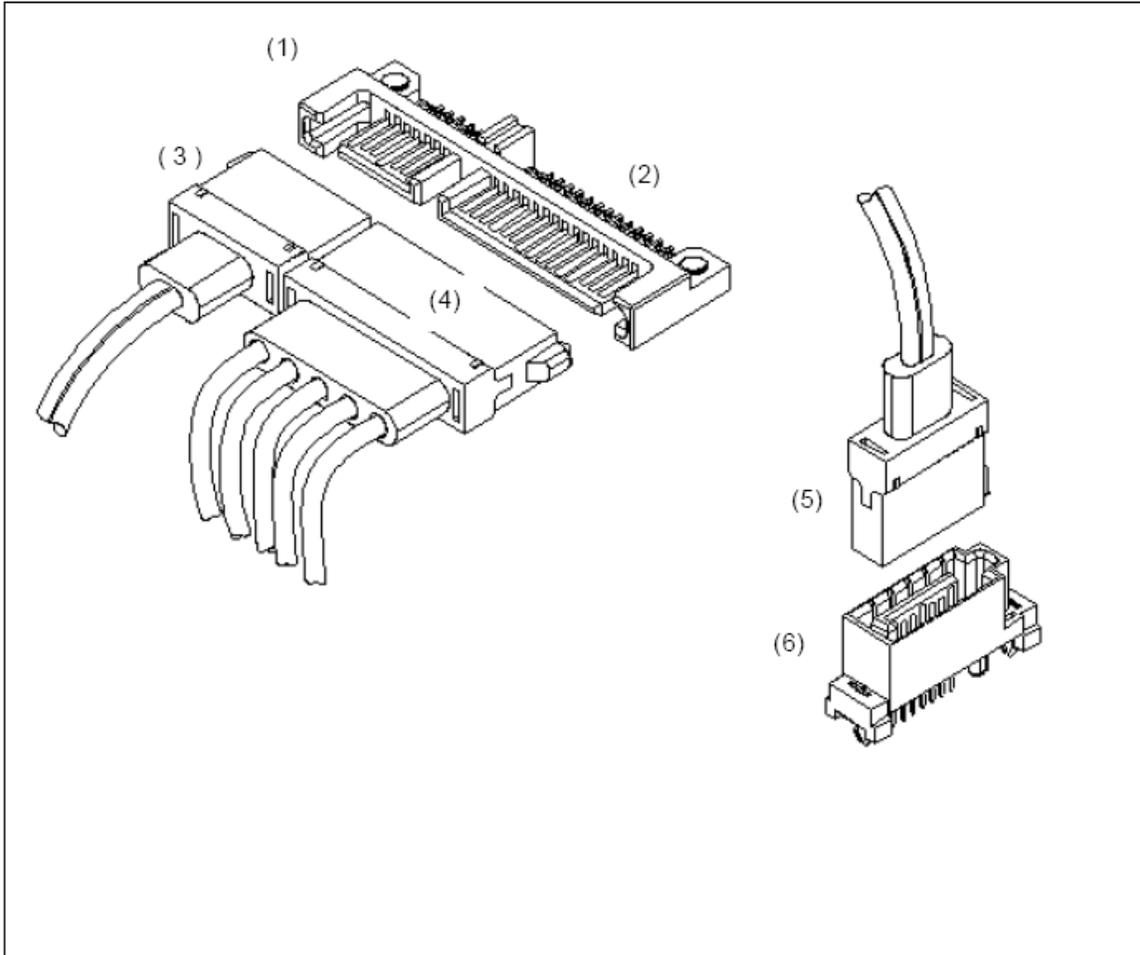
The TX emphasis requirement does not apply to devices using or mating with the following:

- a) Internal LIF-SATA connector (see 6.5);
- b) SATA MicroSSD interface (see 6.8); or
- c) Internal M.2 connector (see 6.9).

TX emphasis for these devices is vendor specific.

7.4.3.3.14.2 Host Tx emphasis requirement for internal 1 m cabled host to device applications (Gen3i)

For connection via a standard SATA internal cable (see section 5.3.2), the device signal plug connector, shown as (1) in Figure TBD, mates with the signal cable receptacle connector on one end of the cable, illustrated as (3) in Figure TBD. The signal cable receptacle connector on the other end of the cable is inserted into a host signal plug connector (see section 6.2.5), shown as (6) in Figure TBD. The signal cable wire consists of two twinax sections in a common outer sheath. When an application connects in this fashion, compliance with the host emphasis requirement shall be met by measuring the emphasis with the CIC rather than with the actual system cable.



Key:

- 1 = device signal plug segment or connector
- 2 = device power plug segment or connector
- 3 = signal cable receptacle connector, to be mated with (1)
- 4 = power cable receptacle connector, to be mated with (2)
- 5 = signal cable receptacle connector, to be mated with (6)
- 6 = the host signal plug connector

Figure TBD – Internal 1m cabled host to device applications SATA connector examples

7.4.3.3.14.3 Device Tx emphasis (Gen1i, Gen2i) (informative)

The purpose of the Gen1 and Gen2 emphasis recommendation is to optimize signal integrity by adjusting the transmitted signal in such a way that it compensates for losses in the interconnect channel. The particular implementation of emphasis is vendor specific. Since generally less emphasis is needed to compensate for losses at Gen1 and Gen2 than is needed for Gen3, it is recommended for devices with the capability of programming different levels of emphasis for different transfer rates that Gen2 device emphasis be limited to no more than 1.5 dB at the device connector and Gen1 device emphasis be limited to no more than 1 dB at the device connector.

7.4.3.3.14.4 Host Tx emphasis (Gen1i, Gen1u, Gen2i, Gen2u) (informative)

The purpose of the Gen1 and Gen2 emphasis recommendation is to optimize signal integrity by adjusting the transmitted signal in such a way that it compensates for losses in the interconnect channel. The particular implementation of emphasis is vendor specific. Since generally less emphasis is needed to compensate for losses at Gen1 and Gen2 than is needed for Gen3, it is

recommended for hosts with the capability of programming different levels of emphasis for different transfer rates that Gen1 and Gen2 host emphasis be limited to no more than 1 dB at the device connector.

7.6.33 Transmitter emphasis (Gen1i, Gen1u, Gen2i, Gen2u, Gen3i, Gen3u)

7.6.33.1 Transmitter emphasis overview

The transmitter emphasis values specified in Table 54 and Table 55 refer to the output signal from the unit under test (UUT) at the mated connector of the device. The host transmit emphasis is specified while attached to the system cable(s), connectors, motherboard, and/or backplane that are used when integrated with the device. For the alternate compliance method specified in Section 7.4.3.3.14.2, the measurement is made with the CIC rather than with the actual system cable.

7.6.33.2 Transmitter emphasis measurement (Gen1i, Gen1u, Gen2i, Gen2u, Gen3i, Gen3u)

7.6.33.2.1 Transmitter emphasis measurement overview

Transmitter emphasis is measured by comparing the HFTP versus the fourth bit of LFTP. Emphasis specifications in Table 54 and Table 55 shall be met according to the measurement method as defined in 7.6.33.3.

Figures TBDa and TBDb show the test setups for measuring emphasis. The HBWS is the standard for measuring emphasis. The losses in the test connections may be significant so it is prudent to minimize and estimate these.

Several methods may be used to estimate the cabling losses:

- use two cables of different lengths and compare the losses of each;
- rely on published data for the cables; or
- obtain a separate means for measuring the cable loss (e.g., characterization with a network analyzer or power meter).

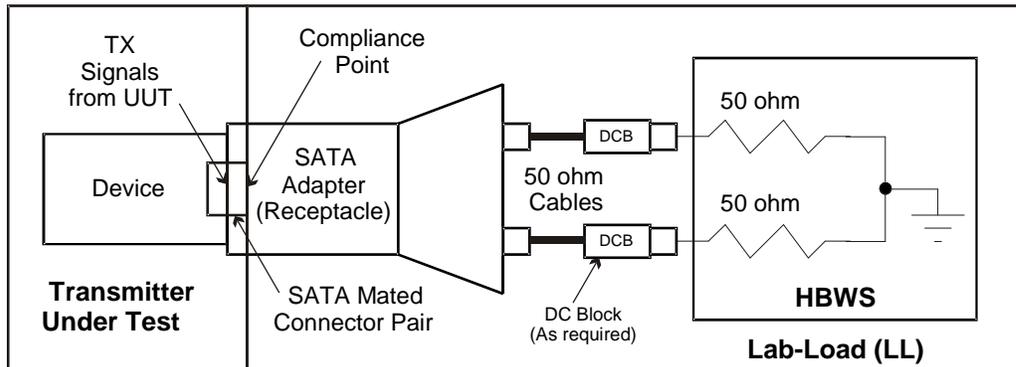


Figure TBDa – Device transmit emphasis test with Lab-Load (LL)

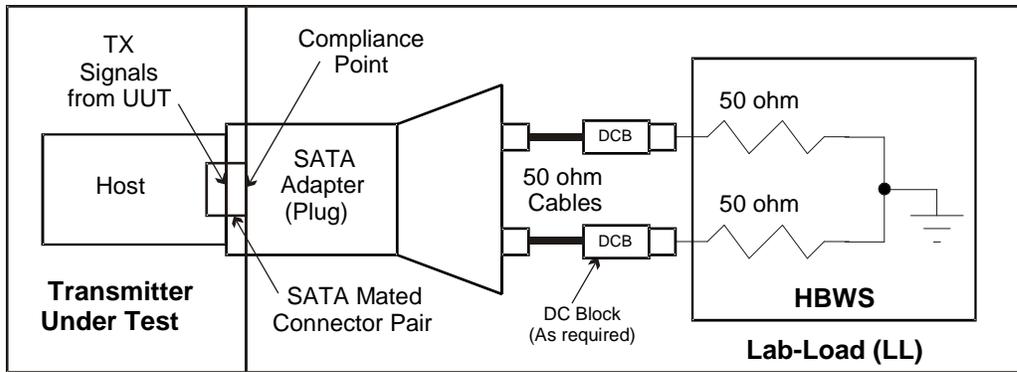


Figure TBDb – Host transmit emphasis test with Lab-Load (LL)

This specification describes emphasis levels in terms of voltage amplitude ratio in dB while driving a test load of 100 ohm differential (i.e., lab-load) and 50 ohm single ended to ground.

7.6.33.3 Measurement of emphasis

To test for emphasis, use the following steps:

Step 1, transmitting a HFTP pattern, for a unit interval (UI) corresponding to a 1 bit, construct a histogram based on n samples collected in the waveform epoch [0.45 UI to 0.55 UI] for the UI. The number of samples in a histogram (n) for the UI shall be greater than or equal to 100 and shall meet the requirement that:

$$1.537 \left(\frac{s}{\bar{x}} \right)^2 \leq n$$

where:

\bar{x} = the mean of the voltage samples in the histogram that may be read from the HBWS in histogram measurement mode

s = the standard deviation of the voltage samples in the histogram that may also be read from the HBWS

n = the number of samples that contribute to the histogram – this may also be read from the HBWS

The inequality above is based on a requirement that enough samples are collected to define a confidence interval with at least 95 % probability and with a width no greater than 10 % of the sample mean.

Call the mean,

$$A = \bar{x}$$

Step 2, transmitting a HFTP pattern, for a unit interval (UI) corresponding to a 0 bit, construct a histogram based on n samples collected in the waveform epoch [0.45 UI to 0.55 UI] for the UI. The number of samples in a histogram (n) for the UI shall be greater than or equal to 100 and shall meet the requirement that:

$$1.537 \left(\frac{s}{\bar{x}} \right)^2 \leq n$$

where:

\bar{x} = the mean of the voltage samples in the histogram that may be read from the HBWS in histogram measurement mode

s = the standard deviation of the voltage samples in the histogram that may also be read from the HBWS

n = the number of samples that contribute to the histogram – this may also be read from the HBWS

Call the mean,

$$B = \bar{x}$$

Step 3, transmitting a LFTP pattern, construct a histogram based on n samples collected in the waveform epoch [0.45 UI to 0.55 UI] for the UI of the last 1 bit in a string of four 1 bits. The number of samples in a histogram (n) for the UI shall be greater than or equal to 100 and shall meet the requirement that:

$$1\ 537 (s / \bar{x})^2 \leq n$$

where:

\bar{x} = the mean of the voltage samples in the histogram that may be read from the HBWS in histogram measurement mode

s = the standard deviation of the voltage samples in the histogram that may also be read from the HBWS

n = the number of samples that contribute to the histogram – this may also be read from the HBWS

Call the mean,

$$C = \bar{x}$$

Step 4, transmitting a LFTP pattern, construct a histogram based on n samples collected in the waveform epoch [0.45 UI to 0.55 UI] for the UI of the last 0 bit in a string of four 0 bits. The number of samples in a histogram (n) for the UI shall be greater than or equal to 100 and shall meet the requirement that:

$$1\ 537 (s / \bar{x})^2 \leq n$$

where:

\bar{x} = the mean of the voltage samples in the histogram that may be read from the HBWS in histogram measurement mode

s = the standard deviation of the voltage samples in the histogram that may also be read from the HBWS

n = the number of samples that contribute to the histogram – this may also be read from the HBWS

Call the mean,

$$D = \bar{x}$$

Step 5, from A, B, C, and D obtained in steps 1 through 4, compute:

$$V_{\text{Emphasis}} = 20\log[(A - B)/(C - D)]$$

The test for minimum device emphasis is passed if:

$$V_{\text{Emphasis}} \geq V_{\text{EmphasisDevice}}(\text{Min})$$

The test for maximum device emphasis is passed if:

$$V_{\text{Emphasis}} \leq V_{\text{EmphasisDevice}}(\text{Max})$$

The test for minimum host emphasis is passed if:

$$V_{\text{Emphasis}} \geq V_{\text{EmphasisHost}}(\text{Min})$$

The test for maximum host emphasis is passed if:

$$V_{\text{Emphasis}} \leq V_{\text{EmphasisHost}}(\text{Max})$$

See Table 54 and Table 55, according to 7.4.2 for $V_{\text{EmphasisDevice}}$ and $V_{\text{EmphasisHost}}$, otherwise the test for emphasis has not been passed.