

**Proposed
Draft**

**Serial ATA
International Organization**

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TPR074v1SATA32

Title: Obsolete Parallel ATA Emulation

Proposed change, new functionality, or behavior to Serial ATA Revision 3.2

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Document History

Version	Date	Comments
00	14-Aug-2015	Initial draft
01	17-Aug-2015	Incorporate changes requested by 17 August SATA Digital working group call. This is the recommended revision of this proposal

1 Introduction

The SATA series of specifications has been in existence for over 15 years. During that time, some of the functionality has become obsolete and is no longer in need of being part of the specification.

Text removals are shown in ~~red-strikeout~~. Text additions are shown in blue underlined.

2 Summary of the problem

The purpose of this proposal is to obsolete Parallel Emulation. This material may be found in previous SATA specifications if the historical information is important.

3 Summary of the solution

Delete subclause 13.1 from SATA 3.2

4 Proposed changes

Delete subclause 13.1 from SATA 3.2.

As a result of deleting subclause 13.1, the following additional changes are also required.

8.4.3 Device phy initialization state machine

...

DP2: DR_COMINIT	Transmit COMINIT ^{a,b}		
1. Unconditional	→	DR_AwaitCOMWAKE	
^a COMINIT transmitted for a 6 bursts duration ^b According to 13.1, devices <u>Devices</u> shall respond with a COMINIT signal at the completion of the device power up sequence or within 10 ms of the de-qualification of a received			

...

Appendix C. Device emulation of nIEN with interrupt pending (informative)

This specification defines the Interrupt bit in Register Device to Host FISes as the interrupt pending state of the device, and it is not modified by the state of nIEN bit in received Register Host to Device FISes. In this specification, devices ignore the nIEN bit in received Register Host to Device FISes and always perform as if nIEN bit is cleared to zero (see 10.5.5 and 10.5.6).

Some devices implemented to prior Serial ATA specification revisions used the nIEN bit of the Register Host to Device FIS as a pre-condition to setting the Interrupt bit to one of the Register Device to Host FIS and Set Device Bits FIS. The purpose of using nIEN bit to enable the Interrupt bit was to emulate the operation of the parallel implementation of ATA. In the parallel implementation, if the nIEN bit is cleared to zero, the device is enabled for the INTRQ line to the host. If the nIEN bit is set to one, the INTRQ line is put into the high impedance state by the device. ~~This function is typically used in devices that support Device 0 and Device 1 operation (see 13.1.4), and it is also required for Overlapped operation.~~

~~In this specification, the implementation of Device 0 / Device 1 emulation is performed exclusively by the host (see 13.1.4).~~

One serious side effect of device emulation of nIEN is the possibility of lost interrupts. In the parallel implementation,