Proposed	**Serial ATA**
Draft	**International Organization**

Serial ATA Revision 3.3 Technical Proposal TPR077

Title: DEADLINE HANDLING Correction

Proposed change, new functionality, or behavior to Serial ATA Revision 3.3

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This Draft Specification is NOT the final version of the Specification and is subject to change without notice. A modified, final version of this Specification ("Final Specification") when approved by the Promoters will be made available for download at this Web Site: http://www.serialata.org.

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Document History

Version	Date	Comments
00	02/22/2016	Initial draft
01	02/29/2016	Removed additional text, as shown by the change markings.
02	03/14/2016	Added: ignore RDNC and WDNC if PRIO is not equal to 01b on READ FPDMA QUEUED and WRITE FPDMA QUEUED commands.
03	03/14/2016	Accepted changes, updated the page headers and title.
04	03/28/2016	Approved by Digital workgroup.
05	03/28/2016	Member review , D209 changed to TPR077.

1   Introduction

This is a mandatory change to the requirements in SATA Revision 3.3.

No new IDENTIFY DEVICE bit is intended to be defined for this change.

2   Summary of the problem

DEADLINE HANDLING was first introduced in SATA Revision 3.0 and was unchanged in 3.1.

It is likely that there is more than one implementation of the 3.0 definition, and it is possible that nobody is compliant with the change introduced at the last minute in revision 3.2.

In **SerialATA_Revision_3_2_Rev21_(RC)**, section 13.6.6.4.1, the WDNC parameter is described as:

> If the WDNC (Write Data Not Contiunue) bit is cleared to zero, then the device may allow WRITE FPDMA QUEUED command completion times to exceed what the ICC parameter specified. If the WDNC bit is set to one, then the all WRITE FPDMA QUEUED commands shall be completed by the time specified by the ICC timer value, othewise the device shall return **command aborted for all outstanding commands**. WDNC is only applicable to WRITE FPDMA QUEUED commands with PRIO is set to 01b (Isochronous – deadline dependent priority). (See 13.6.5).

But in **SATA Revision 3.2 Gold and in SATA Revision 3.3 Gold** (same section), it says:

> If the WDNC (Write Data Not Contiunue) bit is cleared to zero, then the device may allow WRITE FPDMA QUEUED command completion times to exceed what the ICC parameter specified. If the WDNC bit is set to one, then the all WRITE FPDMA QUEUED commands shall be completed by the time specified by the ICC timer value, otherwise the device shall return **command aborted for all outstanding WRITE FPDMA QUEUED commands with PRIO set to 01b** (see 13.6.5).

This change (for RDNC and WDNC) was introduced as a result of a last-minute review comment, which was not reviewed or approved by the Digital WG.

3   Proposed changes

[Editor's note: Existing text is black. New text is marked as underlined in blue color. Material to be deleted is red with strikethrough markings.]

[Editor's note: Update the DEADLINE HANDLING command as follows]

RDNC   If the Read Data Not Continue (RDNC) bit is cleared to zero, then the device may allow READ FPDMA QUEUED command completion times to exceed what the ICC field specified. If the RDNC bit is set to one, then the all READ FPDMA QUEUED commands shall be completed by the time specified by the ICC field timer value, otherwise the device shall return command aborted for all outstanding READ FPDMA QUEUED commands with PRIO set to 01b (see 13.6.4).

The state of the WDNC bit and RDNC bit shall be preserved across software resets and COMRESETs (via Software Setting Preservations), and shall not be preserved across power cycles.

RDNC   If the Read Data Not Continue (RDNC) bit is cleared to zero, then the device may allow a READ FPDMA QUEUED command completion time to exceed the value specified by the ICC field in that READ FPDMA QUEUED command. If the RDNC bit is set to one, then all READ FPDMA QUEUED commands with the PRIO field set to 01b (see [prio field definition]xxx) shall either:

a) be completed by the time specified by the ICC field timer value in that READ FPDMA QUEUED command; or

b) the device shall return command aborted for all outstanding commands.

The state of the RDNC bit shall be preserved across software resets and COMRESETs (via Software Setting Preservations), and shall not be preserved across power cycles.

The device shall ignore the state of the RDNC bit for READ FPDMA QUEUED commands where the PRIO field is not set to 01b.

WDNC ~~If the Write Data Not Continue (WDNC) bit is cleared to zero, then the device may allow WRITE FPDMA QUEUED command completion times to exceed what the ICC field specified. If the WDNC bit is set to one, then the all WRITE FPDMA QUEUED commands shall be completed by the time specified by the ICC field timer value, otherwise the device shall return command aborted for all outstanding WRITE FPDMA QUEUED commands with the PRIO field set to 01b (see 13.6.5).~~

WDNC   If the Write Data Not Continue (WDNC) bit is cleared to zero, then the device may allow a WRITE FPDMA QUEUED command completion times to exceed the value specified by the ICC field in that WRITE FPDMA QUEUED command. If the WDNC bit is set to one, then all WRITE FPDMA QUEUED commands with the PRIO field set to 01b shall either:

- a) be completed by the time specified by the ICC field timer value in that WRITE FPDMA QUEUED command; or

- b) the device shall return command aborted for all outstanding commands.

The state of the WDNC bit shall be preserved across software resets and COMRESETs (via Software Setting Preservations), and shall not be preserved across power cycles.

The device shall ignore the state of the WDNC bit for WRITE FPDMA QUEUED commands where the PRIO field is not set to 01b.

[Editor's note: No additional changes to the DEADLINE HANDLING command]