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Proposed Draft Serial ATA International Organization

Version 0.17

February 23, 2009

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Title : Extensions to the FPDMA QUEUED Command Protocol to Support Fixed 512 Byte Block Transfer DMA Commands

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Document History

Version	Date	Comments
0.01	03/28/2008	Initial draft.
0.02	04/28/2008	Removing dependency on NCQ Management command
0.03	12/08/2008	Removing all attributes except for Trim to reflect the T13 proposal.
0.04	12/15/2008	Added state transitions for data transfer (similar to FPDMA QUEUED WRITE) for NCQ DATA SET MANAGEMENT
0.10	01/13/2009	Removed all state machine changes and reformulated the proposal to be a general extension to the FPDMA QUEUED protocol so that all fixed size, 512 byte block DMA transfer commands may be supported. Removed all background information about Data Set Management as the proposed Data Set Management command will come from T13. The mapping of registers to fields is now all that is needed.
0.11	01/24/2009	Incorporated feedback: Corrected IDENTIFY and DCO definitions Removed DSM specifics defined in T13 Created Auxiliary and Auxiliary (exp) registers to hold the displaced Features data. This restored PRIO to the new command. Added READ FPDMA QUEUED and WRITE FPDMA QUEUED command to include Auxiliary, Auxiliary and Sub Command register values. Added method for discovering DSM Subcommand support
0.12	01/26/2009	Fixed wording errors for 512 Byte Block FPDMA Sector Count and basis statements. Reworded the LBA Range overlap requirements in the DATA SET MANAGEMENT command for clarity.
0.13	01/28/2009	Changed the name of the new commands from READ 512 BYTE BLOCK FPDMA QUEUED to RECEIVE FPDMA QUEUED and WRITE 512 BYTE BLOCK FPDMA QUEUED to SEND FPDMA QUEUD. Also changed the values of the new fields added to READ FPDMA QUEUED and WRITE FPDMA QUEUED back to 'Reserved'.
0.14	02/06/2009	Removed definition of required device behavior in case of an FPDMA IO and NCQ DSM range overlap. The drive now has full discretion. Added READ LOG EXT page definition (section 9.1.2 and 9.3.3.3) for defining SEND FPDMA QUEUED and RECEIVE FPDMA QUEUED supported Subcommands. Changed FIS declaration style
0.15	02/12/2009	Removed the Subcommand field from the H2D FIS and moved the Subcommand value to a Subcommand field in the SEND FPDMA QUEUED and RECEIVED FPDMA QUEUED Sector Count (ext) field.
0.16	02/13/2009	Fixed inconsistency and editorial errors. These are items that would have been caught during 30 day review. No functional change.
0.17	02/23/2009	Fixed inconsistency and editorial errors. These are items that would have been caught during 30 day review. No functional change.

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1 Introduction

This proposal discusses the details necessary for defining and implementing the extension to the FPDMA QUEUED protocol for processing commands with fixed 512 byte block transfer sizes

It creates two new commands that identify the new fixed 512 byte block operations: RECEIVE FPDMA QUEUED and SEND FPDMA QUEUED. These two operations are accompanied by new field definitions in the Host to Device Register FIS in order to accommodate the ATA commands that will be using these two new transport methods.

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At the end, an initial new ATA command, DATA SET MANAGEMENT is introduced and mapped into the SEND FPDMA QUEUED operation as an example of how new commands can be carried by the FPDMA QUEUED protocol.

2 Opportunities for Extending the NCQ Command Set

The FPDMA QUEUED protocol has included support for only 2 data transport operations since its inception, IO operations READ FPDMA QUEUED and WRITE FPDMA QUEUED. This very small subset of possible ATA data operations has been hindered by the requirement that FPDMA QUEUED operations and Non FPDMA QUEUED operations cannot be intermixed. Switching between the two sets of commands is inefficient.

There are efficiency and performance improvement opportunities for new NCQ specific operations that could possibly be handled in the same method as READ FPDMA QUEUED and WRITE FPDMA QUEUED. This is particularly true for control commands and management commands which are often intermixed with IO operations.

Additionally the mechanics of the FPDMA QUEUED protocol offer the benefit of being able to separate command data transfer from command completion allowing non IO operations which take a significant time to accomplish to be handled in parallel with other operations such as IO.

3 Extending the NCQ Command Set to Support 512 Byte Block Transfer DMA Commands

Extensions to the FPDMA QUEUED protocol can be done without modifying the FPDMA QUEUED state machine. It is necessary to extend some of the states definitions which cause some complications to the specification in terms of style and consistency.

In this draft of the proposal areas of consistency and style conflict have been flagged with comments and questions for the committee. Through committee discussion and online email reflector conversations I expect that these areas will be resolved.

It is my belief that although some of these sections may change cosmetically to create a consistent style, the changes will not be functional and that the material included in this document is functionally correct as it is.

4 Extending the NCQ Command Set Proposal

The primary focus of this proposal is to create methods for transferring commands beyond the IO operations of READ and WRITE. This is a separate objective from defining the commands and payloads that would use these new extensions to the NCQ Command Set. Although one command is included in this proposal to provide precedence, the bulk of the new commands that will use this extension will be introduced in a separate proposal in order to keep this effort focused on the logistics of the transport alone.

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The only requirements for the solution provided here is that it:

- Be able to use the FPDMA QUEUED protocol without breaking legacy implementations
- Be able to adequately transport fixed 512 byte block ATA DMA commands
- Extend NCQ to handle new commands in a general manner that can be extended easily in the future
- New subcommands handled by NCQ extensions need to be feature negotiated as a white list (specifically identified as NCQ capable)

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- New subcommands handled by NCQ extension are not dependant on having nonNCQ equivalents

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- Use the smallest possible amount of Reserved space in the H2D Register FIS as possible

5 Proposed Changes to NCQ in SATA

The following sections 6 through 10.3.5.1.1 are modifications to existing SATA 3.0 sections and show their changes in red. Sections 10.3.5.2, 10.3.5.3 and 10.3.6 are completely new sections to be added to the SATA 3.1 specification.

All sections are ordered and given the same headings and subheadings as the sections they modify or follow. In the case that the SATA 2.6 specification and the SATA 3.0 specification don't match both sections were given. Figure and Title numbers were taken from SATA 3.0. New Figure and Titles are left unnumbered if only immediately referenced within the proposal.

6 Normative References [Section 3]

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6.1 References under development [Section 3.1]

ATA/ATAPI Command Set - 2 (ACS-2) [ANSI INCITS T13/2015-D]

7 Transport Layer [Section 10]

7.1 FIS Types [Section 10.3]

7.1.1 Register – Host to Device [Section 10.3.4]

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0	Features (7:0)								Command								C	R	R	R	PM Port				FIS Type (27h)							
1	Device								LBA (23:16)								LBA (15:8)								LBA(7:0)							
2	Features (15:8)								LBA (47:40)								LBA (39:32)								LBA (31:24)							
3	Control								ICC								Count (15:8)								Count (7:0)							
									7	6	5	4	3	2	1	0																	
4	Reserved (0)								Reserved (0)								Auxiliary (15:8)								Auxiliary (7:0)							

Figure 193 – Register – Host to Device FIS layout

If a field in this FIS is not defined by a command, it shall be Reserved for that command.

Auxiliary (7:0) – Contains parameter values specified on a per command basis.

Auxiliary (15:8) – Contains parameter values specified on a per command basis.

7.1.2 Set Device Bits – Device to Host [Section 10.3.6]

0	Error								R	Status Hi				R	Status Lo			N	I	R	R	PM Port				FIS Type (A1h)							
1	Protocol Specific																														

Figure 195 – Set Device Bits – Device to Host FIS layout

Field Definitions

I – Interrupt Bit. This bit signals the host adapter to enter an interrupt pending state. If the host is executing tagged queued commands (READ DMA QUEUED WRITE DMA QUEUED) with the device, the host should only enter the interrupt pending state if both the BSY bit and the DRQ bit in the shadow Status register are zero when the frame is received. If the host is executing native queued commands (READ FPDMA QUEUED, WRITE FPDMA QUEUED, NCQ MANAGEMENT, RECEIVE FPDMA QUEUED, or SEND FPDMA QUEUED) with the device, the interrupt pending state is entered regardless of the current state of the BSY bit or the DRQ bit in the shadow Status register. Devices shall not modify the behavior of this bit based on the state of the nIEN bit received in Register Host to Device FISes.

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8 Device Command Layer Protocol [Section 11]

8.1 Device Idle protocol [Section 11.2]

DI0 : Device_idle	Wait.	
1. FIS receipt	→	DI1: Check_FIS
2. * Ready to complete released command.	→	DI4: Set_service
3. * Ready to receive data for WRITE FPDMA QUEUED or SEND FPDMA QUEUED command and FIS receipt not indicated and no error encountered	→	DFPDMAQ4: DataPhase_ PreWriteSetup
4. * Ready to transmit data for READ FPDMA QUEUED or RECEIVE FPDMA QUEUED command and FIS receipt not indicated and no error encountered	→	DFPDMAQ3: DataPhase_ ReadSetup
5. * One or more FPDMA QUEUED commands completed successfully and FIS receipt not indicated and no error encountered	→	DFPDMAQ10: SendStatus[1]
6. * FPDMA QUEUED command terminated with failure and FIS receipt not indicated	→	DFPDMAQ11: ERROR
7. Asynchronous Notification is enabled and event has occurred that requires notification and NotifyPending = 0 and FIS receipt not indicated.	→	AN0: Notify_host
NOTE: 1. This condition may be true simultaneously with condition 3 or 4. Devices implementing status aggregation may select any of the transitions 3, 4, or 5 if their conditions evaluate to true. Devices not implementing status aggregation shall prioritize transition 5 over transitions 3 and 4.		

DI2 : Check_command[1]	Check the command to determine required command protocol. If asynchronous notification is supported then NotifyPending is cleared to zero.	
1. Non-data command protocol and no native queued command outstanding.	→	DND0: Non-data
2. PIO data-in command protocol and no native queued command outstanding.	→	DPIOI0: PIO_in
3. PIO data-out command protocol and no native queued command outstanding.	→	DPIOO0: PIO_out
4. READ DMA command protocol and no native queued command outstanding.	→	DDMAI0: DMA_in
5. WRITE DMA command protocol and no native queued command outstanding.	→	DDMAO0: DMA_out
6. PACKET command protocol and no native queued command outstanding.	→	DP0: PACKET
7. * READ DMA QUEUED command protocol and no native queued command outstanding.	→	DDMAQI0: DMA_queued_in
8. * WRITE DMA QUEUED command protocol and no native queued command outstanding.	→	DDMAQIO: DMA_queued_out

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9. EXECUTE DEVICE DIAGNOSTIC command protocol and no native queued command outstanding.	→	DEDD0: Execute_device_diag
10. DEVICE RESET command protocol.	→	DDR0: Device_reset
11. Command not implemented and no native queued command outstanding.	→	DI3: No_command
12. * SERVICE command protocol and no native queued command outstanding.	→	DI5: Service_test
13. * ~~READ~~ FPDMA QUEUED command protocol.	→	DFPDMAQ1: AddCommand_ ToQueue
~~14. * WRITE FPDMA QUEUED command protocol.~~	→	~~DFPDMAQ1: AddCommand_ ToQueue~~
~~15. * NCQ QUEUE MANAGEMENT command protocol.~~	→	~~DFPDMAQ1: AddCommand_ ToQueue~~
14. Not READ FPDMA QUEUED and not WRITE FPDMA QUEUED and not a NCQ MANAGEMENT and not a RECEIVE FPDMA QUEUED and not a SEND FPDMA QUEUED and not DEVICE RESET and native queued command(s) outstanding	→	DFPDMAQ12: BrokenHost_ ClearBusy
NOTE: 1. This state shows transitions for all commands. If a device does not implement any particular command, then that transition should not be processed.		

DI0: Device_Idle: This state is entered when the device has completed the execution of a command protocol, a COMRESET protocol, a software reset protocol, or a queued command has been released.

When in this state, the device is awaiting a command. If queuing is supported, the device may be waiting to acquire data or establish buffer space to complete a queued command.

*** Transition DI0:3:** When the device is ready to receive the data for a WRITE FPDMA QUEUED or SEND FPDMA QUEUED command, the device shall transition to the DFPDMAQ4: DataPhasePreWriteSetup state. This condition also applies for the case where non-zero buffer offsets are used to complete a previous partial data transfer.
*** Transition DI0:4:** When the device is ready to transmit the data for a READ FPDMA QUEUED or RECEIVE FPDMA QUEUED command, the device shall transition to the DFPDMAQ3: DataPhaseReadSetup state. This condition also applies for the case where non-zero buffer offsets are used to complete a previous partial data transfer.

DI2: Check_command state: This state is entered when the device recognizes that the received Register FIS contains a new command. NOTE: This state shows transitions for all commands. If a device does not implement any particular command, then transition DI2:11 to state DI3:No_command shall be made.

*** Transition DI2:13:** When the received command is a ~~READ~~ FPDMA QUEUED command protocol, the device shall transition to the DFPDMAQ1: AddCommandToQueue state.

~~*** Transition DI2:14:** When the received command is a WRITE FPDMA QUEUED command~~

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~~protocol, the device shall transition to the DFPDMAQ1: AddCommandToQueue state.]~~

*** Transition DI2:~~14~~ ~~15~~:** When the received command is a not a READ FPDMA QUEUED; and not a WRITE FPDMA QUEUED; and not a NCQ MANAGEMENT; and not a RECEIVE FPDMA QUEUED; and not a SEND FPDMA QUEUED; and not a DEVICE RESET; and there are native queued command(s) outstanding, an error has occurred and the device shall transition to the DFPDMAQ12: BrokenHost_ClearBusy state.

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8.2 FPDMA QUEUED command protocol [Section 11.14]

This class includes:

- READ FPDMA QUEUED
- WRITE FPDMA QUEUED
- NCQ MANAGEMENT
- RECEIVE FPDMA QUEUED
- SEND FPDMA QUEUED

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DFPDMAQ3: DataPhaseReadSetup: This state is entered when the device has determined that it is ready to transmit data for a previously queued READ FPDMA QUEUED or RECEIVE FPDMA QUEUED command.

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DFPDMAQ4: DataPhasePreWriteSetup: This state is entered when the device has determined that it is ready to receive data for a previously queued WRITE FPDMA QUEUED or SEND FPDMA QUEUED command.

DFPDMAQ5: DataPhase_WriteSetup: This state is entered when the device is ready to Auto Activate and receive data for a previously queued WRITE FPDMA QUEUED or SEND FPDMA QUEUED command.

DFPDMAQ6: DataPhase_OldWriteSetup: This state is entered when the device is ready to receive data for a previously queued WRITE FPDMA QUEUED or SEND FPDMA QUEUED command, and the device does not support Auto-Activate, or it is not enabled.

DFPDMAQ7: DataPhaseXmit_Activate: This state is entered after the device has completed transmission of a DMA Setup FIS for a WRITE FPDMA QUEUED or SEND FPDMA QUEUED command or the device has finished receiving a Data FIS for a WRITE FPDMA QUEUED or SEND FPDMA QUEUED command, and the transfer count is not exhausted.

DFPDMAQ8: DataXmitRead: This state is entered after the device has completed transmission of a DMA Setup FIS for a READ FPDMA QUEUED or RECEIVE FPDMA QUEUED command.

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DFPDMAQ9: DataXmitWrite: This state is entered after the device has completed transmission of a DMA Setup FIS for a WRITE FPDMA QUEUED or SEND FPDMA QUEUED command.

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DFPDMAQ12: BrokenHost_ClearBusy: This state is entered when the device has received a READ FPDMA QUEUED or WRITE FPDMA QUEUED or NCQ MANAGEMENT or RECEIVE FPDMA QUEUED or SEND FPDMA QUEUED command with a TAG that already exists in its command queue, or when the received command is a not a READ FPDMA QUEUED; and not a WRITE FPDMA QUEUED; and not a NCQ MANAGEMENT; and not a RECEIVE

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FPDMA QUEUED; and not a SEND FPDMA QUEUED; and not a DEVICE RESET; and there are native queued command(s) outstanding.

9 Host Command Layer protocol [Section 12]

9.1 FPDMA QUEUED command protocol [Section 12.1]

This high-level state machine describes the behavior of the host for the Native Command Queuing command protocol. The host behavior described by the state machine may be provided by host software and/or host hardware and the intent of the state machines is not to indicate any particular implementation.

This class includes:

- READ FPDMA QUEUED
- WRITE FPDMA QUEUED
- NCQ MANAGEMENT
- RECEIVE FPDMA QUEUED
- SEND FPDMA QUEUED

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HFPI0: Idle: When in this state, if queuing is supported and enabled, the Command layer is awaiting a READ FPDMA QUEUED, WRITE FPDMA QUEUED, NCQ MANAGEMENT, RECEIVE FPDMA QUEUED, or SEND FPDMA QUEUED command from the higher level protocol, or awaiting an interrupt from the Device indicating completion of previously queued commands, or waiting for a TAG location to become available for a command waiting in the command queue.

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Transition HFPI0:1: If a READ FPDMA QUEUED, WRITE FPDMA QUEUED, NCQ MANAGEMENT, RECEIVE FPDMA QUEUED, or SEND FPDMA QUEUED command is pending that has not had a TAG value assigned to it and there is a free TAG location available for assignment then a transition shall be made to the HFPDMAQ2: PresetACTBit state.

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HFPDMAQ1: AddCommandToQueue: The Command layer enters this state when it has received a READ FPDMA QUEUED, WRITE FPDMA QUEUED, NCQ MANAGEMENT, RECEIVE FPDMA QUEUED, or SEND FPDMA QUEUED command from the higher level protocol, and adds it to the internal host command queue.

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10 Application Layer [Section 13]

10.1 IDENTIFY (PACKET) DEVICE and SET FEATURES [Section 13.2]

10.1.1 IDENTIFY DEVICE [Section 13.2.1]

77	O		Serial ATA capabilities	
		R	15-7	Reserved
		F	6	Supports RECEIVE FPDMA QUEUED and SEND FPDMA QUEUED commands
		F	5	Supports NCQ Queue Management Command
		F	4	Supports Native Command Queuing Streaming information
		V	3-1	Coded value indicating current negotiated Serial ATA signal speed
		F	0	Shall be cleared to zero

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10.1.1.1 Word 77: Serial ATA capabilities [Section 13.2.1.17]

Bit 6 when set to one indicates that the device supports use of the RECEIVE FPDMA QUEUED, and SEND FPDMA QUEUED command by the host. This bit shall only be set to one if the device supports NCQ as shown in bit 8 of Word 76.

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Bit 7-15 are reserved and shall be cleared to zero.

10.2 Device Configuration Overlay [Section 13.4]

Word	Description
0-7	As defined in the ATA reference
8	Serial ATA command / feature sets supported 15-8 Reserved (0) 7 1 = Reporting support for RECEIVE FPDMA QUEUED, and SEND FPDMA QUEUED is allowed 6 1 = Reporting support for NCQ Queue Management is allowed 5 1 = Reporting support for Automatic Partial to Slumber is allowed 4 1 = Reporting support for software settings preservation is allowed 3 1 = Reporting support for asynchronous notification is allowed 2 1 = Reporting support for interface power management is allowed 1. 1 = Reporting support for non-zero buffer offsets in DMA Setup FIS is allowed 0 1 = Reporting support for Native Command Queuing[1] is allowed
	Reserved for Serial ATA
10-255	As defined in the ATA/ATAPI-8 Standard

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Note:

1. Applicable to non-PACKET devices only – i.e. IDENTIFY DEVICE

Figure 203 - Device Configuration Overlay data structure

Bit 7 of Word 8 in Device Configuration Overlay data structure indicates the device may support RECEIVE FPDMA QUEUED, and SEND FPDMA QUEUED. When set to one, the device is allowed to report support for RECEIVE FPDMA QUEUED, and SEND FPDMA QUEUED, only if the device is already supporting NCQ indicated by bit 0 of Word 8 set to one. If bit 0 of Word 8 is set to zero this bit shall be set to zero. When cleared to zero, device support for RECEIVE FPDMA QUEUED, and SEND FPDMA QUEUED shall be disabled and IDENTIFY Device WORD 77 bit 6 shall be cleared to zero.

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If NCQ is disabled and READ FPDMA QUEUED, WRITE FPDMA QUEUED, NCQ MANAGEMENT, or RECEIVE FPDMA QUEUED, and SEND FPDMA QUEUED command is issued to the device, the device shall abort the command with the ERR bit set to one in the Status register and the ABRT bit set to one in the Error register. The setting of this bit is applicable to non-PACKET devices only.

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Bits 8-15 are reserved and shall be cleared to zero.

10.3 Native Command Queuing (Optional) [Section 13.6: SATA 2.6 Section 13.5]

10.3.1 Definition [Section 13.6.1]

10.3.1.1 Priority [Section 13.6.1.5]

Host knowledge of I/O priority may be transmitted to the device as part of the command. There are two priority values for NCQ commands, normal and high. When the host marks an NCQ command as high priority, the host is requesting a better quality of service for that command than commands issued with normal priority.

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The classes are forms of soft priority. The device may choose to complete a normal priority command before an outstanding high priority command, although preference should be given to the high priority commands. One example where a normal priority command may be completed before a high priority command is when the normal priority command is a cache hit, whereas the high priority command requires access of the device media.

The priority class is specified in the PRIO bit for NCQ commands (READ FPDMA QUEUED, ~~and~~ WRITE FPDMA QUEUED, NCQ MANAGEMENT, RECEIVE FPDMA QUEUED, or SEND FPDMA QUEUED). This bit may specify either the normal priority or high priority value. If a command is marked by the host as high priority, the device should attempt to provide better quality of service for the command. It is not required that devices process all high priority requests before satisfying normal priority requests.

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10.3.2 Intermixing Non-Native Queued Commands and Native Queued Commands [Section 13.6.2]

The host shall not issue a non-native queued command while a native queued command is outstanding. Upon receiving a non-native queued command while a native queued command is outstanding, the device shall signal the error condition to the host by transmitting a Register FIS

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to the host with the ERR and ABRT bits set to one and the BSY bit cleared to zero in the Status field of the FIS and halt command processing as described in section 13.5.1.4 except as noted below. Non-native queued commands include all commands other than the READ FPDMA QUEUED, WRITE FPDMA QUEUED, ~~and~~ NCQ MANAGEMENT, RECEIVE FPDMA QUEUED, and SEND FPDMA QUEUED commands defined in sections 13.6.3.1, 13.6.3.6, 13.6.3.10, 13.6.3.13 and section 13.6.3.14.

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10.3.3 Command Definitions [Section 13.6.3]

There are 5 NCQ commands: READ FPDMA QUEUED, WRITE FPDMA QUEUED, NCQ MANAGEMENT, RECEIVE FPDMA QUEUED, and SEND FPDMA QUEUED.

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NCQ MANAGEMENT is the only NCQ command that is performed with no data transfer. READ FPDMA QUEUED and WRITE FPDMA QUEUED commands have transfer sizes of logical sector size multiples. RECEIVE FPDMA QUEUED and SEND FPDMA QUEUED commands have transfer sizes of 512 byte multiples. READ FPDMA QUEUED and RECEIVE FPDMA QUEUED commands transfer data from the device to the host. WRITE FPDMA QUEUED and SEND FPDMA QUEUED commands transfer data from the host to the device. NCQ MANAGEMENT, RECEIVE FPDMA QUEUED and SEND FPDMA QUEUED contain subcommands that determine the operation of the commands referenced in subcommand sections of this specification.

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10.3.3.1 READ FPDMA QUEUED [Section 13.6.3.1]

10.3.3.1.1 Inputs [Section 13.6.3.1.1]

Register	7	6	5	4	3	2	1	0
Features (7:0)	Sector Count 7:0							
Features (15:8)	Sector Count 15:8							
Count (7:0)	TAG					Reserved		
Count (15:8)	PRIO 1:0		Reserved					
LBA Low (7:0)	LBA 7:0							
LBA Low (31:24)	LBA 31:24							
LBA Mid (15:8)	LBA 15:8							
LBA Mid (39:32)	LBA 39:32							
LBA High (23:16)	LBA 23:16							
LBA High (47:40)	LBA 47:40							
ICC	ICC 7:0							
Auxiliary(7:0)	Reserved							
Auxiliary (15:8)	Reserved							
Device	FUA	1	Res	0	Reserved			
Command	**60h**							

Figure 206 – READ FPDMA QUEUED command definition

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10.3.3.2 WRITE FPDMA QUEUED [Section 13.6.3.2]

10.3.3.2.1 Inputs [Section 13.6.3.2.1]

Register	7	6	5	4	3	2	1	0
Features (7:0)	Sector Count 7:0							
Features (15:8)	Sector Count 15:8							
Count (7:0)	TAG					Reserved		
Count (15:8)	PRIO 1:0		Reserved					
LBA Low (7:0)	LBA 7:0							
LBA Low (31:24)	LBA 31:24							
LBA Mid (15:8)	LBA 15:8							
LBA Mid (39:32)	LBA 39:32							
LBA High (23:16)	LBA 23:16							
LBA High (47:40)	LBA 47:40							
ICC	ICC 7:0							
Auxiliary(7:0)	Reserved							
Auxiliary (15:8)	Reserved							
Device	FUA	1	Res	0	Reserved			
Command	**61h**							

Figure 210 – WRITE FPDMA QUEUED command definition

Deleted: Command

10.3.3.3 SATA Logs [Section 13.7: No SATA 2.6 equivalent]

10.3.4 Log Address Definitions [Section 13.7.1]

The log addresses assigned for Serial ATA are defined in Table 80.

Log Address	Description
00h - 0Fh	As defined in the ATA8 ACS standard
10h	NCQ Queued Error log
11h	Phy Event Counters log
12h	NCQ Queue Management log
13h	NCQ Send and Receive log
14h - 17h	Reserved for future Serial ATA definition
18h - FFh	As defined in the ATA8 ACS standard

Table 80 - Log Addresses for Serial ATA

10.3.5 General Purpose Log Directory (00h) [Section 13.7.2]

Devices supporting the Queued Error Log (see 13.7) reflect this support in the General Purpose Log Directory log (00h) by having the value 1 at offset 20h and the value 0 at offset 21h of that log to indicate existence of a log at address 10h of 1 page in length.

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Devices supporting the Phy Event Counters Log reflect this support in the General Purpose Log Directory (00h) by having the value 1 at offset 22h and the value 0 at offset 23h of that log to indicate existence of a log at address 11h of 1 page in length.

Devices supporting the NCQ Queue Management Log reflect this support in the General Purpose Log Directory (00h) by having the value 1 at offset 24h and the value 0 at offset 25h of that log to indicate existence of a log at address 12h of 1 page in length.

Devices supporting NCQ Send and Receive Log reflect this support in the General Purpose Log Directory (00h) by having the value 1 at offset 26h and the value 0 at offset 27h of that log to indicate existence of a log at address 13h of 1 page in length.

Byte	Value
0 - 1Fh	As defined in the ACS-2 standard
20h	1 if Native Command Queuing is supported 0 if Native Command Queuing is not supported
21h	0
22h	1 if Phy Event Counters are supported 0 if Phy Event Counters are not supported
23h	0
24h	1 if NCQ Queue Management is supported 0 if NCQ Queue Management is not supported
25h	0
26h	1 if NCQ Send and Receive log is supported 0 if NCQ Send and Receive log is not supported
27h	0

Table 81 - General Purpose Log directory values for Serial ATA

10.3.5.1.1 NCQ Send and Receive Log (13h) [Section 13.7.6]

To determine the supported SEND FPDMA QUEUED and RECEIVE FPDMA QUEUED subcommands and their respective features, host software shall read log 13h.

Deleted: issue READ LOG EXT with a Log Address of

This page shall be supported if the SEND FPDMA QUEUED and RECEIVE FPDMA QUEUED command is supported (IDENTIFY DEVICE word 77 bit 6 is set to one.)

Table _____ - Log Page 13h - NCQ SEND and RECEIVE Log

Dword	Bits	Description
0	31-1	Reserved
0	0	1 = Supports the SEND FPDMA QUEUED Data Set Management subcommand 0 = Does not support the SEND FPDMA QUEUED Data Set Management subcommand

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1	31-1	Reserved for future SEND FPDMA QUEUED Data Set Management subcommand supported attributes
1	0	1 = The SEND FPDMA QUEUED Data Set Management subcommand supports the Trim Attribute 0 = The SEND FPDMA QUEUED Data Set Management subcommand does not support the Trim Attribute
128-2	31-0	**Reserved**

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Deleted: SubCommand

10.3.5.2 RECEIVE FPDMA QUEUED

Deleted: RECIEVE

512 Byte Block DMA IN subcommands make use of this transport command. The RECEIVE FPDMA QUEUED command supports LBA mode only and uses 48-bit addressing only. The format of the command is defined in Figure _____.

Deleted: sub command
Deleted: RECIEVE

10.3.5.2.1 Inputs

Register	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Features (7:0)	Sector Count 7:0							
Features (15:8)	Sector Count 15:8							
Count (7:0)	TAG					Reserved		
Count (15:8)	PRIO 1:0		Res	Subcommand				
LBA Low (7:0)	LBA 7:0							
LBA Low (31:24)	LBA 31:24							
LBA Mid (15:8)	LBA 15:8							
LBA Mid (39:32)	LBA 39:32							
LBA High (23:16)	LBA 23:16							
LBA High (47:40)	LBA 47:40							
ICC	ICC 7:0							
Auxiliary(7:0)	Auxiliary (7:0)							
Auxiliary (15:8)	Auxiliary (15:8)							
Device	Res	1	Res	0	Reserved			
Command	**65h**							

Deleted: SubCommand

Figure _____ – RECEIVE FPDMA QUEUED command definition

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Deleted: Command

Count — The number of 512 byte blocks to be transferred, 0000h indicates that 65,536 512 byte blocks are to be transferred.

TAG — The TAG value shall be assigned by host software to be different from all other TAG values corresponding to outstanding commands. The assigned TAG value

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shall not exceed the value specified in IDENTIFY DEVICE word 75.

PRIO The Priority (PRIO) value shall be assigned by the host based on the priority of the command issued. The device shall make a best effort to complete High priority requests in a more timely fashion than Normal and Isochronous priority requests. The device shall make a best effort to complete Isochronous priority requests prior to its associated deadline. The Priority values are defined as follows:

00b	Normal Priority
01b	Isochronous – deadline dependent priority
10b	High priority
11b	Reserved

Subcommand

Deleted: SubCommand

The value of this field is Reserved.

LBA The value of this field is Reserved.

Deleted: The value of this field is defined on a per command basis as defined in section 9.3.6 of this specification.

ICC The Isochronous Command Completion (ICC) field shall be assigned by the host based on the intended deadline associated with the command issued. By default, when deadline is expired, the device shall continue to complete the command as soon as possible.

Auxiliary The value of this field is Reserved.

Deleted: The value of this field is defined on a per command basis as defined in section 9.3.6 of this specification.

Upon accepting the command, the device shall clear the BSY bit if/when it is prepared to receive another command by transmitting a Register FIS to the host with the BSY bit cleared to zero in the Status field of the FIS. The ability for the device to quickly clear the BSY bit allows the host to issue another queued command without blocking on this bit. The host shall check the BSY bit in the shadow Status register before attempting to issue a new command in order to determine that the device is ready to receive another command (and determine that the host has write access to the Shadow Register Block Registers). The device shall not trigger an interrupt in response to having successfully received the command, so the initial status return that clears BSY shall not have an interrupt associated with it.

10.3.5.2.2 Success Outputs

Upon successful completion of one or more outstanding commands, the device shall transmit a Set Device Bits FIS with the Interrupt bit set to one and one or more bits set to one in the ACT field corresponding to the bit position for each command TAG that has completed since the last status notification was transmitted. The ERR bit in the Status register shall be cleared to zero and the value in the Error register shall be zero.

The ACT field occupies the last 32 bits of the Set Device Bits FIS as defined in Figure ___ below.

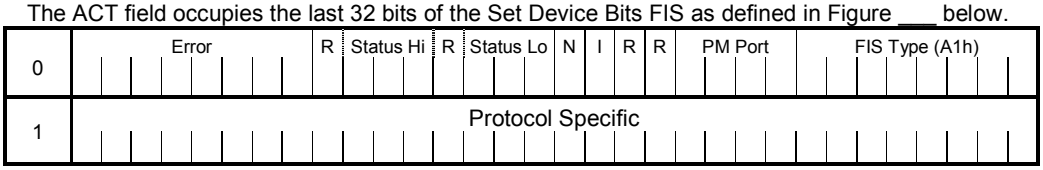

Figure ____ – Set Device Bits FIS for successful NCQ command completion

ACT The ACT field of the Set Device Bits FIS communicates successful completion notification for each of up to 32 queued commands. The field is bit-significant and the device sets bit positions to one for each command tag it is indicating successful completion notification for. The device may set more than one bit to one if it is explicitly aggregating successful status returns.

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Error The Error register shall be cleared to zero.
Status As defined in section 10.3.6. The ERR bit shall be cleared to zero indicating successful command completion.
I Interrupt bit. The interrupt bit shall be set to one.
All other fields as defined in section 10.3.6.

Devices should be aware that if choosing to aggregate status to the point where many of the outstanding commands have actually completed successfully without notification to the host, that an error may cause the final completion status of those commands to be failure. The device should be selective when using status aggregation for outstanding queued commands to ensure the host is made aware of successful completion for outstanding commands in a way that an error would not force a high number of unnecessary command retries.

10.3.5.2.3 Error Outputs

10.3.5.2.3.1 Upon Receipt of a Command

If the device has received a command that has not yet been acknowledged by clearing the BSY bit to zero and an error is encountered, the device shall transmit a Register FIS (see figure ____ below) to the host with the ERR bit set to one and the BSY bit cleared to zero in the Status field, the ATA error code in the Error field.

Register	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Error	Error							
Count (7:0)	na							
Count (15:8)	na							
LBA (7:0)	na							
LBA (31:24)	na							
LBA (15:8)	na							
LBA (39:32)	na							
LBA (23:16)	na							
LBA (47:40)	na							
Device	na							
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Figure _____ –RECEIVE FPDMA QUEUED error status result values on command receipt

Deleted: RECIEVE

ERROR ATA error code for the failure condition of the failed command
BSY 0
DRDY 1
DF 0
DRQ 0
ERR 1

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Following transmission of the Register FIS, the device shall stop processing any outstanding or new commands until the Queued Error Log (see 13.7) has been read before continuing to abort all outstanding commands. See 13.6.3.5 for more details.

10.3.5.2.3.2 During Execution of a Command

If all commands have been acknowledged by clearing the BSY bit to zero and an error condition is detected, the device shall transmit a Set Device Bits FIS (see Figure ____ below) to the host with the ERR bit set to one in the Status field, the ATA error code in the Error field, and the Interrupt bit set to one. All outstanding commands at the time of an error shall be aborted as part of the error response and may be re-issued as appropriate by the host. For any commands that have not completed successfully or have resulted in error, the device shall clear the corresponding ACT bits to zero in the Set Device Bits FIS.

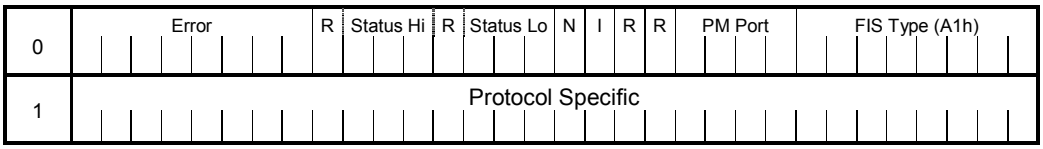

Figure ____ – Set Device Bits FIS with error notification, and command completions

ACT — The ACT field of the Set Device Bits FIS communicates successful completion notification for each of up to 32 queued commands. The field is bit-significant and the device sets bit positions to one for each command tag it is indicating successful completion notification for. The device may set more than one bit to one if it is explicitly aggregating successful status returns.

Error — The Error register shall contain the ATA error code.

Status — As defined in 10.3.6. The ERR bit shall be set to one indicating an NCQ error has occurred.

I — Interrupt bit. The interrupt bit shall be set to one.

All other fields as defined in section 10.3.6.

Only the registers that are updated as part of the Set Device Bits FIS are modified if the device signals an error condition when the BSY bit in the shadow Status register is cleared to zero, leaving the other Shadow Register Block Registers unchanged. If the device signals an error condition when the BSY bit in the shadow Status register is set to one, the device clears the BSY bit to zero with a Register FIS which updates all registers in the Shadow Register Block.

Following transmission of the Set Device Bits FIS, the device shall stop processing any outstanding or new commands until the Queued Error Log (see 13.7) has been before continuing to abort all outstanding commands. See 13.6.3.5 for more details.

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10.3.5.3 SEND FPDMA QUEUED

512 Byte Block DMA OUT subcommandss make use of this transport command. The SEND FPDMA QUEUED command supports LBA mode only and uses 48-bit addressing only. The format of the command is defined in Figure _____.

Deleted: sub command

10.3.5.3.1 Inputs

Register	7	6	5	4	3	2	1	0
Features (7:0)	Sector Count 7:0							
Features (15:8)	Sector Count 15:8							
Count (7:0)	TAG					Reserved		
Count (15:8)	PRIO 1:0		Res	Subcommand				
LBA Low (7:0)	LBA 7:0							
LBA Low (31:24)	LBA 31:24							
LBA Mid (15:8)	LBA 15:8							
LBA Mid (39:32)	LBA 39:32							
LBA High (23:16)	LBA 23:16							
LBA High (47:40)	LBA 47:40							
ICC	ICC 7:0							
Auxiliary(7:0)	Auxiliary (7:0)							
Auxiliary (15:8)	Auxiliary (15:8)							
Device	Res	1	Res	0	Reserved			
Command	**64h**							

Deleted: SubCommand

Figure _____ – SEND FPDMA QUEUED command definition

Deleted: Command

Count The number of 512 byte blocks to be transferred, 0000h indicates that 65,536 512 byte blocks are to be transferred.

TAG The TAG value shall be assigned by host software to be different from all other TAG values corresponding to outstanding commands. The assigned TAG value shall not exceed the value specified in IDENTIFY DEVICE word 75.

PRIO The Priority (PRIO) value shall be assigned by the host based on the priority of the command issued. The device shall make a best effort to complete High priority requests in a more timely fashion than Normal and Isochronous priority requests. The device shall make a best effort to complete Isochronous priority requests prior to its associated deadline. The Priority values are defined as follows:

00b	Normal Priority
01b	Isochronous – deadline dependent priority
10b	High priority
11b	Reserved

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Subcommand

Deleted: Sub Command

The values of this field is defined in section 10.3.6 of this specification.

Deleted: defined on a per command basis as

LBA The values of this field is defined in section 10.3.6 of this specification.

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ICC The Isochronous Command Completion (ICC) field shall be assigned by the host based on the intended deadline associated with the command issued. By default, when deadline is expired, the device shall continue to complete the command as soon as possible.

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Auxiliary The values of this field is defined in section 10.3.6 of this specification.

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Upon accepting the command, the device shall clear the BSY bit if/when it is prepared to receive another command by transmitting a Register FIS to the host with the BSY bit cleared to zero in the Status field of the FIS. The ability for the device to quickly clear the BSY bit allows the host to issue another queued command without blocking on this bit. The host shall check the BSY bit in the shadow Status register before attempting to issue a new command in order to determine that the device is ready to receive another command (and determine that the host has write access to the Shadow Register Block Registers). The device shall not trigger an interrupt in response to having successfully received the command, so the initial status return that clears BSY shall not have an interrupt associated with it.

10.3.5.3.2 Success Outputs

Upon successful completion of one or more outstanding commands, the device shall transmit a Set Device Bits FIS with the Interrupt bit set to one and one or more bits set to one in the ACT field corresponding to the bit position for each command TAG that has completed since the last status notification was transmitted. The ERR bit in the Status register shall be cleared to zero and the value in the Error register shall be zero.

The ACT field occupies the last 32 bits of the Set Device Bits FIS as defined in Figure ___ below.

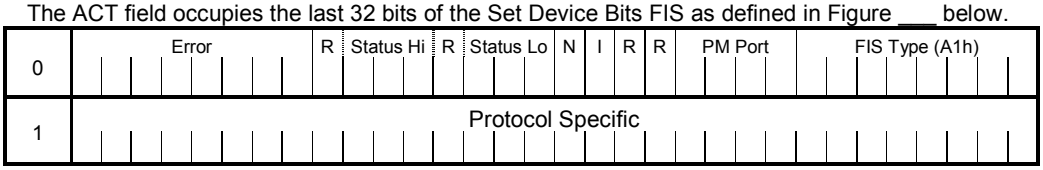

Figure ____ – Set Device Bits FIS for successful NCQ command completion

ACT The ACT field of the Set Device Bits FIS communicates successful completion notification for each of up to 32 queued commands. The field is bit-significant and the device sets bit positions to one for each command tag it is indicating successful completion notification for. The device may set more than one bit to one if it is explicitly aggregating successful status returns.

Error The Error register shall be cleared to zero.

Status As defined in section 10.3.6. The ERR bit shall be cleared to zero indicating successful command completion.

I Interrupt bit. The interrupt bit shall be set to one.

All other fields as defined in section 10.3.6.

Devices should be aware that if choosing to aggregate status to the point where many of the outstanding commands have actually completed successfully without notification to the host, that an error may cause the final completion status of those commands to be failure. The device should be selective when using status aggregation for outstanding queued commands to ensure the host is made aware of successful completion for outstanding commands in a way that an error would not force a high number of unnecessary command retries.

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10.3.5.3.3 Error Outputs

If the device has received a command that has not yet been acknowledged by clearing the BSY bit to zero and an error is encountered, the device shall transmit a Register FIS (see figure ____ below) to the host with the ERR bit set to one and the BSY bit cleared to zero in the Status field, the ATA error code in the Error field.

Register	7	6	5	4	3	2	1	0
Error	Error							
Count (7:0)	na							
Count (15:8)	na							
LBA (7:0)	na							
LBA (31:24)	na							
LBA (15:8)	na							
LBA (39:32)	na							
LBA (23:16)	na							
LBA (47:40)	na							
Device	na							
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Figure _____ – SEND FPDMA QUEUED error status result values on command receipt

ERROR	ATA error code for the failure condition of the failed command
BSY	0
DRDY	1
DF	0
DRQ	0
ERR	1

Following transmission of the Register FIS, the device shall stop processing any outstanding or new commands until the Queued Error Log (see 13.7) has been read before continuing to abort all outstanding commands. See 13.6.3.5 for more details.

10.3.5.3.3.1 During Execution of a Command

If all commands have been acknowledged by clearing the BSY bit to zero and an error condition is detected, the device shall transmit a Set Device Bits FIS (see Figure ____ below) to the host with the ERR bit set to one in the Status field, the ATA error code in the Error field, and the Interrupt bit set to one. All outstanding commands at the time of an error shall be aborted as part of the error response and may be re-issued as appropriate by the host. For any commands that have not completed successfully or have resulted in error, the device shall clear the corresponding ACT bits to zero in the Set Device Bits FIS.

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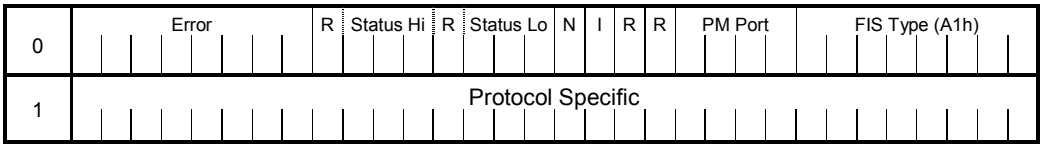

Figure ____ – Set Device Bits FIS with error notification, and command completions

ACT	The ACT field of the Set Device Bits FIS communicates successful completion notification for each of up to 32 queued commands. The field is bit-significant and the device sets bit positions to one for each command tag it is indicating successful completion notification for. The device may set more than one bit to one if it is explicitly aggregating successful status returns.
Error	The Error register shall contain the ATA error code.
Status	As defined in 10.3.6. The ERR bit shall be set to one indicating an NCQ error has occurred.
I	Interrupt bit. The interrupt bit shall be set to one.

All other fields as defined in section 10.3.6.

Only the registers that are updated as part of the Set Device Bits FIS are modified if the device signals an error condition when the BSY bit in the shadow Status register is cleared to zero, leaving the other Shadow Register Block Registers unchanged. If the device signals an error condition when the BSY bit in the shadow Status register is set to one, the device clears the BSY bit to zero with a Register FIS which updates all registers in the Shadow Register Block.

Following transmission of the Set Device Bits FIS, the device shall stop processing any outstanding or new commands until the Queued Error Log (see 13.7) has been before continuing to abort all outstanding commands. See 13.6.3.5 for more details.

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10.3.6 SEND FPDMA QUEUED Subcommands

Deleted: Sub Command

Subcommands for the SEND FPDMA QUEUED commands are contained within the Sector Count (13:8) field. The allowed values are defined in Table _____ below.

Deleted: SubCommands

Value	Subcommand
00h	Data Set Management (see Section 10.3.6.1)
01h-1Fh	Reserved

Deleted: SubCommand

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Table ____ - Subcommands for SEND FPDMA QUEUED

Deleted: SubCommands

10.3.6.1 DATA SET MANAGEMENT

The DATA SET MANAGEMENT subcommand functionality and behavior is dependent on all requirements of the DATA SET MANAGEMENT command and the IDENTIFY DEVICE command defined in ACS-2.

Deleted: SubCommand

Deleted: Data Set Management

Deleted: Command

Deleted: Identify Device

Deleted: Command

10.3.6.1.1 Inputs

Register	7	6	5	4	3	2	1	0
Auxiliary (7:0)	Reserved							Trim
Auxiliary (15:8)	Reserved							
LBA (7:0)	Reserved							
LBA (31:24)	Reserved							
LBA (15:8)	Reserved							
LBA (39:32)	Reserved							
LBA (23:16)	Reserved							
LBA (47:40)	Reserved							

Figure _____ – SEND FPDMA QUEUED, Subcommand = 00h

Deleted: SubCommand

Trim As defined by the DATA SET MANAGEMENT command in ACS-2.

Deleted: Data Set Management

Deleted: Command

10.3.6.1.2 Success Outputs

See SEND FPDMA QUEUED Success Outputs Section

10.3.6.1.3 Error Outputs

See SEND FPDMA QUEUED Error Outputs Section

10.3.6.1.4 Output from the Host to the Device Data Structure

As defined in the DATA SET MANAGEMENT command in ACS-2.

Deleted: Data Set Management

Deleted: Command

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