Proposed Draft

Serial ATA International Organization

Version 3

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Title : Speed Clarification

Proposed change to Serial ATA Revision 3.0

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Document History

Workgroup	Chairperson Name	Email address
1	03/14/2009	Initial draft.
2	3/23/2009	Modified table text for when word 77, bits 3:1 = 000b
3	3/30/2009	

1 Introduction

It has been pointed out that Serial ATA Revision 3.0 is not completely clear about which signalling speeds are required. This proposes text changes for clarification.

2 Proposed Changes to Serial ATA Revision 3.0

[editor note: New text is marked as underlined in blue color. Material to be deleted ~~is red with strikethrough markings.~~]

7.4.25.1.2 Speed Negotiation

Speed negotiation and transition to lower serial interface data rates shall be implemented for higher data speed compatible interfaces, negotiating and transitioning down to lower data speed, as required. There is no requirement for speed negotiation and transition to lower speeds than Gen1. ~~If the Gen2 speed is supported, then the device shall support the Gen1 speed. If Gen3 is supported, then the device shall support Gen1 and Gen2 speeds.~~If Gen2 speed is supported, then Gen1 speed shall be supported. If Gen3 speed is supported, then Gen1 and Gen2 speeds shall be supported.

13.2.1.16 Word 76: Serial ATA capabilities

If not 0000h or FFFFh, the device claims compliance with the Serial ATA specification and supports the signaling speed indicated in bits 1-3. Since Serial ATA supports generational compatibility, multiple bits may be set. Bit 0 is reserved and shall be cleared to zero (thus a Serial ATA device has at least one bit cleared in this field and at least one bit set providing clear differentiation). If this field is not 0000h or FFFFh, words 77 through 79 shall be valid. If this field is 0000h or FFFFh the device does not claim compliance with the Serial ATA specification and Words 76 through 79 are not valid and shall be ignored.

Bit 0 shall be cleared to zero.

Bit 1 when set to one indicates that the device is a Serial ATA device and supports the Gen1 signaling speed of 1.5 Gbps. See 7.4.25.1.2.

Bit 2 when set to one indicates that the device is a Serial ATA device and supports the Gen2 signaling speed of 3.0 Gbps. See 7.4.25.1.2.

Bit 3 when set to one indicates that the device is a Serial ATA device and supports the Gen3 signaling speed of 6.0 Gbps. See 7.4.25.1.2.

Bit 4-7 are reserved for future Serial ATA signaling speed grades and shall be cleared to zero.

Bit 8 when set to one indicates that the Serial ATA device supports the Native Command Queuing scheme defined in section 13.6.

Bit 9 when set to one indicates that the Serial ATA device supports the Partial and Slumber interface power management states when initiated by the host.

Bit 10 when set to one indicates that the Serial ATA device supports Phy event counters. If the device supports Phy event counters, it shall support the Phy Event Counter Log (see 13.9.3)

Bit 11 when set to one indicates that the device supports performing an unload/park of the heads upon reception of the IDLE IMMEDIATE command with the Unload Feature specified while NCQ commands are outstanding. This bit shall only be set to one if the device supports NCQ as shown in bit 8 of Word 76.

Bit 12 when set to one indicates that the device supports the Priority field in the READ FPDMA QUEUED and WRITE FPDMA QUEUED commands and optimization based on this information. This bit shall only be set to one if the device supports NCQ as shown in bit 8 of Word 76.

Bit 13 indicates that the device supports host Automatic Partial to Slumber transitions. The device shall tolerate a Partial exit latency up to the max Slumber exit latency. This allows the host to asynchronously transition from Partial to Slumber. If Word 76, bit 9 (supports receipt of host-initiated interface power management requests) is cleared to zero, then bit 13 shall be cleared to zero.

Bit 14 indicates that the device supports Automatic Partial to Slumber transitions and may asynchronously transition from Partial to Slumber when enabled. If Word 78, bit 3 (supports initiating interface power management) is cleared to zero, then Word 76 bit 14 shall be cleared to zero.

Bit 15 when set to one indicates that either the READ LOG DMA EXT and READ LOG EXT commands may be used in all cases with identical results (see 13.7). If IDENTIFY DEVICE word 119 bit 3 is cleared to zero, this bit shall be cleared to zero. If bit 15 is cleared to zero and the host issues the READ LOG DMA EXT command to read the Queued Error Log or the Phy Event Counters log, the device shall return command aborted.

13.2.1.17 Word 77: Serial ATA Additional capabilities

Word 77 reports additional optional capabilities supported by the device. Support for this word is optional and if not supported, the word shall be zero indicating the device has no support for additional Serial ATA capabilities.

Bit 0 shall be cleared to zero

Bits 1-3 are a coded value that indicates the Serial ATA Phy speed at which the device is currently communicating. Table 76 defines these values:

Old Table 76

Coded Values			
Bit 3	Bit 2	Bit 1	Description
0	0	1	Gen1 signaling speed of 1.5 Gbps
0	1	0	Gen2 signaling speed of 3.0 Gbps
0	1	1	Gen3 signaling speed of 6.0 Gbps
All Non-Defined Values			Reserved for future Serial ATA signaling speeds

Replacement Table 76

Coded Values			
Bit 3	Bit 2	Bit 1	Description
0	0	0	Reporting of current signalling speed is not supported
0	0	1	Current signalling speed is Gen1
0	1	0	Current signalling speed is Gen2
0	1	1	Current signalling speed is Gen3
All other values			Reserved