

**Proposed  
Draft**

**Serial ATA  
International Organization**

**Version 0.01  
March 17, 2009**

---

**TPD\_117\_20090317\_v001**

**Title : Apply SATA 2.5 Design Guide 2 for all  
devices**

**Proposed change to Serial ATA Revision 3.0**

This is an internal working document of the Serial ATA International Organization. As such, this is not a completed standard and has not been approved. The Serial ATA International Organization may modify the contents at any time. This document is made available for review and comment only.

Permission is granted to the Promoters, Contributors and Adopters of the Serial ATA International Organization to reproduce this document for the purposes of evolving the technical content for internal use only without further permission provided this notice is included. All other rights are reserved and may be covered by one or more Non Disclosure Agreements including the Serial ATA International Organization participant agreements. Any commercial or for-profit replication or republication is prohibited. Copyright © 2000-2009 Serial ATA International Organization. All rights reserved.

This Draft Specification is NOT the final version of the Specification and is subject to change without notice. A modified, final version of this Specification ("Final Specification") when approved by the Promoters will be made available for download at this Web Site: <http://www.serialata.org>.

THIS DRAFT SPECIFICATION IS PROVIDED "AS IS" WITH NO WARRANTIES WHATSOEVER, INCLUDING ANY WARRANTY OF MERCHANTABILITY, NON-INFRINGEMENT, FITNESS FOR ANY PARTICULAR PURPOSE OR ANY WARRANTY OTHERWISE ARISING OUT OF ANY PROPOSAL, SPECIFICATION, OR SAMPLE. Except for the right to download for internal review, no license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted or intended hereunder.

THE PROMOTERS DISCLAIM ALL LIABILITY, INCLUDING LIABILITY FOR INFRINGEMENT OF ANY PROPRIETARY RIGHTS, RELATING TO USE OF INFORMATION IN THIS DRAFT SPECIFICATION. THE PROMOTERS DO NOT WARRANT OR REPRESENT THAT SUCH USE WILL NOT INFRINGE SUCH RIGHTS.

THIS DOCUMENT IS AN INTERMEDIATE DRAFT FOR COMMENT ONLY AND IS SUBJECT TO CHANGE WITHOUT NOTICE.

\* Other brands and names are the property of their respective owners.

Copyright © 2005-2009 Serial ATA International Organization. All rights reserved.

### Author Information

Author Name	Company	Email address
Jim Hatfield	Seagate	James.C.Hatfield@seagate.com

### Workgroup Chair Information

Workgroup	Chairperson Name	Email address
Digital	Mladen Luksic	Mladen.Luksic@wdc.com

### Document History

Version	Date	Comments
1	03/17/2009	Initial draft.

## 1 Introduction

Serial ATA Revision 2.5 Design Guide 002 (“SATA25\_Supp\_002.pdf”) contains material describing the situation when a software reset is sent by the host after the OOB sequence has completed but before the device has sent the signature FIS34h.

It inserted language into the Port Multiplier section, but the material really applies to all device types.

This document proposes to insert the language into a different section of the specification and to remove similar language from the port multiplier section.

## 2 Summary of Design Guide 2 Recommendation

### “Recommended Host Behavior:

It is recommended that host software not issue SRST prior to successful reception of the Signature FIS by the host, unless the host is Port Multiplier aware. In a scenario of a failed/timed out power up or hardware reset, the recommended recovery is the issuance of a hard reset (i.e. COMRESET). “

### “Recommended Device Behavior:

In the case that a device has not sent a Signature FIS (e.g. prior to completion of spin-up) and receives X\_RDY from the host, a device may hold off responding with R\_RDY until its application layer is in a state which it is able to process a new command/control FIS from the host controller including SRST. In some cases, this may be held off until after transmission of the Signature FIS. A device is required to respond to the host’s X\_RDY transmission, but the response may be deferred as mentioned above. “

## 3 Proposed Changes to Serial ATA Revision 3.0

[editor note: New text is marked as underlined in blue color. Material to be deleted ~~is red with strikethrough markings.~~ ]

**9.6.4 Link Receive State Diagram**

**Table 71 – State Diagram Link Receive**

<b>LR1: L_RcvChkRdy</b>	Transmit R_RDY <sub>P</sub> .	
1. X_RDY <sub>P</sub> received from Phy.	→	L_RcvChkRdy
2. SOF <sub>P</sub> received from Phy.	→	L_RcvData
3. Any Dword other than (X_RDY <sub>P</sub> or SOF <sub>P</sub> ) received from Phy.	→	L_IDLE
4. PHYRDY <sub>n</sub>	→	L_NoCommErr <sup>1</sup>
NOTES: 1. The Link layer shall notify the Transport layer of the condition and fail the attempted transfer.		

  

<b>LR2: L_RcvWaitFifo</b>	Transmit SYNC <sub>P</sub> .	
1. X_RDY <sub>P</sub> received from Phy and FIFO space available.	→	L_RcvChkRdy
2. X_RDY <sub>P</sub> received from Phy and FIFO space not available.	→	L_RcvWaitFifo
3. Any Dword other than X_RDY <sub>P</sub> received from Phy.	→	L_IDLE
4. PHYRDY <sub>n</sub>	→	L_NoCommErr <sup>1</sup>
NOTES: 1. The Link layer shall notify the Transport layer of the condition and fail the attempted transfer.		

**LR1: L\_RcvChkRdy state:** This state is entered when X\_RDY<sub>P</sub> has been received from the Phy layer.

When in this state, the Link layer shall transmit R\_RDY<sub>P</sub> and wait for SOF<sub>P</sub> from the Phy layer.

In the case that a device has not sent a Signature FIS (e.g. prior to completion of spin-up) and receives X\_RDY from the host, a device may hold off responding with R\_RDY until its application layer is in a state which it is able to process a new command/control FIS from the host controller including SRST. In some cases, this may be held off until after transmission of the Signature FIS. A device is required to respond to the host's X\_RDY transmission, but the response may be deferred as mentioned above.

**Transition LR1:1:** When the Link layer receives X\_RDY<sub>P</sub> from the Phy layer, the Link layer shall make a transition to the LR1: L\_RcvChkRdy state.

#### **13.15.4.1.1 Considerations when Port Multiplier Not Present**

Directly attached devices may not be prepared to receive a software reset from the host prior to transmission of the Signature FIS.

It is recommended that host software not issue software reset prior to successful reception of the Signature FIS by the host, unless the host is Port Multiplier aware.

~~Devices may receive a software reset prior to transmission of the Signature FIS if the host is Port Multiplier aware. In the case that a device has not sent a Signature FIS and receives X\_RDY<sub>P</sub> from the host, a device may hold off responding with R\_RDY<sub>P</sub> until its application layer is in a state that is able to process a new command/control FIS from the HBA, including software reset. In some cases, the device may hold off transmission of R\_RDY<sub>P</sub> until it is prepared to transmit the Signature FIS.~~