Proposed **Serial ATA**
Draft **International Organization**

Version 01

October 12, 2009

SATA30_TPR_D125_20091012_V02
Title: NCQ Status bit 4

Proposed change, new functionality, or behavior to Serial ATA Revision 3.0

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Document History

Version	Date	Comments
1	08/25/2009	Initial draft
2	10/12/2009	Added description for normal and error returns for all FPDMA QUEUED protocol commands, and removed the description in the SDB FIS description because it was not sufficient.

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1 Introduction

There has long been widespread confusion about whether an NCQ command completes with Status bit 4 set to one or cleared to zero.

Success: x40 vs. x50

Error: x41 vs. x51

2 Summary of the problem

Current Interoperability tests allow either value.

This proposal clarifies that either value is acceptable.

Section 10.3.6 is referenced by all Success Output and Error Output sections for all NCQ commands, and not by any non-NCQ commands.

3 Proposed correction

[editor note: New text is marked as underlined in blue color. Material to be deleted ~~is red with strikethrough markings.~~]

[editors note:
[make the following change to all of these sections (as appropriate to each command):
[13.6.3.2 success outputs (for READ FPDMA QUEUED)
[13.6.3.6 success outputs (for WRITE FPDMA QUEUED)
[13.XX success outputs (for NCQ QUEUE MANAGEMENT)
[13.xxx success outputs (for SEND FPDMA QUEUED)
[13.xxx success outputs (for RECEIVE FPDMA QUEUED)

3.1.1.1 Success Outputs [editors note: this is actually 13.6.3.2]

Upon successful completion of one or more outstanding commands, the device shall transmit a Set Device Bits FIS with the Interrupt bit set to one and one or more bits set to one in the ACT field corresponding to the bit position for each command TAG that has completed since the last status notification was transmitted. The ERR bit in the Status register shall be cleared to zero and the value in the Error register shall be zero.

The ACT field occupies the last 32 bits of the Set Device Bits FIS as defined in Figure 190 below.

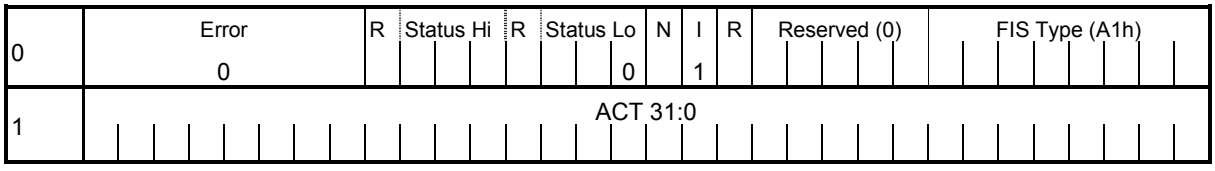

Figure 190 – Set Device Bits FIS for successful READ FPDMA QUEUED command completion

ACT The ACT field of the Set Device Bits FIS communicates successful completion notification for each of up to 32 queued commands. The field is bit-significant and the device sets bit positions to one for each command tag it is indicating

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successful completion notification for. The device may set more than one bit to one if it is explicitly aggregating successful status returns.

Error — The Error register shall be cleared to zero.

Status — As defined in section 10.3.6. The ERR bit shall be cleared to zero indicating successful command completion. Bit 4 may be set to one.

I — Interrupt bit. The interrupt bit shall be set to one.

All other fields as defined in section 10.3.6.

NOTE: Devices should be aware that if choosing to aggregate status to the point where many of the outstanding commands have actually completed successfully without notification to the host, that an error may cause the final completion status of those commands to be failure. A device should be selective when using status aggregation for outstanding queued commands to ensure the host is made aware of successful completion for outstanding commands in a way that an error would not force a high number of unnecessary command retries.

3.1.1.2 Error Outputs

3.1.1.2.1.1 Upon receipt of a command

If the device has received a command that has not yet been acknowledged by clearing the BSY bit to zero and an error is encountered, the device shall transmit a Register FIS (see Figure 1) to the host with the ERR bit set to one and the BSY bit cleared to zero in the Status field, the ATA error code in the Error field.

Register	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Error	ERROR							
Count(7:0)	na							
Count(15:8)	na							
LBA(7:0)	na							
LBA(31:24)	na							
LBA(15:8)	na							
LBA(39:32)	na							
LBA(23:16	na							
LBA(47:40)	na							
Device	na							
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Figure 1 – READ FPDMA QUEUED error on command receipt

ERROR — ATA error code for the failure condition of the failed command

BSY — 0

DRDY — 1

DF — 0

DRQ — 0

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ERR 1

Status bit 4 may be set to one.

Following transmission of the Register FIS, the device shall stop processing any outstanding or new commands until the Queued Error Log (see **Error! Reference source not found.**) has been read before continuing to abort all outstanding commands.

3.1.1.2.1.2 During execution of a command

If all commands have been acknowledged by clearing the BSY bit to zero and an error condition is detected, the device shall transmit a Set Device Bits FIS (see Figure 191 below) to the host with the ERR bit set to one in the Status field, the ATA error code in the Error field, and the Interrupt bit set to one. All outstanding commands at the time of an error shall be aborted as part of the error response and may be re-issued as appropriate by the host. For any commands that have not completed successfully or have resulted in error, the device shall clear the corresponding ACT bits to zero in the Set Device Bits FIS.

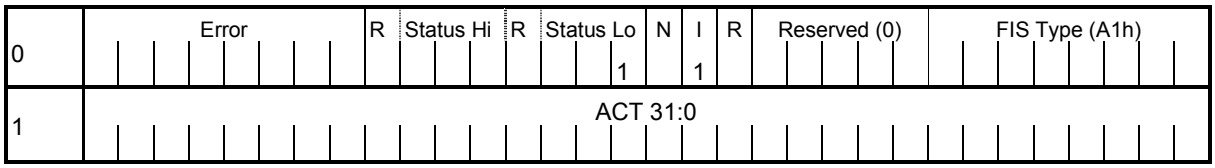

Figure 2 - Set Device Bits FIS with error notification, and command completions

SActive The ACT field of the Set Device Bits FIS communicates successful completion notification for each of up to 32 queued commands. The field is bit-significant and the device sets bit positions to one for each command tag it is indicating successful completion notification for. The device may set more than one bit to one if it is explicitly aggregating successful status returns.

Error The Error register shall contain the ATA error code.

Status As defined in section 10.3.6. The ERR bit shall be set to one indicating an NCQ error has occurred. Status bit 4 may be set to one.

I Interrupt bit. The interrupt bit shall be set to one.

All other fields as defined in section 10.3.6.

Only the registers that are updated as part of the Set Device Bits FIS are modified if the device signals an error condition when the BSY bit in the Shadow Status register is cleared to zero, leaving the other Shadow Register Block Registers unchanged. If the device signals an error condition when the BSY bit in the shadow Status register is set to one, the device clears the BSY bit to zero with a Register FIS which updates all registers in the Shadow Register Block, but the corresponding error information for the command is still retrieved by reading the Queued Error Log.

Following transmission of the Set Device Bits FIS, the device shall stop processing any outstanding or new commands until the Queued Error Log has been read before continuing to abort all outstanding commands. See **Error! Reference source not found.** for more details.

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