Proposed **Serial ATA**

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Title: Hardware Control Feature Mechanism

Proposed change, new functionality, or behavior to Serial ATA Revision 3.0

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Author Information

Author Name	Company	e-mail address
Jim Hatfield	Seagate Technology	james.c.hatfield@seagate.com
Patrick Hery	Toshiba	patrick.hery@tais.toshiba.com

Workgroup Chair Information

Workgroup	Chairperson Name	e-mail address
Digital	Jim Hatfield	james.c.hatfield@seagate.com

Document History

Version	Date	Comments
00	04/072/2010	Initial merge of C104 and D131 drafts
01	06/07/2010	Changes so DHU only released when negated or POR.
02	06/07/2010	Edited set features to disallow reversion to legacy behavior without a POR and removed DHU released section based on committee discussions. Removed pin verbiage for smoother reading.
03	06/13/2010	Changes requested by the review of 6/14/2010
04	07/07/2010	Changes requested by the review of 6/28/2010
05	07/25/2010	Changes requested by the review of 7/19/2010, added overview, default, extended descriptions, reorganized 13.new to eliminate unnecessary description.
06	07/26/2010	Changes requested by the review of 7/26/2010, added info to table 6 to specify software reset, COMRESET behavior, extended DHU to cover non rotating devices.
07	08/02/2010	Changes requested by the review of 8/02/2010, added regarless of SSP seting in table 6, reworded verbiage on DHU for non rotating devices.

1 Introduction

There are a variety of hardware control features that exist in SATA. The two most commonly used features are listed as:

A. disable staggered spin-up (DSS)
B. Device activity signal (e.g. LED) (DAS)

Due to various hardware issues, these features are mapped onto different physical pins depending on the connecter type as indicated in Table 1 below. Not all features are defined for all connecter types.

Table 1 - DSS and DAS for various connectors

Standard Connector (3.5" & 2.5")	1.8" mSATA Connector	LIF-SATA Connector
Pin 11: • DSS • DAS	Pin 7: • DAS	Pin 8: • DSS • DAS

2 Summary of the problem

Additional hardware control features are being deployed in drives today. Some features are vendor specific and some are not. One such feature is used in some laptop computers that have a free fall detection feature that detects a free fall event and unloads the heads to prevent failures due to head slap on the media. An electrical signal is sent to the HDD to initiate the head unload instead of using the IDLE IMMEDIATE command. This feature will subsequently be referred to as "Direct Head Unload" DHU.

There are possible interoperability issues when drives with different hardware control feature sets are re-purposed or if a drive is replaced with a different drive at a later time. The interoperability issues can extend to damage if improper electrical connections occur. This proposal defines a method for the host to determine if additional hardware control modes are available and to request the drive to change to a different operating mode.

Note: This proposal is dependent on a T13 proposal that is still in discussion:

e08156 - Identify Data log

3 Proposed changes

[editor note: New text is marked as underlined in blue color. Material to be deleted ~~is red with strikethrough markings.~~]

[editors note: add section 4.1.new to section 4.1 Definitions.]

3.1 [editors note: 4.1.new] Hardware Feature Control Pins

For the LIF-SATA connector, Hardware Feature Control (See 13.new) are connector pins P8 and P21. For the 1.8 inch mSATA connector, Hardware Feature Control is connector pin P7. For all other connectors Hardware Feature Control is connector pin P11.

3.2 [editors note: 4.1.new] Direct Head Unload (DHU)

An active high electrical signal used to request that a rotating media device retract the heads from the media. (see 6.new and 13.x)

3.3 Physical Pin Locations

3.3.1 [editors note: 6.1.3.2] Standard SATA Connector (3.5-inch & 2.5-inch HDD)

Table 3

	Name	Type	Description	Cable Usage[2,3]	Backplane Usage[3]
Signal Segment Key					
Signal Segment	S1	GND		1st Mate	2nd Mate
	S2	A+	Differential Signal Pair A	2nd Mate	3rd Mate
	S3	A-		2nd Mate	3rd Mate
	S4	GND		1st Mate	2nd Mate
	S5	B+	Differential Signal Pair B	2nd Mate	3rd Mate
	S6	B-		2nd Mate	3rd Mate
	S7	GND		1st Mate	2nd Mate
Signal Segment "L"					
Central Connector Gap[4]					
Power Segment "L"					
Power Segment	P1	V_{33}	3.3 V Power	2nd Mate	3rd Mate
	P2	V_{33}	3.3 V Power	2nd Mate	3rd Mate
	P3	V_{33}	3.3 V Power, Pre-charge	1st Mate	2nd Mate
	P4	GND		1st Mate	1st Mate
	P5	GND		1st Mate	2nd Mate
	P6	GND		1st Mate	2nd Mate
	P7	V_5	5 V Power, Pre-charge	1st Mate	2nd Mate
	P8	V_5	5 V Power	2nd Mate	3rd Mate
	P9	V_5	5 V Power	2nd Mate	3rd Mate
	P10	GND		1st Mate	2nd Mate
	P11	DAS/DSS/DHU	Device Activity Signal / Disable Staggered Spin-up / Direct Head Unload / Vendor Specific[1]	2nd Mate	3rd Mate
	P12	GND		1st Mate	1st Mate
	P13	V_{12}	12 V Power, Pre-charge	1st Mate	2nd Mate
	P14	V_{12}	12 V Power	2nd Mate	3rd Mate
	P15	V_{12}	12 V Power	2nd Mate	3rd Mate
Power Segment Key					

NOTE:

1. ~~The corresponding pin to be mated with P11 in the power cable receptacle connector shall always be grounded~~. For specific optional usage of pin P11 see section 6.7.
2. Although the mate order is shown, hot plugging is not supported with using the cable connector receptacle.
3. All mate sequences assume zero angular offset between connectors.
4. The signal segment and power segment may be separate.

3.3.2 [editors note: 6.2.4.5] Internal micro SATA pin signal definition and contact mating sequence

Table 10 – Signal and Power Internal Micro SATA Plug and Nominal Mate Sequence

	Name	Type	Description	Cable Usage[1,2]	Backplane Usage[2]
Signal Segment	Refer to Table 3.				
Spacing separate signal and power segments[3]					
Power Segment	P1	V_{33}	3.3 V Power	2nd Mate	3rd Mate
	P2	V_{33}	3.3 V Power, Pre-charge	1st Mate	2nd Mate
	P3	GND		1st Mate	1st Mate
	P4	GND		1st Mate	1st Mate
	P5	V_5	5 V Power, Pre-charge[4]	1st Mate	2nd Mate
	P6	V_5	5 V Power[4]	2nd Mate	3rd Mate
	P7	DAS/DHU	DAS/Direct Head Unload / Vendor Specific[5]	2nd Mate	3rd Mate
	Key	Key	Key	NC	NC
	P8	Optional	Vendor specific[6]	2nd Mate	3rd Mate
	P9	Optional	Vendor specific[6]	2nd Mate	3rd Mate

NOTE:

1. Although the mate order is shown, hot plugging is not supported when using the cable connector receptacle.
2. All mate sequences assume zero angular offset between connectors.
3. The signal segment and power segment may be separate.
4. The 5 V supply voltage pins are included to meet future product requirements and may optionally be provided on the power segment receptacle. Future revisions of this specification may require 5 V supply voltage be provided.
5. ~~The corresponding pin to be mated with pin P7 in the power Internal Micro receptacle connector shall always be grounded.~~ For specific optional usage of pin P7, see section 6.7.
6. No connect on the host side.

3.3.3 [editors note: 6.4.4] Internal LIF-SATA pin signal definition and contact mating sequence

Table 15 - Signal and Power Internal LIF-SATA Plug

Name	Type	Description
P1	GND	
P2	V_{33}	3.3 V Power
P3	V_{33}	3.3 V Power
P4	GND	
P5	V_5	5 V Power
P6	V_5	5 V Power[1]
P7	GND	
P8	DAS/DSS/Vendor Specific	Device Activity Signal/Disable Staggered Spin-up/Vendor Specific[2]
P9	GND	
P10	GND	
P11	A+	Differential Signal Pair A
P12	A-	
P13	GND	
P14	B+	Differential Signal Pair B
P15	B-	
P16	GND	
P17	GND	
P18	Vendor	Vendor Specific
P19	Vendor	Vendor Specific
P20	Vendor	Vendor Specific
P21	~~Vendor~~ DHU	~~Vendor Specific~~ Direct Head Unload[4]
P22	Vendor	Vendor Specific – Mfg pin[3]
P23	Vendor	Vendor Specific – Mfg pin[3]
P24	GND	

NOTE:
1. The 5 V supply voltage pins are included to meet future product requirements. Future revisions of this specification may require 5 V supply voltage be provided.
2. ~~The corresponding pin to be mated with Pin8 shall always be grounded~~. For specific optional usage of Pin8 see section ~~6.4~~ 6.7 ~~Serial ATA Revision 3.0 spec~~.
3. No connect on the host side.
4. For specific optional usage of pin P21 see section 6.7.

3.3.4 [editor's note: 6.7] ~~Power Segment Pin P11 Definition~~ Hardware Feature Control (Optional)

3.3.4.1 [editors note: 6.7.new1] Overview

Prior to processing a SET FEATURES XXX subcommand, the Hardware Feature Control operates using the default behavior in section 6.7.new1.1. Otherwise the Hardware Feature Control operates using the extended behavior in section 6.7.new1.2.

3.3.4.1.1 [editors note: 6.7.new1.1, previously 6.7] Default Behavior

There are two hardware control features listed as:

A. disable staggered spin-up (DSS)
B. Device activity signal (e.g. LED) (DAS)

Due to various hardware issues, these features are mapped onto different physical pins depending on the connecter type as indicated in Table 1 below. Not all features are defined for all connecter types.

Table 2 - DSS and DAS for various connectors

Standard Connector (3.5" & 2.5")	1.8" mSATA Connector	LIF-SATA Connector
Pin 11: • DSS • DAS	Pin 7: • DAS	Pin 8: • DSS • DAS

The Hardware Feature Control, (i.e. pins P11, P7, or P8 depending upon connector)~~Pin P11 of the power segment of the device connector~~ may be used by the device to provide the host with an activity indication and it may be used by the host to indicate whether staggered spin-up should be used. To accomplish both of these goals, the Hardware Feature Control ~~pin P11~~ acts as an input from the host to the device prior to PHYRDY for staggered spin-up control and then acts as an output from the device to the host after PHYRDY for activity indication. The activity indication provided ~~by pin P11~~ is primarily for use in backplane applications. Reference section 13.14 for information on activity LED generation for desktop applications.

A device may optionally support activity indication ~~via pin P11~~, staggered spin-up control ~~via pin P11~~, or both features. If neither feature is supported, then pin P11, P7, or P8 depending upon connector~~pin P11~~ is a no-connect at the device as specified in Table 3.

A host may only support one ~~pin P11~~ feature, either receiving activity indication or staggered spin-up disable control. If a host supports receiving activity indication ~~via pin P11~~, then the host shall not use pin P11, P7, or P8 depending upon connector~~pin P11~~ to disable staggered spin-up. If a host does not support receiving activity indication ~~via pin P11~~, then the host may use pin P11, P7, or P8 depending upon connector~~pin P11~~ to disable staggered spin-up.

3.3.4.2 [editors note: 6.7.new1.2] Extended Behavior

Hardware Feature Control may be used by the device for one of the following:

a. Default use of the hardware feature control [editors note: (see section 6.7.new1.1)];
b. Direct Head Unload (DHU) (see 6.new and 13.x); or

c. vendor specific use (see 13.new).

[editors note: renumber old 6.7.1 to new 6.7.2 and renumber old 6.7.2 to new 6.7.3]

3.3.5 [editors note: 6.new] Electrical Requirements Specification

Table XX – Direct Head Unload electrical requirements

Parameter	Min Value	Max Value	Description & Conditions
$V_{DHUactive}$	1.8V	2.1 V	Host voltage presented to device to load the heads onto the ramp and keep them there. Value specified for all allowable I_{DInact} leakage currents.
$V_{DHUnegate}$	-0.1 V	225 mV	Host voltage presented to device to clear the state of the DHU. The timing to load the heads onto the media is vender specific. Value specified for all allowable I_{DInact} leakage currents.

[editors note: add section 13.new to Clause 13. Change the mV scale to V.]

3.4 [editors note: 13.new] Hardware Feature Control (optional)

In Serial ATA Revision 3.0 and previous specifications, Hardware Feature Control is defined only for these uses:

a) Disable Staggered Spin-up (i.e., DSS) (see 6.7.2 and 13.10); and

b) Activity indication LED (i.e., Device Activity Signal - DAS) (see 6.7.1 and 13.14).

Table 3 specifies the pins used by Hardware Feature Control for various connectors

Table 3 - Pins used by Hardware Feature Control

Standard Connector (3.5" & 2.5")	1.8" mSATA Connector[1]	LIF-SATA Connector
Pin P11: • DSS • DAS • DHU • (other vendor specific)	Pin P7: • DAS (added after SATA 3.0) • DHU • (other vendor specific)	Pin P8: • DSS • DAS • (other vendor specific) Pin P21: • DHU
[1] DSS is not defined for 1.8" mSATA Connector.		

If Hardware Feature Control is supported, then:

a) IDENTIFY DEVICE data word TBDid1 bit TBDS (i.e., see 13.2.1.x) shall be set to one;

b) the SET FEATURES Select Hardware Feature Control subcommand shall be supported (see 13.3.new);

c) page TBDpage of the Identify Data log (see 13.7.new) shall be supported;

d) on processing a power on reset, then:

   A. IDENTIFY DEVICE data word TBDid2 bit TBDE (see 13.2.1.y) shall be cleared to zero;

   B. the Current Hardware Feature Control Identifier in the Identify Data log shall be cleared to zero; and

   C. the Supported Hardware Feature Control Identifier in the Identify Data log shall be cleared to zero; and

   D. See 6.7.new1.1 for requirements of the hardware feature control pin(s); and

e) after processing a SET FEATURES Enable Hardware Feature Control subcommand with no error, then:

   A. IDENTIFY DEVICE data word TBDid2 bit TBDE (see 13.2.1.y) shall be set to one;

   B. the Current Hardware Feature Control Identifier in the Identify Data log shall be non-zero;

   C. the Supported Hardware Feature Control Identifier in the Identify Data log shall be non-zero; and

   D. the behavior of the Hardware Feature Control is specified by the SET FEATURES Enable Hardware Feature Control subcommand.

If Hardware Feature Control is not supported, then:

a) IDENTIFY DEVICE data word TBDid1 bit TBDS (see 13.2.1.x) shall be cleared to zero;

b) IDENTIFY DEVICE data word TBDid2 bit TBDE (see 13.2.1.y) shall be cleared to zero;

c) the SET FEATURES Select Hardware Feature Control subcommand shall not be supported (see TBD);

d) the Supported Hardware Feature Control Identifier (see 13.7.new) in the Identify Data log shall be cleared to zero;

e) the Current Hardware Feature Control Identifier (see 13.7.new) in the Identify Data log shall be cleared to zero; and

f) See 6.7.new1.1 for requirements of the hardware feature control pin(s).

[editors note: modify Table 75 "IDENTIFY DEVICE information"]

3.4.1 [editor's note: 13.2.1] IDENTIFY DEVICE

Table 4 – IDENTIFY DEVICE information

Word	O/M	F/V		
TBDid1	O	F	bit	Hardware Feature Control is supported
			TBDS	[Editors note: suggest using Word 78, bit 5]
TBDid2	O	V	bit	Hardware Feature Control is enabled
			TBDE	[Editors note: suggest using Word 79, bit 5]

[editors note: modify sections "13.2.1.x and 13.2.1.y in IDENTIFY DEVICE"]

3.4.1.1 [editors note: 13.2.1.x] Word TBDid1:

If bit TBDS is set to one, then Hardware Feature Control is supported (see 13.new). If bit TBDS is cleared to zero, then Hardware Feature Control is not supported and IDENTIFY DEVICE data word TBDid2 bit TBDE shall be cleared to zero.

3.4.1.2 [editors note: 13.2.1.y] Word TBDid2:

If bit TBDE is set to one, then Hardware Feature Control is enabled (see 13.new). If bit TBDE is cleared to zero, then Hardware Feature Control is disabled.

[editors note: modify section "13.3 SET FEATURES", table 79]

3.5 [editors note: 13.3] SET FEATURES

Table 5 - Feature identification values

Count(7:0) Value	Description
00h	Reserved
01h	Non-zero buffer offset in DMA Setup FIS
02h	DMA Setup FIS Auto-Activate optimization
03h	Device-initiated interface power state transitions
04h	Guaranteed In-Order Data Delivery
05h	Asynchronous Notification
06h	Software Settings Preservation
07h	Device Automatic Partial to Slumber transitions
08h (TBD)	Enable Hardware Feature Control
~~08h~~09h - FFh	Reserved

[editors note: 13.3.new] Enable Hardware Feature Control

See [editors note: 13.new] for additional information about Hardware Feature Control.

This function enables Hardware Feature Control. Hardware Feature Control shall be disabled by power-on reset.

Count(7:0) is reserved.

LBA(15:0) contains a function identifier (see Table 6).

Table 6 -Hardware Feature Control Pin Definitions

LBA(15:0)	**Description**	**Preserved Across Software Reset**	**Preserved Across COMRESET**
0000h	Reserved	NA	NA
0001h	Direct Head Unload (DHU) (see 13.X DHU)	Y	Yes, regardless of SSP setting.
0002h to EFFFh	Reserved	NA	NA
F000h to FFFFh	Vendor specific	Vendor specific	Vendor specific

On successful completion of this command:

a) Current Hardware Feature Control Identifier (see 13.7.new.1.1) shall be set to the value in LBA(15:0);
b) IDENTIFY DEVICE word TBDid2, bit TBDE shall be set to one; and
c) the behavior of Hardware Feature Control is specified by Table 3.

The device shall return command aborted if:

a) IDENTIFY DEVICE data word TBDid1 bit TBDS is cleared to zero;
b) the value in LBA(15:0) is not equal to the Supported Hardware Feature Control Identifier (see 13.7.new.1.2); or
c) the Current Hardware Feature Control Identifier (see 13.7.new.1.1) is non-zero.

[editors note: add this to section "13.7 SATA Logs"]

[editors note: T13 is on the verge of approving e08156 to create the Identify Data log for ACS-2. This allows for almost unlimited expansion of IDENTIFY DEVICE fields.]

3.6 [editor's note: 13.7.new] Identify Data Log (TBDlogh)

Table 7 – Identify Data log (log TBDlog, page TBDpage)

Byte	O/M	F/V	
TBDlg1.. TBDlg2	O	V	Current Hardware Feature Control Identifier (Word)
TBDlg3.. TBDlg4	O	F	Supported Hardware Feature Control Identifier (Word)

13.7.new.1 Serial ATA Settings (page TBDpage)

13.7.new.1.1 Byte TBDlg1..TBDlg2 - Current Hardware Feature Control Identifier

If the Current Hardware Feature Control Identifier is non-zero, then Table 6 describes the current Hardware Feature Control behavior. If the Current Hardware Feature Control Identifier is cleared to zero, then the current Hardware Feature Control behavior shall be either disable staggered spin-up (DSS) or HDD activity indication (DAS).

13.7.new.1.2 Byte TBDlg3..TBDlg4 - Supported Hardware Feature Control Identifier

The Supported Hardware Feature Control Identifier (see Table 6) indicates the value that is permitted for the Current Hardware Feature Control Identifier field.

[editors note: add new section 13.x to clause 13]

3.7 [editors note: 13.new] DHU Specific Operation Specification (optional)

The optional DHU feature of Hardware Feature Control provides a method for the host to cause a device that has movable read/write heads to move them to a safe position.

DHU is an active high signal driven by the host. See [editors note: 6.new] for electrical requirements for DHU.

If $V_{DHUactive}$ condition (See 6.X) is met, then:

a) the device shall stop read look-ahead if that operation is in process;
b) the device shall stop writing cached data to the media if that operation is in process;
c) if the device has a write buffer, then the device shall retain data in the write buffer;
d) the device shall put itself in a state that minimizes or prevents damage due to a high-G event, (e.g. if a device implements unloading its head(s) onto a ramp, then the device shall retract the head(s) onto the ramp; and if a device implements parking its head(s) in a landing zone on the media, then the device shall park its head(s) in the landing zone).

If VDHUnegate condition (See 6.X) is met, then the device shall perform normal operations.

