**Proposed Draft**

**Serial ATA International Organization**

**Version 7**
**April 6, 2011**

# Serial ATA Technical Proposal # TPR_C106
# Title : SATA Universal Storage Module

## Author Information

| Author Name | Company | Email address |
|---|---|---|
| Alvin Cox | Seagate Technology | alvin.cox@seagate.com |

## Workgroup Chair Information

| Workgroup (Phy, Digital, etc…) | Chairperson Name | Email address |
|---|---|---|
| CABCON | Frank Chu | Frank.Chu@hitachigst.com |
| PHY | Charles Hill | cphill@altaeng.com |

### Document History

| Version | Date | Comments |
|---|---|---|
| 0 | October 22, 2010 | Initial release. |
| 1 | December 16, 2010 | Added Direct connect host concept and initial work defining electrical requirements. Incorporated editorial changes from Harvey Newman. |
| 2 | March 8, 2011 | Completed additions to electrical requirements and added figures for form factor and connectors. Extensive editorial changes. |
| 3 | March 9, 2011 | Updated datum designations on section A-A, removed "e" from exceptions list on page 9 and moved "and" to the correct location. |
| 4 | March 28, 2011 | Corrected section 4.2.6 title and revised text to differentiate the full set of electrical requirement tables for Direct Connect Host, added TX AC common mode voltage and OOB requirements to Table bbb, added section number for host connector to Table 2 and removed note regarding inf-8280 from Table 2, added Table xxx instead of including the dimension table as part of Figure ccc. |
| 5 | March 29, 2011 | Table ccc : Removed "and after CIC" and added 7.4.12 to common mode voltage cross-reference. Added Table 39 to applicable list for Direct Connect host in section 7.2 wording. |
| 6 | April 1, 2011 | Updated the usage model and added definitions for Host Direct and GenHD's. Changed "Direct Connect Host" to "Host Direct". Removed return loss tables from Host Direct requirements. Added Gen1HD, Gen2HD, and Gen3HD as applicable. Resolved conflicts to defing Gen1m as AC coupled. Fixed various editorial issues in the phy section. |
| 7 | April 6, 2011 | Minor editorial corrections and dropped change to 7.2.2.5.4 since it is not affected. Change Host Direct to UHost and GenHD's to Genu's. Changed measurement interval to .45-.55 UI for Gen3u. Changed jitter requirements in Tables bbb and ccc. |
| | | |

## Introduction

This proposal defines the interface characteristics of the SATA Universal Storage Module (SATA USM). The SATA USM provides a new standard usage model for portable storage device using the SATA interface. It includes a standard SATA drive in a special enclosure that may be inserted into a host slot specifically designed to accept the SATA USM. Although the drive may be tested outside of the enclosure for certification as a standard endpoint device, the current specification does not provide a means for describing the electrical characteristics of a host that only has a compliance point at the endpoint device. This proposal defines the usage model and special test requirements for the SATA USM host in a generic format that may be used for other UHost applications.

# 1 Technical Specification Changes

The following additions are based on the content of Serial ATA Revision 3.1RC, Clean DRAFT 2010_09_29. Changes include additions to Table 2, a new usage model, a new lab test load, and a new lab-sourced signal. Although not blue and underlined, all figures added below are new and in the same format as the source document for Serial ATA Revision 3.1RC.

Add to definitions:

**Gen1u**

The electrical specifications defined at 1.5 Gbps for UHost applications. Because a Gen1i/Gen2i/Gen3i endpoint device is attached directly to the mating connection of the UHost, the electrical specifications for Gen1u allow a channel loss up to the approximate equivalence of a 1 meter data cable plus mated connector pair within the UHost.

**Gen2u**

The electrical specifications defined at 3.0 Gbps for UHost applications. Because a Gen1i/Gen2i/Gen3i endpoint device is attached directly to the mating connection of the UHost, the electrical specifications for Gen2u allow a channel loss up to the approximate equivalence of a 1 meter data cable plus mated connector pair within the UHost.

**Gen3u**

The electrical specifications defined at 6.0 Gbps for UHost applications. Because a Gen1i/Gen2i/Gen3i endpoint device is attached directly to the mating connection of the UHost, the electrical specifications for Gen3u allow a channel loss up to the approximate equivalence of the Gen3i CIC (see 7.2.7) plus mated connector pair within the UHost.

**UHost**

A SATA host that provides for attachment of a Gen1i/Gen2i/Gen3i endpoint device directly to the mating connection of the UHost. The UHost may include a channel loss up to the approximate equivalent of the 1 meter cable plus mated connector pair or the Gen3i CIC (see 7.2.7) plus mated connector pair. The UHost does not support the attachment of additional interconnections between the UHost mating connection and the endpoint device connection. See Section 5.2 and Table 2 for usage model applicability.

## 5.2 Usage Models

**5.2.x SATA Universal Storage Module (SATA USM)**

In this application, a Gen1i/Gen2i/Gen3i device is mounted in an enclosure that provides the mechanism for the device to be inserted into or removed from a system accepting a SATA USM device. Compliance points are only defined at the SATA USM device mated connector pair. All electrical specifications at this compliance point shall meet Gen1i/Gen2i/Gen3i specifications for the drive and Gen1u/2u/3u specifications for the host. The signaling at the host controller may exceed the Gen1i/Gen2i/Gen3i transmit maximum providing the Gen1i/Gen2i/Gen3i receiver maximum is not exceeded at the SATA USM device connector. The host and the device shall comply with the electrical hot plug specification described in section 7.2.5. The SATA USM device may be tested for compliance with or without the SATA USM device enclosure. See INF-8280 (available at www.sffcommittee.org) for the SATA USM mechanical, power, and EMC requirements and recommendations. The SATA USM host shall be tested for compliance as a UHost.

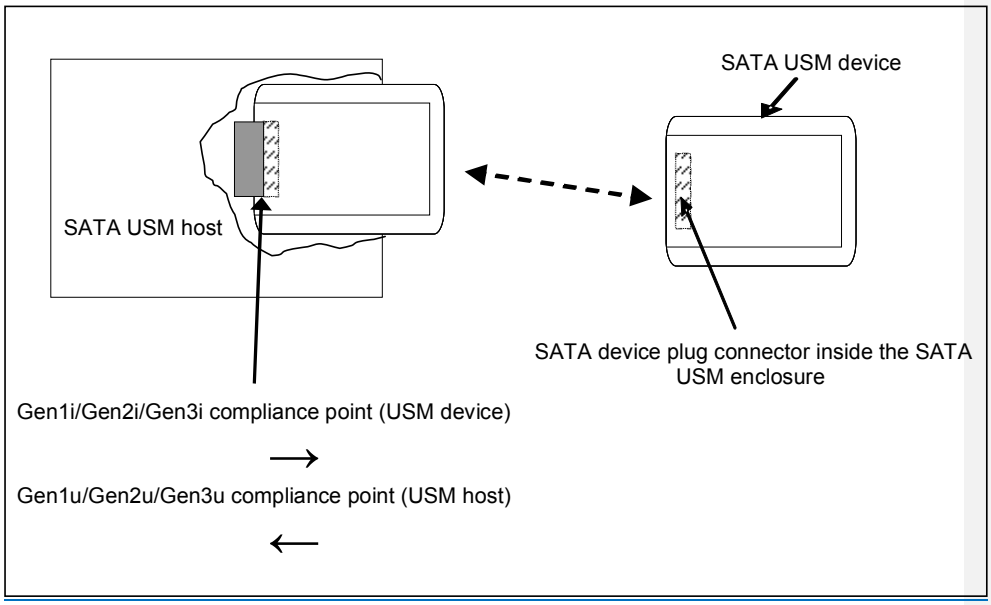


**Figure xy –SATA USM Application**

**Table 2 – Usage Model Descriptions**

| Characteristic | Internal 1 meter Cabled Host to Device | Short Backplane to Device | Internal 4-lane Cabled Disk Arrays | System to System Inter connects – Data Center Applications xSATA | System to System Inter connects – External Desktop Applications eSATA | Proprietary Serial ATA Disk Arrays | Serial ATA and SAS | LIF-SATA | mSATA | SATA USM |
|---|---|---|---|---|---|---|---|---|---|---|
| Use model section number | 5.2.1 | 5.2.2 | 5.2.4 | 5.2.5 | 5.2.6 | 5.2.7 | 5.2.8 | 5.2.10 | 5.2.10 | 5.2.x |
| Cable and/or backplane type | Int SL | BP | Int ML | Ext ML | Ext SL | BP and cable | BP | P | BP | P |
| Cable length | <= 1 m | | <= 1 m | <= 2 m | <= 2 m | | | P | | P |
| Cable Electrical | Table 19 | P | Table 19 | Table 21 | Table 20 | Table 19 | P | Table 19 | P | P |
| Attenuation at 4.5GHz | -6dB | P | -6dB | -8dB | -8dB | -6dB | P | -6dB | P | P |
| Host-side connector | 6.1.5 | P | 6.1.11 or 6.1.12 | 6.3.3 (key 7) | 6.6.1 | 6.1.5 or P | SAS | 6.4.3 | 6.5.2 | 6.6.1 |
| Device-side connector | 6.1.3.1 | 6.1.3.1 | 6.1.3.1 | 6.6.3 (key 7) | 6.6.1 | 6.1.3.1 | 6.1.3.1 | 6.4.2 | 6.5.3.1 | 6.1.3.1 |
| Gen1i 1.5 Gbps | R | D (host to provide received signal) | R | NS | NS | R | D | R | R | D |
| Gen1m 1.5 Gbps | NS | H | NS | R (key 7) | R | NS | NS | NS | NS | NS |
| Gen1u 1.5 Gbps | NS | NS | NS | NS | NS | NS | NS | NS | NS | H |

| Characteristic | Internal 1 meter Cabled Host to Device | Short Backplane to Device | Internal 4-lane Cabled Disk Arrays | System to System Inter connects – Data Center Applications xSATA | System to System Inter connects – External Desktop Applications eSATA | Proprietary Serial ATA Disk Arrays | Serial ATA and SAS | LIF-SATA | mSATA | SATA USM |
|---|---|---|---|---|---|---|---|---|---|---|
| Gen2i 3.0 Gbps | FS | D (host to provide received signal) | FS | NS | NS | FS | D | FS | FS | D |
| Gen2m 3.0 Gbps | NS | H | NS | FS (key 7) | FS | NS | NS | NS | NS | NS |
| Gen2u 3.0 Gbps | NS | NS | NS | NS | NS | NS | NS | NS | NS | H |
| Gen3i 6.0 Gbps | FS | NS | FS | NS | NS | FS | D | FS | NS | D |
| Gen3u 6.0 Gbps | NS | NS | NS | NS | NS | NS | NS | NS | NS | H |
| Hot plug support | NS | R | NS | R | R | R | R | NS | NS | R |

Key:
R – Required : configuration requires appropriate capabilities
FS – Feature specific : configuration is supported by specification but may be tied to an optional capability
NOTE: Feature specific is intended to indicate that Gen1 is required but higher data rates are optional.
NS – Not supported : configuration is not supported by definition in specification
P – Proprietary : implementation is vendor specific and not defined in specification
H – Host
D – Device
SL – single lane
ML – multi-lane
Int – Internal
Ext – External
BP – Backplane
NOTE : Many of the references in the table are section numbers or notations of clarification which do not require Key values

## SATA USM Connector location

The SATA USM connector location is defined to facilitate blind mating. Figure ccc and Table xxx show the connector location on the SATA USM device. The Serial ATA connector is located inside the SATA USM housing as indicated. See INF-8280 (available at www.sffcommittee.org) for additional details regarding the SATA USM.

Field Code Changed

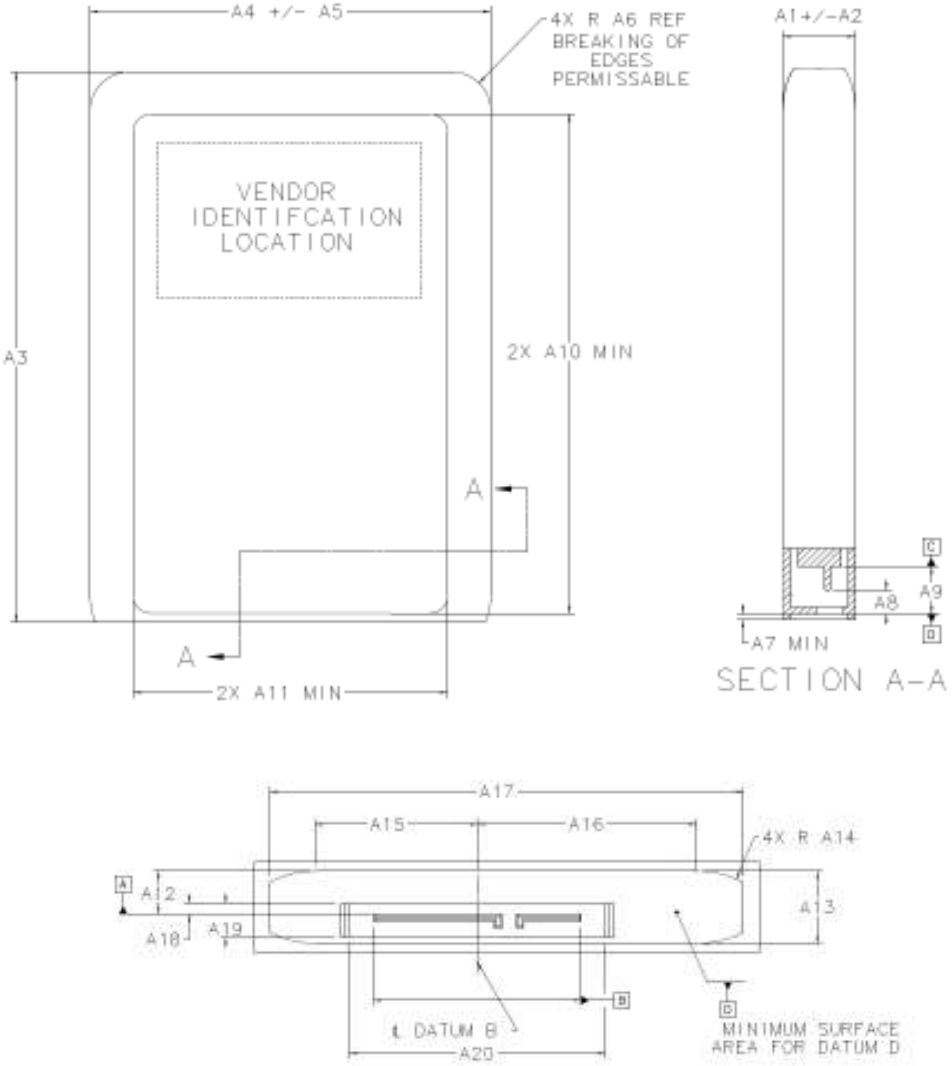


**Figure ccc –SATA USM physical dimensions**

**(See INF-8280)**

| mm | inch | Dimension |
|---|---|---|
| 14.50 | 0.571 | A1 |
| 0.20 | 0.008 | A2 |
| 111.68 | 4.397 | A3 |
| 44.04 | 1.734 | A4 |
| 0.20 | 0.008 | A5 |
| 8.00 | 0.315 | A6 |
| 1.14 | 0.045 | A7 |
| 4.80 | 0.189 | A8 |
| 9.70 | 0.382 | A9 |
| 88.90 | 3.500 | A10 |
| 50.80 | 2.000 | A11 |
| 6.86 | 0.270 | A12 |
| 11.53 | 0.454 | A13 |
| 16.00 | 0.630 | A14 |
| 26.04 | 1.025 | A15 |
| 35.20 | 1.386 | A16 |
| 76.02 | 2.993 | A17 |
| 1.68 | 0.066 | A18 |
| 5.46 | 0.215 | A19 |
| 41.05 | 1.616 | A20 |

**Table xxx –SATA USM physical dimensions**

**(See INF-8280)**

## USM mating interfaces

The USM device uses the device plug connector defined in section 6.1.3.1. The SATA Universal Storage Module receiver uses a custom SATA receptacle connector to properly attach to the module. The connectors shall be capable of a minimum of 1,500 insertion/removal cycles. The SATA USM receptacle connector is available in vertical and horizontal PCB mounting configurations as shown in Figure ddd and Figure eee, respectively. The receptacle connector mating area is compliant with the backplane connector defined in section 6.1.6 with the following four exceptions:

a) side mounted retention springs to improve the connector retention (optional);
b) anti-wiggle bumps to reduce cable deflection (optional);
c) two alignment ribs on each of the long outside surfaces (required); and
d) extended reach/length to properly attach the SATA universal storage module (required).

For hot plug implementation, it should be noted that the side mounted retention springs are optional and that the only contacts present are the power and signal pins defined in Table 3.

See INF-8280 for USM receptacle connector details.

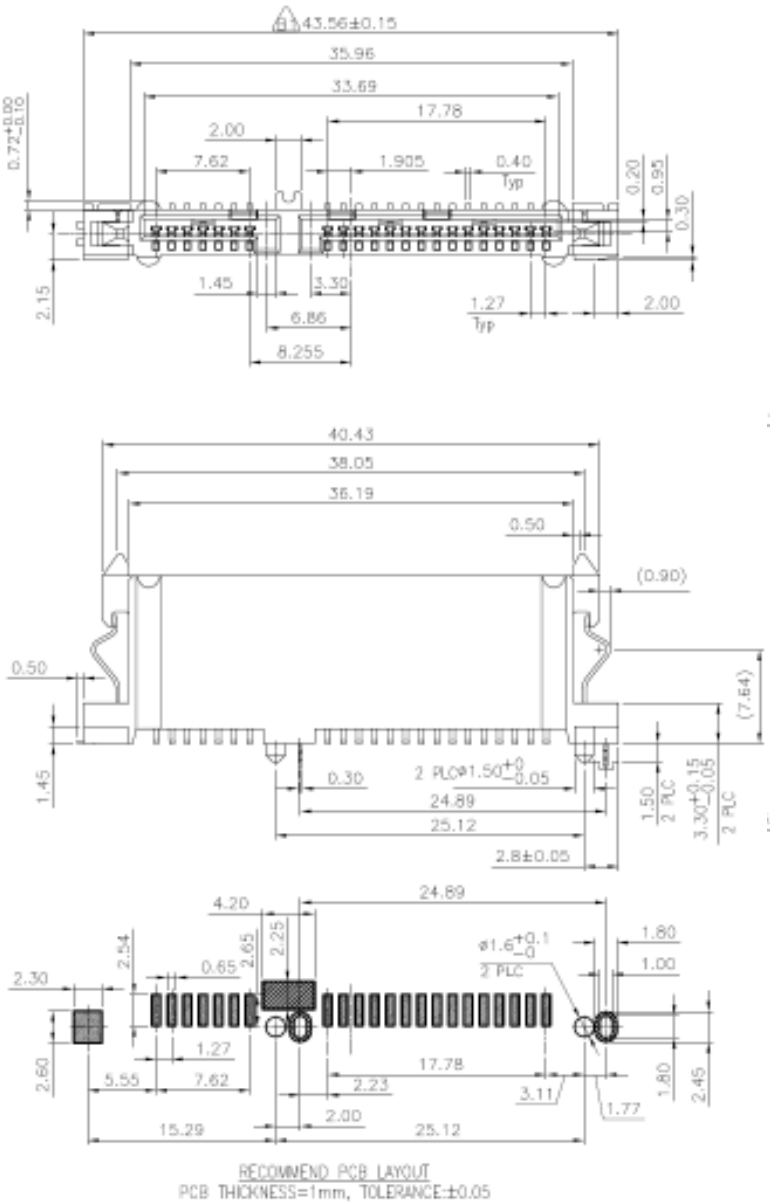


**Figure ccc –SATA USM vertical receptacle**
**(See INF-8280)**

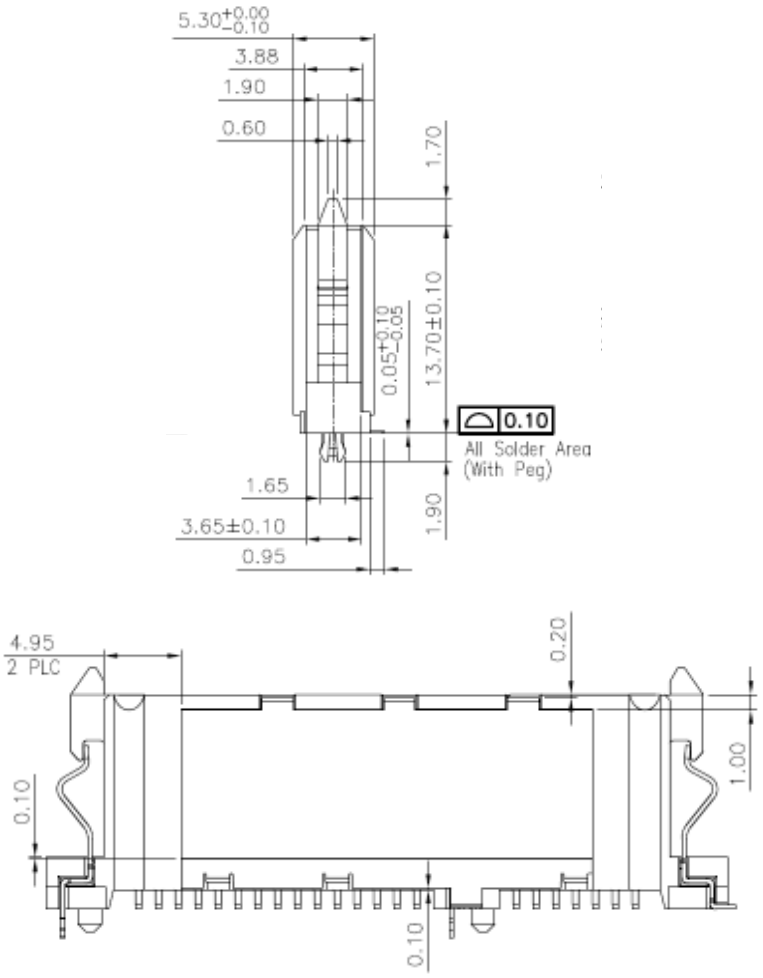


**Figure ccc (continued) –SATA USM vertical receptacle**
**(See INF-8280)**

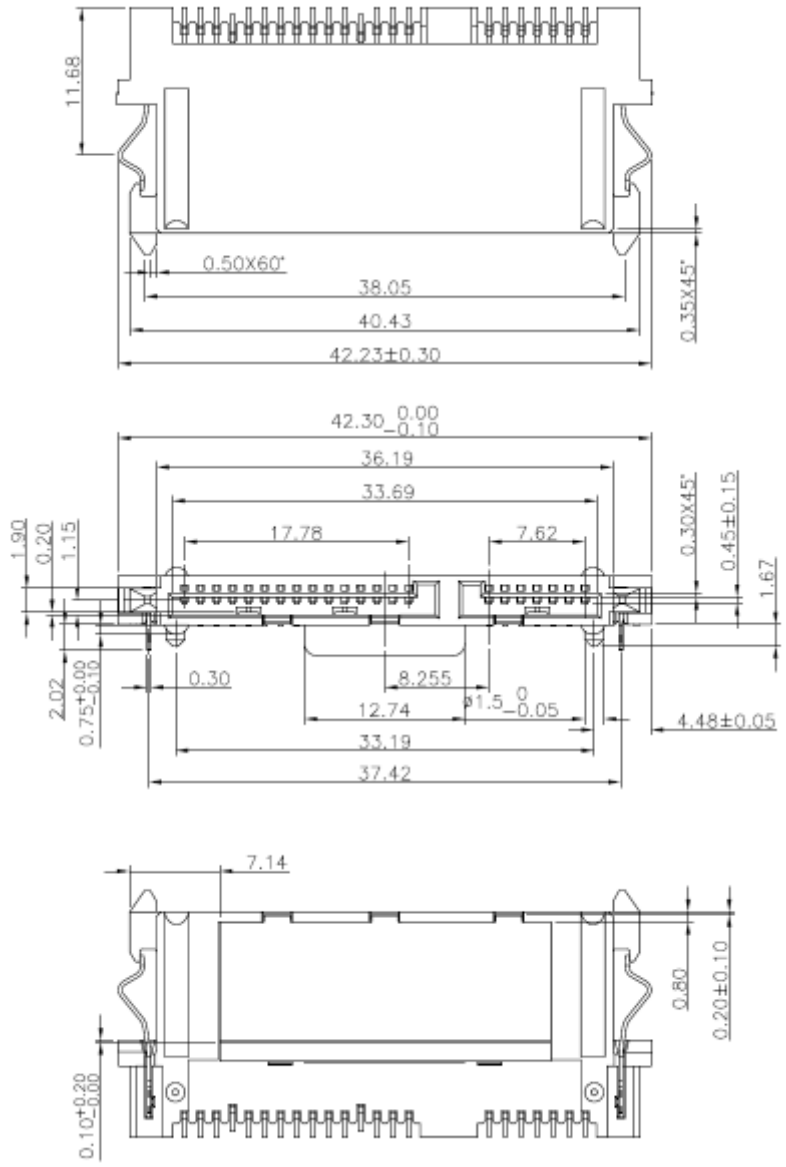


**Figure ddd –SATA USM horizontal receptacle**
**(See INF-8280)**

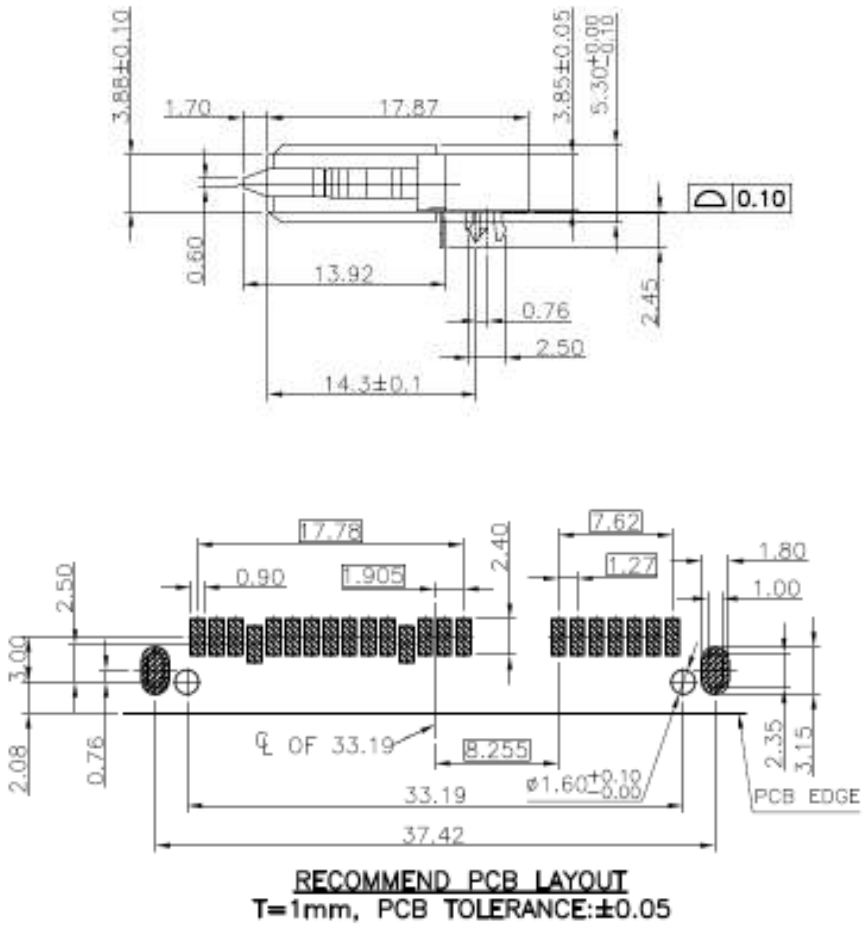


Figure ddd (continued)–SATA USM horizontal receptacle
(See INF- 8280)

**Table 34 – General Specifications**

| Parameters | Units | Limit | Electrical Specification | | | | | | | | Detail Cross-Ref Section | Measurement Cross-Ref Section |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Gen1i | Gen1m | Gen1u | Gen2i | Gen2m | Gen2u | Gen3i | Gen3u | | |
| Channel Speed | Gbps | Nom | 1.5 | | | 3.0 | | | 6.0 | | 7.2.2.1.1 | - |
| Fbaud | GHz | Nom | 1.5 | | | 3.0 | | | 6.0 | | - | - |
| FER, Frame Error Rate | | Max | 8.2e-8 at 95% confidence level | | | 8.2e-8 at 95% confidence level | | | 8.2e-8 at 95% confidence level | | 7.2.2.1.2 | 7.4.1 |
| $T_{UI,}$ Unit Interval | ps | Min | 666.4333 | | | 333.2167 | | | 166.6083 | | 7.2.2.1.3 | 7.4.14 |
| | | Nom | 666.6667 | | | 333.3333 | | | 166.6667 | | | |
| | | Max | 670.2333 | | | 335.1167 | | | 167.5583 | | | |
| $f_{tol}$, TX Frequency Long Term Accuracy | ppm of Fbaud | Min | -350 | | | -350 | | | -350 | | 7.2.2.1.4 | 7.4.7 |
| | | Max | +350 | | | +350 | | | +350 | | | |
| $f_{SSC}$, Spread-Spectrum Modulation Frequency | kHz | Min | 30 | | | 30 | | | 30 | | 7.2.2.1.5 7.3.3 | 7.4.14 |
| | | Max | 33 | | | 33 | | | 33 | | | |
| $SSC_{tol}$, Spread-Spectrum Modulation Deviation | ppm of Fbaud | Min | -5350 | | | -5350 | | | -5350 | | 7.2.2.1.6 7.3.3 | 7.4.14 |
| | | Max | +350 | | | +350 | | | +350 | | | |

| Parameters | Units | Limit | Electrical Specification | | | | | | | | Detail Cross-Ref Section | Measurement Cross-Ref Section |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Gen1i | Gen1m | Gen1u | Gen2i | Gen2m | Gen2u | Gen3i | Gen3u | | |
| $SSC_{tol}$, Spread-Spectrum Modulation Rate | ppm/ usec | Max | 1250 | | | 1250 | | | - | | 7.2.2.1.6 7.3.3 | 7.4.14 |
| $V_{cm,dc}$, DC Coupled Common Mode Voltage | mV | Min | 200 | (AC only) | | (AC only) | | | (AC only) | | 7.2.2.1.7 | 7.4.14 |
| | | Nom | 250 | (AC only) | | (AC only) | | | (AC only) | | | |
| | | Max | 450 | (AC only) | | (AC only) | | | (AC only) | | | |
| $V_{cm,ac\ coupled}$, AC Coupled Common Mode Voltage | mV | Min | 0 | | - | - | | | - | | 7.2.2.1.8 | 7.4.29 |
| | | Max | 2000 | | - | - | | | - | | | |
| $Z_{diff}$, Nominal Differential Impedance | Ohm | Nom | 100 | | | - | | | 100 | | 7.2.2.1.9 | 7.4.26 |
| $C_{ac\ coupling}$ AC Coupling Capacitance | nF | Max | 12 | | | 12 | | | 12 | | 7.2.2.1.10 | 7.4.17 |
| $t_{settle,cm}$, Common Mode Transient Settle Time | ns | Max | 10 | | | - | | | - | | 7.2.2.2.14 | 7.2.5.3 |
| $V_{trans}$, Sequencing Transient Voltage | V | Min | -2.0 | | | -2.0 | | | -2.0 | | 7.2.2.1.11 | 7.4.16 |

**Table bbb - UHost Transmitted Signal Requirements**

| Parameter [1] | Units | Limit | Electrical Specification | | | Detail Cross-Ref Section [2,3] | Measurement Cross-Ref Section [2,3] |
|---|---|---|---|---|---|---|---|
| | | | Gen1u | Gen2u | Gen3u [3] | | |
| $V_{diffTX}$, TX Differential Output Voltage | | Min | 325 | 275 | - | 7.2.2.2.7 | 7.4.5 |
| | mVppd | Min | - | - | 200 | | |
| | | Nom | 400 | - | - | | |
| | | Max | 600 | 750 | - | | |
| | | Max | - | - | 900 | | |
| $t_{20\text{-}80TX}$, TX Rise/Fall Time | ps (UI) | Min 20-80% | 100 (.15) | 67 (.20) | 33 (0.20) | 7.2.2.2.10 | 7.4.4 |
| $UI_{VminTX}$, TX Minimum Voltage Measurement Interval | UI | | 0.45-0.55 | 0.45-0.55 | 0.45-0.55 | 7.2.2.2.9 | 7.4.5 |
| $t_{skewTX}$, TX Differential Skew | ps | Max | - | 50 | 30 | 7.2.2.2.11 | 7.4.15 |
| Vcm,acTX, TX AC Common Mode Voltage | mVp-p | Max | 100 | 100 | 100 | 7.2.2.2.12 7.2.2.2.13 | 7.4.20 7.4.21 |
| $V_{trans}$, Sequencing Transient Voltage LL | V | Min | - | - | -1.2 | 7.2.2.1.12 | 7.4.30 |
| | | Max | - | - | 1.2 | | |
| $Z_{diffTX}$, TX Pair Differential Impedance | Ohm | Min | 85 | - | - | 7.2.2.2.1 | 7.4.26 |
| | | Max | 115 | - | - | | |

| Parameter [1] | Units | Limit | Electrical Specification | | | Detail Cross-Ref Section [2,3] | Measurement Cross-Ref Section [2,3] |
|---|---|---|---|---|---|---|---|
| | | | Gen1u | Gen2u | Gen3u [3] | | |
| $Z_{S-eTX+}$, TX Single-Ended Impedance | Ohm | Min | 40 | - | - | 7.2.2.2.2 | 7.4.27 |
| DVdiffOOB, OOB Differential Delta | mV | Max | - | 25 | 25 | 7.2.2.2.15 | 7.4.23 |
| DVcmOOB, OOB Common Mode Delta | mV | Max | - | 50 | 50 | 7.2.2.2.16 | 7.4.22 |
| TJ at Connector, Clk-Data, $f_{BAUD}/500$ JTF Defined | UI | Max | 0.52 | 0.52 | - | 7.2.2.2.19 7.3 | 7.4.8 7.4.9 |
| DJ at Connector, Clk-Data, $f_{BAUD}/500$ JTF Defined | UI | Max | 0.34 | 0.34 | - | | |
| TJ ($10^{-12}$) without CIC, Clk-Data JTF Defined | UI | Max | - | - | 0.52 | 7.2.2.2.19 7.3 | 7.4.8 7.4.10 |
| TJ ($10^{-6}$) without CIC, Clk-Data JTF Defined | UI | Max | - | - | 0.46 | | |

1. The UHost TX requirements are defined at the target device attachment point and the UHost channel loss is not separable from the host transmitter.
2. Referenced detail and measurement sections may indicate a different connection type in the figures than what applies to the specific unit under test. Many figures are based on the Internal 1 meter Cabled Host to Device usage model. Specific connection type may vary, depending on the type UHost under test.
3. Gen3u measurements are made only with the Lab Load and are not made using the Gen3i CIC.

**Table ccc – Lab-Sourced Signal (for UHost Receiver Tolerance Testing)**

| Parameter | Units | Limit | Electrical Specification | | | Detail Cross-Ref Section[1] | Measurement Cross-Ref Section[1] |
|---|---|---|---|---|---|---|---|
| | | | Gen1u | Gen2u | Gen3u | | |
| $V_{diffRX,}$ RX Differential Input Voltage [2] | mVppd | Min | 400 | 400 | - | 7.2.2.5.3 | 7.4.6 |
| | | Min | - | - | 240 | | |
| | | Max | 600 | 700 | - | | |
| | | Max | - | - | 1000 | | |
| $t_{20\text{-}80RX,}$ RX Rise/Fall Time | ps (UI) | Min 20-80% | 100 (.15) | 67 (.20) | 33 (0.20) | 7.2.2.2.10 | 7.4.4 |
| | | Max 20-80% | 273 (.41) | 136 (.41) | 68 (0.41) | | |
| $UI_{VminRX,}$ RX Minimum Voltage Measurement Interval | UI | | 0.45-0.55 | 0.45-0.55 | - | 7.2.2.5.5 | 7.4.6 |
| | | | - | - | 0.45-0.55 | | 7.4.3.2 |
| $t_{skewRX,}$ RX Differential Skew | ps | Max | - | 20 | 20 | 7.2.2.5.6 | 7.4.15 |
| $V_{cm,acRX,}$ RX AC Common Mode Voltage | mVp-p | Max | 50 | 50 | 50 | 7.2.2.5.7 | 7.4.11 7.4.12 |
| $f_{cm,acRX,}$ AC Common Mode Frequency | MHz | Min | 2 | 2 | 2 | 7.2.2.5.8 | 7.4.11 |
| | | Max | 200 | 200 | 200 | | |
| $Z_{diffRX,}$ RX Pair Differential Impedance | Ohm | Min | 85 | - | - | 7.2.2.3.1 | 7.4.26 |
| | | Max | 115 | - | - | | |
| $Z_{s\text{-}eRX,}$ RX Single-Ended Impedance | Ohm | Min | 40 | - | - | 7.2.2.3.2 | 7.4.27 |

| Parameter | Units | Limit | Electrical Specification | | | Detail Cross-Ref Section[1] | Measurement Cross-Ref Section[1] |
|---|---|---|---|---|---|---|---|
| | | | Gen1u | Gen2u | Gen3u | | |
| TJ at Connector, Clk-Data, $f_{BAUD}/500$ JTF Defined | UI | Max | 0.45 | 0.45 | - | 7.2.2.5.9 7.3 | 7.4.8 7.4.11 |
| DJ at Connector, Clk-Data, $f_{BAUD}/500$ JTF Defined | UI | Max | 0.27 | 0.27 | - | | |
| TJ Clk-Data JTF Defined | UI | Max | - | - | 0.60 | 7.2.2.5.10 7.3 | 7.4.8 7.4.12 |
| RJ, MFTP Clk-Data JTF Defined | UI | Max | - | - | 0.18 p-p (2.14 ps 1 sigma) | | |

1. Referenced detail and measurement sections may indicate a different connection type in the figures than what applies to the specific unit under test. Many figures are based on the Internal 1 meter Cabled Host to Device usage model. Specific connection type may vary depending on the type UHost under test.
2. Gen3u Lab-Sourced Signals for minimum RX Differential Input Voltage and TJ are made adjusted using the Gen3i CIC into a Lab Load. After setting these levels the Gen3i CIC is removed and the resulting signal is applied to the UHost receiver under test.

## 7.1 Descriptions of Phy Electrical Specifications

The following terms have been developed for the various Electrical Specifications:

- **Gen1i**: Generation 1 Electrical Specifications: These are the 1.5 Gbps electrical specifications for internal host to device applications.
- **Gen1m**: Generation 1 Electrical Specifications for Short Backplane and external cabling applications: These are the 1.5 Gbps electrical specifications aimed at short 1.5 Gbps internal backplane applications, External Desktop Applications using the external single lane cable, and System-to-System Data Center Applications using external Multilane cables up to two meters in length. These include only modified receiver Differential input specifications. All other electrical specifications relating to Gen1m compliance points are identical to Gen1i specifications. This specification is for these limited applications only and is not intended for any other system topology.
- **Gen1u**: Generation 1 Electrical Specifications defined at 1.5 Gbps for UHost applications. Because a Gen1i/Gen2i/Gen3i endpoint device is attached directly to the mating connection of the UHost, the electrical specifications for Gen1u allow a channel loss up to the approximate equivalence of a 1 meter data cable plus mated connector pair within the UHost.
- **Gen2i**: Generation 2 Electrical Specifications: These are 3.0 Gbps electrical specifications for internal host to device applications.
- **Gen2m**: Generation 2 Electrical Specifications for Short Backplane and External Desktop Applications: These are 3.0 Gbps electrical specifications aimed at short internal backplane applications, External Desktop Applications using the external single lane cable, and System-to-System Data Center Applications using external Multilane cables up to two meters in length. These include only modified receiver differential input specifications. All other electrical specifications relating to Gen2m compliance points are identical to Gen2i specifications. This specification is for this limited application only and is not intended for any other system topology.
- **Gen2u**: Generation 2 Electrical Specifications defined at 3.0 Gbps for UHost applications. Because a Gen1i/Gen2i/Gen3i endpoint device is attached directly to the mating connection of the UHost, the electrical specifications for Gen2u allow a channel loss up to the approximate equivalence of a 1 meter data cable plus mated connector pair within the UHost.
- **Gen3i**: Generation 3 Electrical Specifications: These are 6.0 Gbps electrical specifications for internal host to device applications.
- **Gen3u**: Generation 3 Electrical Specifications defined at 6.0 Gbps for UHost applications. Because a Gen1i/Gen2i/Gen3i endpoint device is attached directly to the mating connection of the UHost, the electrical specifications for Gen3u allow a channel loss up to the approximate equivalence of the Gen3i CIC (see 7.2.7) plus mated connector pair within the UHost.

### 7.1.3 Compliance Testing

Table 34, Table 35, Table 36, Table 37, Table 38, ~~and~~ Table 39, Table bbb, and Table ccc detail the electrical requirements for SATA compliance. Each requirement is defined in section 7.2.2. Jitter is described in section 7.3. Measurement methods for each specification are detailed in section 7.4. Section 7.5 discusses Interface States relating to OOB and power management. Section 6.7 describes the Interconnect requirements

## 7.2 Electrical specifications

Serial ATA devices and hosts shall comply with the electrical specifications shown in Table 34, Table 35, Table 36, Table 37**,** Table 38, and Table 39. The transmitter consists of the driver integrated circuit (IC), printed circuit board, and mated connector pair. The receiver consists of the receiver IC, printed circuit board, and mated connector pair.

The Serial ATA UHost (see Table 2 for applicability) shall comply with the electrical specifications shown in Table 34, Table 39, Table bbb, and Table ccc. JTF requirements in Table 36 apply to the Serial ATA UHost and are included through the measurement cross-references. The transmitter consists of the driver IC, mated connector pair and the channel between the driver IC and connector. The receiver consists of the receiver IC, mated connector pair and the channel between the receiver IC and connector.

### 7.2.2.1 General Specifications Details

This section contains the details on Table 34, Table 35, and Table bbb entries.

#### 7.2.2.1.7 DC Coupled Common Mode Voltage (Gen1i~~, Gen1m~~)

The Common mode DC level is defined as [(TX+) + (TX-)]/2 and [(RX+) + (RX-)]/2 measured at the mated connector.

This requirement only applies to Gen1i DC-coupled designs (no blocking capacitors) that hold the common-mode DC level at the connector. The four possible common mode biasing configurations shown in Figure 121 demonstrate that only DC-coupled designs need sustain the specified common-mode level to ensure interoperability. AC coupled designs may allow the DC level at the connector to float. The SATA interfaces defined as Gen1m, Gen1u, Gen2i, Gen2m, Gen2u,~~and~~ Gen3i, and Gen3u shall be AC-coupled and this requirement does not apply to these.

#### 7.2.2.1.8 AC Coupled Common Mode Voltage

The SATA interfaces, defined as Gen1i, may be AC or DC coupled as shown in Figure 121. The SATA interfaces defined as Gen1m, Gen1u, Gen2i, Gen2m, Gen2u,~~and~~ Gen3i, and Gen3u shall be AC-coupled. Figure 122 shows an example of a fully AC-coupled system.

Compliance points for SATA are defined at the connector. The AC coupled common mode voltage in Table 34 defines the open circuit DC voltage level of each single-ended signal at the IC side of the coupling capacitor in an AC coupled Phy and it shall be met during all possible power and electrical conditions of the Phy including power off and power ramping. Since the Gen1m, Gen1u, Gen2i, Gen2m, Gen2u,~~and~~ Gen3i, and Gen3u specification defines only the signal characteristics as observable at the connector, this value is not applicable to those specifications. The common mode transient requirements defined in Table 34 were determined sufficient to limit stresses on the attached components under transient conditions, which was the sole intent of the AC, coupled common mode voltage requirement. Due to this, the following is true even for Gen1i where $V_{cm,ac\ coupled}$ applies: AC coupled common mode voltage levels outside the specified range may be used provided that the transient voltage requirements of Table 34 are met.

**Figure 122 – Common Mode Biasing for Gen1m, Gen1u, Gen2i, Gen2m, Gen2u,~~and~~ Gen3i, and Gen3u**

#### 7.2.2.1.10 AC Coupling Capacitance

The value of the coupling capacitor used in AC coupled implementations. AC coupling is optional for Gen1i and mandatory for Gen1m, Gen1u, Gen2i, Gen2m, Gen2u,~~and~~ Gen3i, and Gen3u.

#### 7.2.2.1.12 Sequencing Transient Voltage Lab Load (Gen3i, Gen3u)

### 7.2.2.2 Transmitter Specification Details

This section contains the details on Table 35 and Table bbb entries.

#### 7.2.2.2.1 TX Pair Differential Impedance (Gen1i, Gen1m, Gen1u)

#### 7.2.2.2.2 TX Single-Ended Impedance (Gen1i, Gen1m, Gen1u)

#### 7.2.2.2.7 Transmitted Signal Requirements Details

This section contains the details on Table 34, Table 36, Table bbb, and Table ccc entries.

*Editor's note; It was previously identified to the editor that 7.2.2.2.7 should have been 7.2.2.3 to be consistent with the rest of the specification structure. The adding of table references to the text of 7.2.2.2.7 assumes proper changes to the hierarchy will be made by the editor.*

#### 7.2.2.2.8 TX Differential Output Voltage

The differential voltage [(TX+) – (TX-)] measured at the Transmitter shall comply with the respective electrical specifications of section 7.2.

This is measured at mated Serial ATA connector on transmit side including any pre-emphasis.
For Gen3i and Gen3u the maximum differential output voltage is likewise measured at the TX compliance point, but the minimum differential output voltage is measured after the Gen3i CIC. The minimum voltage for Gen3u is not measured after the Gen3i CIC. (See section.7.4.3.)

#### 7.2.2.2.12 TX AC Common Mode Voltage (Gen2i, Gen2m, Gen2u)

#### 7.2.2.2.13 TX AC Common Mode Voltage (Gen3i, Gen3u)

Maximum sinusoidal amplitude of common mode signal measured at the transmitter connector.

The Transmitter shall not deliver more output voltage than that specified in Table 36 and Table ccc using the common mode voltage measuring technique defined in section 7.4.2.1.

#### 7.2.2.2.15 OOB Differential Delta (Gen2i, Gen2m, Gen2u, Gen3i, Gen3u)

#### 7.2.2.2.16 OOB Common Mode Delta (Gen2i, Gen2m, Gen2u, Gen3i, Gen3u)

#### 7.2.2.2.19 Clock-to-Data Transmit Jitter (Gen1i, Gen1m, Gen1u, Gen2m, Gen2u, Gen3i, Gen3u)

Transmitters shall meet the jitter specifications for the Reference Clock characteristics specified in each case.

Table 36 and Table bbb shows the maximum amount of jitter that a transmitter may generate and still be SATA compliant and section 7.4.8 describes the measurement. Since this specification places the compliance point afterthe connector, any jitter generated at the package connection, on the printed circuit board, and at the board connector shall be included in the measurement.

#### 7.2.2.3 Receiver Specification Details

This section contains the details on Table 37 and Table ccc entries.

#### 7.2.2.3.1 RX Pair Differential Impedance (Gen1i, Gen1m, Gen1u)

#### 7.2.2.3.2 RX Single-Ended Impedance (Gen1i, Gen1m, Gen1u)

### 7.2.2.4 Lab Load Details

### 7.2.2.4.x SATA USM Host Lab Load

Due to the direct connection application of the SATA USM Host, the host shall be mated to a plug connection as shown in figure aaa. The adaptor may require additional mechanical clearance to mate to the SATA USM host connector. See SFF publication INF-8280 for host connector details.

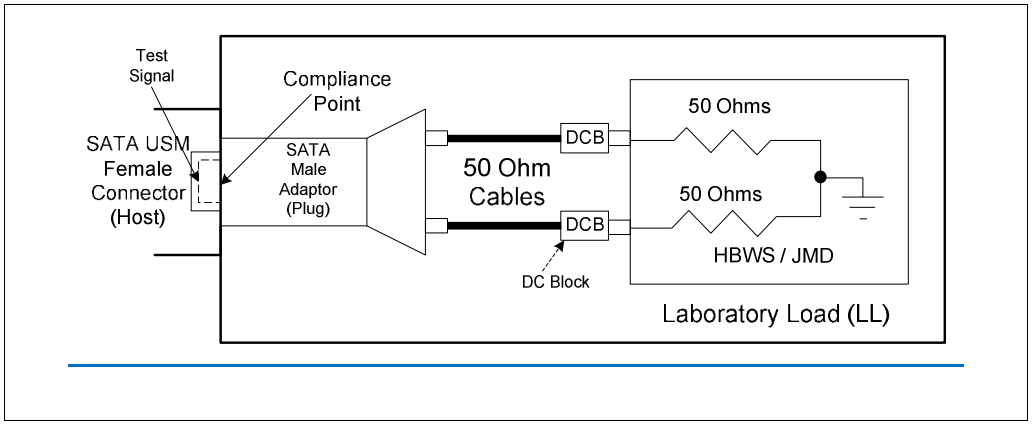


**Figure aaa – LL Laboratory Load for SATA USM Host**

The electrical characteristics of the LL shall be greater than the required performance of the parameter being measured such that the LL effects on the parameter under test may be successfully compensated for, or de-embedded, in the measured data.

### 7.2.2.5 Lab-Sourced Signal Details

### 7.2.2.5.x SATA USM Host Lab Sourced Signal Details

Due to the direct connection application of the SATA USM Host, the host shall be mated to a plug connection as shown in Figure bbb. The adaptor may require additional mechanical clearance to mate to the SATA USM host connector. See SFF publication INF-8280 for host connector details.

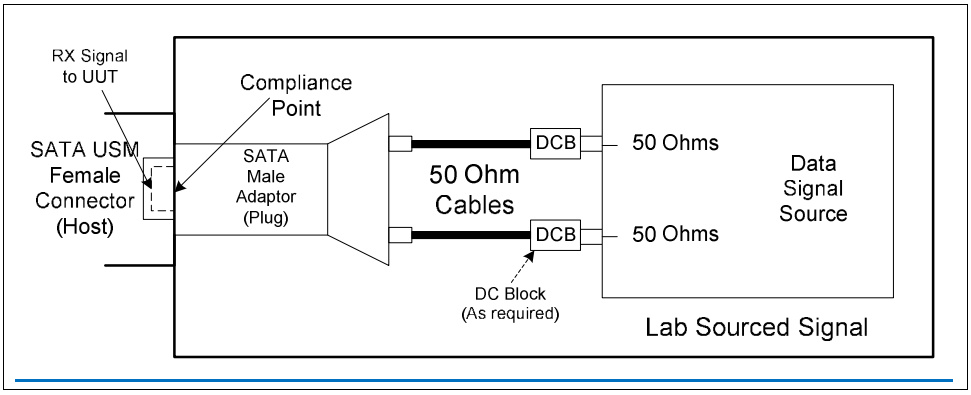


**Figure bbb – LSS Lab-Sourced Signal for SATA USM Host**

The Lab-Sourced signal is a laboratory generated signal which is calibrated into an impedance matched load of 100 Ohms differential and 25 Ohms common mode and then applied to the RX+ and RX- signals of the Receiver Under Test. The LSS represents the output of a device transmitter. In the case of Gen3i, the Gen3i CIC is used to calibrate the Lab-Sourced Signal as required, but removed from the signal path when applied to the UUT RX. When the Lab-Sourced Signal is signal is applied to the Receiver Under Test, the Frame Error Rate specifications of Table 34 shall be met.

#### 7.2.2.5.6 RX Differential Skew (Gen2i, Gen2m, Gen2u, Gen3i, Gen3u)

RX Differential Skew is the time difference between the single-ended mid-point of the RX+ signal rising/falling edge, and the single-ended mid-point of the RX- signal falling/rising edge, as measured at the RX connector. The receiver should tolerate the RX skew levels per Table 38 and Table ccc, as generated by a Lab-Sourced Signal.

#### 7.2.2.5.7 RX AC Common Mode Voltage

Max peak-to-peak sinusoidal amplitude of AC common mode signal [(RX+) + (RX-)]/2.

The Receiver shall operate to within the frame error rate cited in Table 34, when subjected to a sinusoidal common mode interfering signal with peak-to-peak voltage $V_{cmRX,ac}$ defined in Table 38 and Table ccc and swept across the frequency range, $f_{cm,acRX}$, defined in Table 38 and Table ccc at a sweep rate period no shorter than 33.33 us.

#### 7.2.2.5.9 Clock-Data Receiver Jitter Tolerance (Gen1i, Gen1m, Gen1u, Gen2i, Gen2m, Gen2u)

Jitter tolerance is the ability of the receiver to recover data in the presence of jitter. The minimum amount of jitter that a receiver shall be able to operate is the jitter tolerance specification provided in Table 38 and Table ccc and section 7.4.11 describes the measurement for Gen1 and Gen2.

#### 7.2.2.5.10 Clock-Data Receiver Jitter Tolerance (Gen3i, Gen3u)

See 7.4.12 for Gen3i and Gen3u jitter tolerance measurement details.

### 7.2.3 Loopback

In addition to meeting all electrical specifications in Table 34 through ~~Table 39~~Table ccc, all Hosts and Devices shall provide Far-End Retimed Loopback mode. Two other loopback modes are optional but if implemented shall comply with sections 7.2.3.2 and 7.2.3.3.

### 7.2.7 Compliance Interconnect Channels (Gen3i, Gen3u)

For Gen3i, Compliance Interconnect Channels are defined as a set of calibrated physical test circuits applied to the Transmitter mated connector, intended to be representative of the highest-loss interconnects. For Gen3u, the Gen3i Compliance Interconnect Channel is used to set up the Lab-Sourced Signal and then removed prior to applying the signal to the UHost receiver under test (see Table ccc). A Compliance Interconnect Channel is not used in testing the UHost transmitter.

The Compliance Interconnect Channel (CIC) is used to verify that the signal electrical characteristics at the Transmitter mated connector are sufficient to ensure compliance to the input electrical specifications for Gen3i receivers as delivered through worst-case media. The magnitude of this worst-case loss as a function of frequency is defined mathematically as a Transmitter Compliance Transfer Function (TCTF). Any linear, passive, differential two-port (e.g., a SATA cable) with loss greater than the TCTF at all frequencies and which meets the ISI loss constraint (defined below) is defined to be a CIC. (See also section **Error! Reference source not found.**.)

#### 7.3.2.1 Gen1i, Gen1m, Gen1u, Gen2i, ~~and~~ Gen2m and Gen2u Normative Requirements

For Gen1i, Gen1m, Gen1u, Gen2i, ~~and~~ Gen2m, and Gen2u, the Reference Clock characteristics are controlled by the resulting JTF (Jitter Transfer Function) characteristics obtained by taking the time difference between the Type 2 PLL output (the Reference Clock) and the data stream sourced to the PLL. The PLL CLTF -3 dB corner frequency, and other adjustable CLTF parameters such a peaking, are determined by the value required to meet the requirements of the JTF. (See section 7.4.8 for JTF information)

The JTF for Gen1i, ~~and~~ Gen1m, and Gen1u shall have the following characteristics for an encoded Gen1 D24.3 pattern (1100110011 0011001100). This is the Gen1 MFTP which is a test pattern that has clock-like characteristics and a transition density of 0.5. Gen1u shall use the values shown in Table 36 specified for Gen1i/Gen1m.

The JTF for Gen2i, ~~and~~ Gen2m, and Gen2u shall have the following characteristics for an encoded Gen2 D24.3 pattern (1100110011 0011001100). This is the Gen2 MFTP which is a test pattern that has clock-like characteristics and a transition density of 0.5. Gen2u shall use the values shown in Table 36 specified for Gen2i/Gen2m.

#### 7.3.2.2 Gen1i, Gen1m, Gen1u, Gen2i, ~~and~~ Gen2m and Gen2u Informative Comments

#### 7.3.2.3 Gen3i and Gen3u Normative Requirements

For Gen3i and Gen3u the Reference Clock characteristics are controlled by the resulting JTF (Jitter Transfer Function) characteristics obtained by taking the time difference between the Type 2 PLL output (the Reference Clock) and the data stream sourced to the PLL. The PLL CLTF -3 dB corner frequency, and other adjustable CLTF parameters such a peaking, are determined by the value required to meet the requirements of the JTF. (See section 7.4.8 for JTF information)

The JTF for Gen3i shall have the following characteristics for an encoded Gen3 D24.3 pattern (1100110011 0011001100). This is the Gen3 MFTP, which is a test pattern that has clock-like characteristics and a transition density of 0.5. Gen3u shall use the values shown in Table 36 specified for Gen3i.

### 7.3.4 Jitter Budget

There are two types of jitter, random jitter (RJ) and deterministic jitter (DJ). Random jitter is Gaussian and unbounded. For ease, the standard deviation ($RJ_\sigma$) is multiplied by a factor, which corresponds to the target BER. For a target BER = $10^{-12}$, the associated multiplication factor for Serial ATA is 14.

Total jitter (TJ) is peak-to-peak and defined as:

$$TJ = (14 * RJ_\sigma) + DJ$$

Table 36, ~~and~~ Table 38, Table bbb, and Table ccc show the compliance jitter values. The measurement of jitter is described in section 7.4.8.

## 7.4 Measurements

The values specified in Table 36 and Table bbb refer to the output signal from the unit under test at the mated connector into a Laboratory Load. The signals are not specified when attached to a system cable or backplane.

The values specified in Table 38 and Table ccc refer to the input signal from any signal source as measured at the unit under test using a Laboratory Load.

#### 7.4.2.1.2 Lone Bit Pattern Measurements, Option 1

*(Editor's note: last paragraph of this section)*

See Table 36 and Table bbb, section ~~1.1.1~~7.2.1 for $V_{diffTX}$(Min). Otherwise, the test for minimum differential voltage amplitude has not been passed. If the test for minimum voltage amplitude is failed, the number of samples, n, is to be increased and the test shall be executed again for this larger number of samples. Failure to arrive at a value n, for which the test passes, means that the requirement of the specification, for minimum differential voltage amplitude, has not been met.

#### 7.4.2.1.3 Approximation to Lone Bit Pattern Measurements, Option 2

*(Editor's note: next to last paragraph of this section)*

See Table 36 and Table bbb, section 7.2.1 for $V_{diffTX}$(Min). Otherwise, the test for minimum differential voltage amplitude has not been passed. If the test for minimum voltage amplitude is failed, the number of samples, n, is to be increased and the test shall be executed again for this larger number of samples. Failure to arrive at a value n, for which the test passes, means that the requirement of the specification for minimum differential voltage amplitude has not been met.

#### 7.4.2.2 Test for Maximum Differential Voltage Amplitudes

*(Editor's note: located in step 1 of this section)*

See Table 36 and Table bbb, section 7.2.1 for $V_{diffTX}$(Max).

### 7.4.3 Measurement of Differential Voltage Amplitudes (Gen3i, Gen3u)

The amplitude measurement of differential signals for Gen3i use different methods for the maximum amplitude and the minimum amplitude compliance tests. The maximum amplitude is a peak-to-peak value measured at the TX compliance point into a Lab Load. This limits the magnitude of signals present in the interface. The minimum amplitude is a measurement of the minimum eye opening, using the specified method, after the Gen3i CIC, into a Lab Load. This provides a minimum signal level for the receiver, measured in a manner that is representative of how a typical receiver would process the signal.

Achieving both the maximum and minimum differential amplitude compliance limits as listed in Table 36 shall be required, using the same transmitter settings for both tests.

The same methods and patterns are used for setting up the Lab-Sourced Signal for Receiver Tolerance Testing, with the compliance limits specified in Table 38.

The Gen3u transmitted signal maximum amplitude is a peak-to-peak value measured at the TX compliance point into the Lab Load. The minimum amplitude is a measurement of the minimum eye opening, using the specified method, into a Lab Load. The Gen3i CIC is not used for the Gen3u transmitted signal minimum amplitude. The measured values shall comply with the limits specified in Table bbb.

The same methods and patterns are used for setting up the Lab-Sourced Signal for Gen3u receiver tolerance testing, with the compliance limits specified in Table ccc. The Gen3i CIC is used to calibrate the Lab-Sourced Signal for Gen3u receiver tolerance testing; however, the Gen3i CIC losses are removed from the Lab-Sourced Signal prior to testing the Gen3u receiver under test for compliance.

#### 7.4.3.1 Maximum Differential Voltage Amplitude (Gen3i, Gen3u)

#### 7.4.3.2 Minimum Differential Voltage Amplitude (Gen3i, Gen3u)

The minimum TX differential amplitude shall be measured through the Gen3i CIC as specified in section 7.2.7 terminated into the Lab Load. Figure 154 shows a drawing of this test connection. A Gen3 LBP shall be used for this compliance measurement, although it is possible that with other patterns and signal path characteristics, lower amplitudes may be present in the actual system.

The Gen3u transmitted minimum TX differential amplitude shall be measured terminated into the Lab Load. Figure 154 shows a drawing of this test connection. The the Gen3i CIC is not used for this measurement. The measured value shall comply with the limits specified in Table bbb.

The minimum amplitude is defined as the vertical eye opening of the $10^{-12}$ BER contour at the 50% point of the UI, when the data is captured using the Gen3i Reference Clock JTF defined in section 7.3.2.

### 7.4.4 Rise and Fall Times

For Gen3i and Gen3u, the Rise and Fall time values, between 20% and 80%, are measured using only the Gen3 LFTP. This minimizes errors in determining the 0% and 100% reference levels using the Mode Amplitude measurement method. The analysis zone of the measurement shall be made over a minimum time length of 8 UI. This is a Lab Load measurement. The Rise and Fall time compliance limits, for the differential TX test pattern are listed in Table 36 and Table bbb. The average Rise time of all rising edges and the separate average Fall time of all falling edges within the analysis zone shall meet the Rise and Fall time compliance limits respectively. The Rise and Fall time compliance limits for the differential Data Signal Source (see Figure 171), for Receiver Tolerance testing, are also set with this method and pattern. The compliance limits for the Lab-Sourced Signal are listed in Table 38 and Table ccc.

### 7.4.5 Transmitter Amplitude

The transmitter amplitude values specified in Table 36 and Table bbb refer to the output signal from the unit under test (UUT) at the mated connector into a Laboratory Load (LL) (for Gen1i, Gen1m, Gen1u, Gen2i, ~~Gen1m,~~ Gen2m, Gen2u, ~~and~~ Gen3i, and Gen3u), or from the unit under test through a Compliance Interconnect Channel (CIC) into a Laboratory Load (for Gen3i only). The signals are not specified when attached to a system cable or backplane.

### 7.4.5.1 Transmitter Amplitude (Gen1 and Gen2)

Transmitter minimum amplitude is measured with each of three waveforms: HFTP, MFTP, and the Lone Bit Pattern (LBP). Amplitude specifications shall be met according to the measurement method outlined in section 7.4.2

The minimum amplitude value is measured during the TX minimum voltage measurement interval defined in Table 36 and Table bbb. The Reference Clock (defined in section 7.3.2) defines the ideal (zero jitter) zero crossing times. The maximum amplitude is measured according to the measurement method outlined in section 7.4.2.2 using waveforms LFTP and MFTP.

### 7.4.5.2 Transmitter Amplitude (Gen3i, Gen3u)

Transmitter minimum amplitude is measured with the Lone Bit Pattern (LBP). Amplitude specifications shall be met according to the measurement method outlined in section 7.4.3.

The minimum amplitude value is measured during the TX minimum voltage measurement interval defined in Table 36 and Table bbb. The Reference Clock (defined in section 7.3.2) defines the ideal (zero jitter) zero crossing times. The maximum amplitude is measured according to the measurement method outlined in section 7.4.3 using the MFTP waveform.

Figure 154 and Figure 155 show test setups for measuring transmitter amplitude. See section 7.4.5.1 for suggestions on compensating for losses in the test connections.

### 7.4.6 Receive Amplitude

This section describes setting the receive amplitude, a test condition common to many tests. The proper operation of the receiver is its ability to receive a signal. An example of this testing is described in section 7.4.11. The values as specified in Table 38 and Table ccc refer to the input signal from any signal source as measured at the device under test using a Laboratory Load.

### 7.4.8 Jitter Measurements

The causes of jitter are categorized into random sources (RJ) and deterministic sources (DJ). Although the total jitter (TJ) is the convolution of the probability density functions for all the independent jitter sources, this specification defines the random jitter as Gaussian and the total jitter (at a BER of $10^{-12}$) as the deterministic jitter plus 14 times the random jitter. The TJ specifications of Table 36, ~~and~~ Table 38, Table bbb, and Table ccc were chosen at a targeted BER of $10^{-12}$. In Table 36 and Table bbb, Gen3i and Gen3u TX jitter is specified by providing limits for TJ($10^{-12}$) and TJ($10^{-6}$). The BERT scan method described in section 7.4.8.1 is the only method that measures the actual TJ and is used as the reference for all TJ estimation methods. The method for estimating TJ is unique to each measurement instrument.

*Editor's note; The second paragraph below does not have the proper spacing and appears to be an incorrect addition based on a previous ECN. The same paragraph appears at the end of this section just above Figure 163. I have included that last paragraph and updated it while deleting the one I believe to be in the wrong location.*

The jitter measurement methodology is defined as a clock to data jitter measurement. Figure 160 shows a block diagram of a deserializer input. The serial data is split into two paths. One path feeds clock recovery circuitry, which becomes the reference signal used to latch the data bits of the serial data stream. This clock recovery circuitry has a low pass transfer function $H_L$. This low pass function is the CLTF of the PLL or clock recovery circuit. The jitter seen by the receiver is the time difference of the recovered clock edge to the data edge position. This time difference function is shown in Figure 161. The resulting jitter seen by the receiver has a high pass function $H_H$ shown in Figure 162. This high pass function is the JTF (Jitter Transfer Function) of the system. This defines the measurement function required by all jitter measurement methodologies. The required characteristics for the JTF ~~(Gen1i, Gen1m, Gen2i, Gen2m)~~ and the CLTF corner frequency $f_c$ are provided in section 7.3.2~~7.3.8~~. In the case

of a JMD, the JTF may be simply viewed as the ratio of the reported jitter to the applied jitter, for a sinusoidal PJ input.
~~Both the CLTF and the JTF are uniquely defined by the open loop transfer function G(s). Defining a CLTF does not uniquely define the G(s) and subsequently the JTF due to the level of cancellation of G(s) in the numerator and denominator of the CLTF especially when G(s) is much greater than 1, which is necessary for jitter tracking by the clock recovery circuit. This is the rationale for Gen1i, Gen1m, Gen2i and Gen2m directly specifying the JTF rather than the CLTF of the clock recovery circuit. When the JTF of a JMD meets the requirements specified, the JMD reported jitter levels will closer represent the jitter applied to the receiver in this reference design.~~

Both the CLTF and the JTF are uniquely defined by the open loop transfer function G(s). Defining a CLTF does not uniquely define the G(s) and subsequently the JTF due to the level of cancellation of G(s) in the numerator and denominator of the CLTF especially when G(s) is much greater than 1, which is necessary for jitter tracking by the clock recovery circuit. This is the rational for ~~Gen2i, Gen2m, and Gen3i:~~ directly specifying the JTF rather than the CLTF of the clock recovery circuit. When the JTF of a JMD meets the requirements specified, the JMD reported jitter levels will closer represent the jitter applied to the receiver in this reference design.

#### 7.4.8.1 Jitter Measurements with a Bit Error Rate Tester (BERT)

*Editor's note; This is the last paragraph in the section.*
These jitter separation issues are not present for the Gen3i and Gen3u electrical specification for TX jitter, when TJ($10^{-12}$) and TJ($10^{-6}$) are measured directly with a full population BERT scan. A full population BERT scan is one that has analyzed a sufficient population of bits versus errors to achieve a 95% confidence level at the BER level being measured. Estimations of the TJ(BER) levels based on the separation of RJ and DJ components or measurements at lower population levels shall be validated by comparing the reported values to those of the full population BERT scan which is the TJ reference standard.

### 7.4.9 Transmit Jitter (Gen1i, Gen1m, Gen1u, Gen2i, Gen2m, Gen2u)

The transmit jitter values specified in Table 36 and Table bbb refer to the output signal from the unit under test (UUT) at the mated connector into a Laboratory Load (LL) (for Gen1i, Gen1m, Gen1u, Gen2i, ~~and~~ Gen2m, and Gen2u). The signals are not specified when attached to a system cable or backplane. All the interconnect characteristics of the transmitter, package, printed circuit board traces, and mated connector pair are included in the measured transmitter jitter. Since the SATA adapter is also included as part of the measurement, good matching and low loss in the adapter are desirable to minimize its contributions to the measured transmitter jitter.

### 7.4.10 Transmit Jitter (Gen3i, Gen3u)

The Transmit Jitter values TJ($10^{-12}$) and TJ($10^{-6}$) specified in Table 36 and Table bbb refer to the output signal from the unit under test (UUT) at the mated connector into a Laboratory Load (LL), and, for Table 36, from the unit under test through a Compliance Interconnect Channel (CIC) into a Laboratory Load. The signals are not specified when attached to a system cable or backplane. All the interconnect characteristics of the transmitter, package, printed circuit board traces, and mated connector pair are included in the measured transmitter jitter. Since the SATA adapter is also included as part of the measurement, good matching and low loss in the adapter are desirable to minimize its contributions to the measured transmitter jitter.

The second measurement of the Transmit Total Jitter parameters measures the jitter on the TX signal after passing through the Gen3i Compliance Interconnect Channel (see section 7.2.7) into the Laboratory Load as is shown in Figure 166. This measurement does not apply to the Transmit Jitter values in Table bbb.

### 7.4.11 Receiver Tolerance (Gen1i, Gen1m, Gen1u, Gen2i, Gen2m, Gen2u)

### 7.4.12 Receiver Tolerance (Gen3i, Gen3u)

The performance measure for receiver tolerance and Common Mode interference rejection is the correct detection of data by the receiver. When measuring receiver and Common Mode tolerance it is necessary to set the maximum allowable jitter and Common Mode interference on the signal sent to the receiver and monitor data errors.

The data signal source provides a data signal with jitter, and a controlled rise/fall time with a matched output impedance. Additional DJ (ISI) is added by the CIC. The sine wave source provides common mode interference with a matched output impedance. The two sources are combined with resistive splitters ~~into the receiver under test (see Figure 171)~~to calibrate the data signal source for the receiver under test. Equivalent signal generation methods that provide the data with jitter, common mode interference, and an impedance-matched output are allowed. All the interconnect characteristics of the receiver, mated connector pair, printed circuit board traces, and package are included in the measured receiver jitter tolerance.

To calibrate the test signal for Receiver Tolerance testing, the Data Signal Source is measured using two procedures, one for Random Jitter (RJ) and a second for Total Jitter (TJ) and the common mode signal content.

The rise time and fall time of the Data Signal Source in the following figures shall meet the requirements listed in Table 38 and Table ccc for the Gen3i and Gen3u Lab Sourced Signal. This defines the signal rise time and fall time characteristics in the signal path before the CIC. This requirement shall be met using the rise time and fall time methods described in section 7.4.4.

Figure 169 show the test configuration for setting the Random Jitter (RJ) level as is defined in Table 38 and Table ccc for the Gen3i and Gen3u Lab Sourced Signal. The RJ level is set using a Gen3i MFTP pattern. This method minimizes the measurement errors of RJ, compared to the case when other signal degradations are present, and shall be done before adding additional jitter components and common mode signals.

This second procedure is performed after the RJ level of the Data Signal Source is set, as described above. Figure 170 shows one example approach for setting the Total Jitter (TJ) and the common mode signal level. The actual calibration plane is at the SMA connectors that will be applied to the SATA to SMA adaptor during the Receiver Tolerance test. This is shown in Figure 170 as a dotted vertical line. The JMD is used as the standard for measuring jitter, and the HBWS is used as the standard for measuring the common mode interference and signal amplitude. Since the SATA adapter is not included when setting the level of jitter, good matching and low loss in the adapter are desirable to minimize contributions to the amount of receiver jitter used in testing. Unlike other measurements, it is generally not possible to remove the effects of the SATA adapter on jitter since jitter due to mismatch depends on the entire test setup.

The measurement of the minimum and maximum amplitude levels of the test signal at the calibration plane, are performed in the same method used for these parameters for the TX amplitude tests. (see section 7.4.3 for required method) In general the maximum peak-to-peak amplitude of a Gen3 MFTP pattern is the maximum limit, and the minimum eye opening of a Gen3 LBP at a BER of $10^{-12}$ is the minimum limit. The Gen3i CIC is used to calibrate the Lab-Sourced Signal minimum amplitude for Gen3u receiver tolerance testing; however, the Gen3i CIC losses shall be removed from the Lab-Sourced Signal prior to testing of the Gen3u receiver under test.

Figure 171 shows the calibrated Lab Sourced Signal applied to the Gen3i Receiver Under Test. Figure 168 shows the calibrated Lab Sourced Signal applied to the Gen3u Receiver Under Test.

The receiver tolerance test shall be conducted over variations in parameters SSC on and off, minimum and maximum amplitude, common mode interference over the specified frequency range, the test patterns LBP and the full payload COMP described in section 7.2.4.3, and jitter which includes the maximum random and deterministic jitter of various types: data dependent, periodic, duty cycle distortion. The receiver tolerance to the impairments is required over all signal variations.

### 7.4.15 Intra-Pair Skew

Intra-pair skew measurements are important measurements of transmitters and receivers. For transmitters they are a measure of the symmetry of the SATA transmitter silicon (see Table 36 and Table bbb).

Receivers shall be tested to show required performance with the RX Differential Skew set to maximum as specified in Table 38 and Table ccc**.** Skew may be created using test cables of differing propagation delay or active control by the data signal source within the Lab-Sourced Signal generator. Receiver skew may be setup at the same time as receiver amplitude as seen in Figure 175. Use the HFTP as the pattern when setting the skew. The skew measurement is performed as described above for the transmitter.

### 7.4.20 TX AC Common Mode Voltage (Gen2i, Gen2m, Gen2u)

This parameter is a measure of common mode noise other than the CM spikes during transitions due to TX+/TX- mismatch and skews which are limited by the rise/fall mismatch and other requirements. Measurement of this parameter is achieved by transmitting through a mated connector into a Lab Load such as shown in Figure 154. The transmitter shall use an MFTP (mid-frequency test pattern). The measurement instrument may be a HBWS or other instrument with analog bandwidth of at least 3 * bitrate / 2.

### 7.4.21 Tx AC Common Mode Voltage (Gen3i, Gen3u)

### 7.4.26 TDR Differential Impedance (Gen1i, Gen1m, Gen1u)

### 7.4.27 TDR Single-Ended Impedance (Gen1i, Gen1m)

### 7.4.28 DC Coupled Common Mode Voltage (Gen1i, ~~Gen1m~~)

### 7.4.30 Sequencing Transient Voltage - Laboratory Load (Gen3i, Gen3u)

*Editor's note:*

1. *Depending on how the Lab Load definitions are organized/numbered, the reference to the section for lab load may need to change. I suggest grouping the three lab loads into the next level under a single lab load higher level section rather than splitting them into different sections The current designation is 7.2.2.4 and could stay with the following suggested organization. The "standard" lab load could be 7.2.2.4.1, and then the one for USM and the one for mSATA as 7.2.2.4.2 and 7.2.2.4.3 (editor's choiceon numbering). The mSATA lab load is currently in the lab-sourced signal section rather than in the lab load section.*
2. *Similar editorial reorganization should be considered to put all the Lab-Sourced Signals under a single section with respective subsections.*
3. *There should be a global search on lab-Sourced signal to make all of them either hyphenated or non-hyphenated as I have noticed both ways being present in the specification.*