Proposed Draft

Serial ATA International Organization

Revision 12a
06/01/2011

Serial ATA Technical Proposal #035
Title : SATA BGA SSD

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Document History

Version	Date	Comments
01	12/08/2010	• Initial release.
02	01/18/2011	• Added lab load and lab-sourced signal drawings. • Updated BGA SSD Applications section and drawing • Added actual use model description table
03	01/19/2011	• Added reference to JEDEC spec (3.2). • Changed text in “BGA SSD Applications”. • Made “compliance points” singular in all drawings. • Removed host language in LL and LSS; it was just a disclaimer • Added “de-embedding” text in LL • Added placeholder for explanatory text re: LSS
V04	02/01/2011	• Updated Section 6.6 – BGA SSD Interface (mechanical, ball-out,etc) • Added method for assigning signals to pins on different packages.
V05	02/09/2011	• Updated Ball-out table - Section 6.6.3.
V06	02/22/2011	• Updated ball-out table; continued refinement. • Eliminated “BGA SSD Ballout Schematic – Informative”. No need for this given the ball-out table is normative.
V07	03/08/2011	• Updated ball-out table • Improved labeling in ballout table and footprints to more clearly link ballout to footprints. • Added “optional” signals for SPI
V08	04/05/2011	• Updated ball-out table per TSB comments. • Cleaned up and removed other misc items.
V09	04/12/2011	• Clarified Clock and Reset signals with footnotes in ball-out table. • Cleaned up ball-out table re: how voltage signals described. • Clarified definition of DNU. • Fixed description of SATA Ground signals. • Edited SPI signal descriptions.
V10	04/26/2011	• Accepted changes from previous discussions (voltage, TEST pins, etc) • Added LL and LSS for BGA SSD Host per PHY WG • Added AC Coupling per PHY WG • Added Gen 1u/2u/3u per PHY WG • Moved five DNU’s to Optional for Low Power and VSP • Updated section #’s to match latest SATA 3.1 spec draft
V11	04/26/2011	• Added 4.2.8.8 as placeholder for updating RESERVED definition. • Edited DNU and TEST definitions • Edited RX/TX signal names to better align w/ SATA conventions. • Edited description of proposed Low Power signal placeholders.
V12	06/01/2011	• Changed JEDEC Reference to Approved, not Under Development • Updated definition of “Reserved” to cover HW resources • Added note about signal “de-embedding” to LL and LSS • Removed informative note/pictures re: test fixture. • Added separate AC Coupling drawing for BGA SSD use case.

1 Introduction

This proposal is intended to define a new electrical pin-out to allow SATA to be delivered using a BGA package so that BGA SSD products can be standardized, expanding the use of the SATA protocol in small form-factor applications. This proposal is being presented by SanDisk.

2 Technical Specification Changes

The following additions are based on the content of Serial ATA Revision 3.1RC, 18-April-2011. Changes include additions to Table 2, a new usage model, new lab test loads, and new lab-sourced signals. Although not blue and underlined, all figures added below are new and in the same format as the source document for Serial ATA Revision 3.1RC.

Proposed changes to SATA 3.1 text are marked in blue. Black text is the text of this proposal, not to be incorporated into SATA V3.1. Section headers correspond to the section in SATA 3.1 into which the proposed text is to be inserted.

3.1 Approved References

Add the following reference to the list of references:

Serial Peripheral Interface Bus (SPI) – See http://en.wikipedia.org/wiki/Serial_Peripheral_Interface_Bus. SPI is a de facto standard for a general purpose, synchronous serial interface.

MO-276E - Standard and Low Profile, Rectangular Fine Pitch Ball Grid Array Family 0.50mm Pitch

4.2.2.8 Reserved

A keyword indicating reserved bits, bytes, words, fields, code values, or physical resources (such as pins on a connector) that are set-aside for future standardization. Their use and interpretation may be specified by future extensions to this Serial ATA Revision 3.1 Release Candidate page 42 of 715 or other standards. A reserved bit, byte, word, or field shall be cleared to zero, or in accordance with a future extension to this standard. The recipient shall not check reserved bits, bytes, words, or fields. Receipt of reserved code values in defined fields shall be treated as a command parameter error and reported by returning command aborted. Reserved pins on a connector shall be not connected.

6.2 Usage Models

Table 1 – Usage Model Descriptions

Characteristic	Internal 1 meter Cabled Host to Device	Short Backplane to Device	Internal 4-lane Cabled Disk Arrays	System to System Inter connects – Data Center Applications xSATA	System to System Inter connects – External Desktop Applications eSATA	Proprietary Serial ATA Disk Arrays	Serial ATA and SAS	LIF-SATA	mSATA	BGA SSD
Use model section number	5.2.1	5.2.2	5.2.4	5.2.5	5.2.6	5.2.7	5.2.8	5.2.10	5.2.10	5.2.10
Cable and/or backplane type	Int SL	BP	Int ML	Ext ML	Ext SL	BP and cable	BP	P	BP	P
Cable length	<= 1 m		<= 1 m	<= 2 m	<= 2 m			P		P
Cable Electrical	Table 19	P	Table 19	Table 21	Table 20	Table 19	P	Table 19	P	P
Attenuation at 4.5GHz	-6dB	P	-6dB	-8dB	-8dB	-6dB	P	-6dB	P	P
Host-side connector	6.1.5	P	6.1.11 or 6.1.12	6.3.3 (key 7)	6.6.1	6.1.5 or P	SAS	6.4.3	6.5.2	NS
Device-side connector	6.1.3.1	6.1.3.1	6.1.3.1	6.6.3 (key 7)	6.6.1	6.1.3.1	6.1.3.1	6.4.2	6.5.3.1	NS
Gen1i 1.5 Gbps	R	D (host to provide received signal)	R	NS	NS	R	D	R	R	D
Gen1m 1.5 Gbps	NS	H	NS	R (key 7)	R	NS	NS	NS	NS	NS
Gen1u 1.5 Gbps	NS	NS	NS	NS	NS	NS	NS	NS	NS	H
Gen2i 3.0 Gbps	FS	D (host to provide received signal)	FS	NS	NS	FS	D	FS	FS	D
Gen2m 3.0 Gbps	NS	H	NS	FS (key 7)	FS	NS	NS	NS	NS	NS

Characteristic	Internal 1 meter Cabled Host to Device	Short Backplane to Device	Internal 4-lane Cabled Disk Arrays	System to System Inter connects – Data Center Applications xSATA	System to System Inter connects – External Desktop Applications eSATA	Proprietary Serial ATA Disk Arrays	Serial ATA and SAS	LIF-SATA	mSATA	BGA SSD
Gen2u 3.0 Gbps	NS	NS	NS	NS	NS	NS	NS	NS	NS	H
Gen3i 6.0 Gbps	FS	NS	FS	NS	NS	FS	D	FS	NS	D
Gen3u 6.0 Gbps	NS	NS	NS	NS	NS	NS	NS	NS	NS	H
Hot plug support	NS	R	NS	R	R	R	R	NS	NS	NS

Key:
R – Required : configuration requires appropriate capabilities
FS – Feature specific : configuration is supported by specification but may be tied to an optional capability
NOTE: Feature specific is intended to indicate that Gen1 is required but higher data rates are optional.
NS – Not supported : configuration is not supported by definition in specification
P – Proprietary : implementation is vendor specific and not defined in specification
H – Host
D – Device
SL – single lane
ML – multi-lane
Int – Internal
Ext – External
BP – Backplane
NOTE : Many of the references in the table are section numbers or notations of clarification which do not require Key values

5.2.10.3 BGA SSD Applications

In this application, a Gen1i/2i/3i device is directly connected, via socket or solder connection, to the PCB of a Serial ATA host. Compliance points are defined at the point of connection between the BGA SSD Device and the SATA host. All electrical specifications at this compliance point shall meet Gen1i/2i/3i specifications for the device and Gen1u/2u/3u for the host. The signaling at the host controller may exceed the Gen1i/2i/3i transmit maximum providing the Gen1i/2i/3i receiver maximum is not exceeded at the BGA interface.

The BGA SSD host is an embedded host. It is the responsibility of the system manufacturer that the mounting location for the BGA SSD provides AC coupling between the host and the device. AC coupling is not provided in the BGA SSD.

The BGA SSD device shall be tested for specification compliance as a SATA device. See section 7.4.1.1.3 (BGA SSD Lab Load) and section 7.4.1.2.3 (BGA SSD Lab-Sourced Signal).

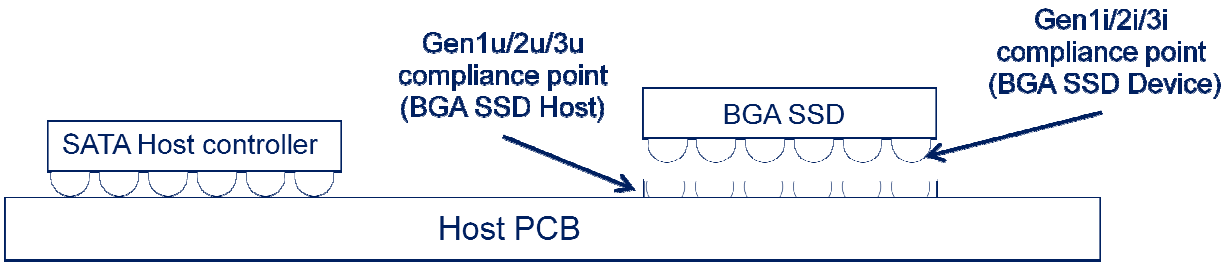


Figure x: Embedded BGA SSD Application

6.7 BGA SSD Interface (to be inserted before existing Section 6.7)

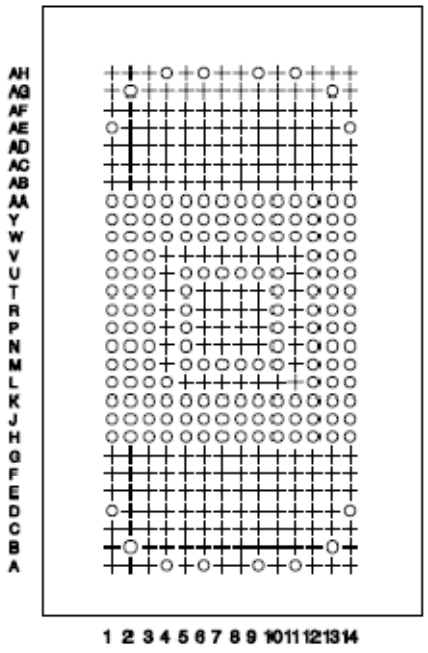
This section defines the mechanical properties of the a BGA SSD device and device interface.

6.7.1 BGA SSD Mechanical Specification

A BGA SSD shall use package variants AC, AM, AK, AL, CA, or CB, as defined in the JEDEC document "MO-276, Standard Profile and Low Profile Rectangular Fine Pitch Ball Grid Array Family, 0.50 mm Pitch"; revision E or later.

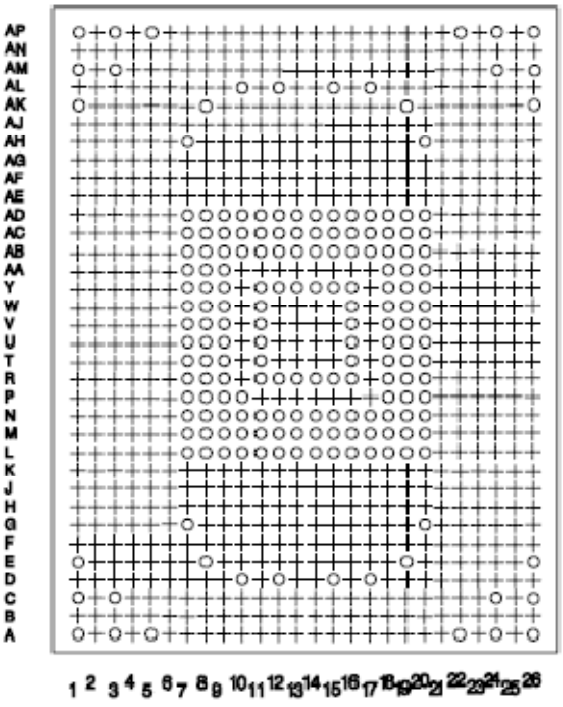
The rest of this section is informative only; refer to JEDEC MO-276E (or later) for the formal mechanical specification of BGA SSD packages.

The specified package variants for a BGA SSD use four distrinct package footprints. The package footprints (bottom view) are shown below. A "+" sign denotes a depopulated ball position. The functional balls (signals or power) for each footprint are the inner 3 or 4 rows on each footprint (square rows); the rest of the populated balls are mechanical only, for package stability. The normative signal assignment for the functional balls is specified in Section 6.6.2, BGA SSD Ballout.



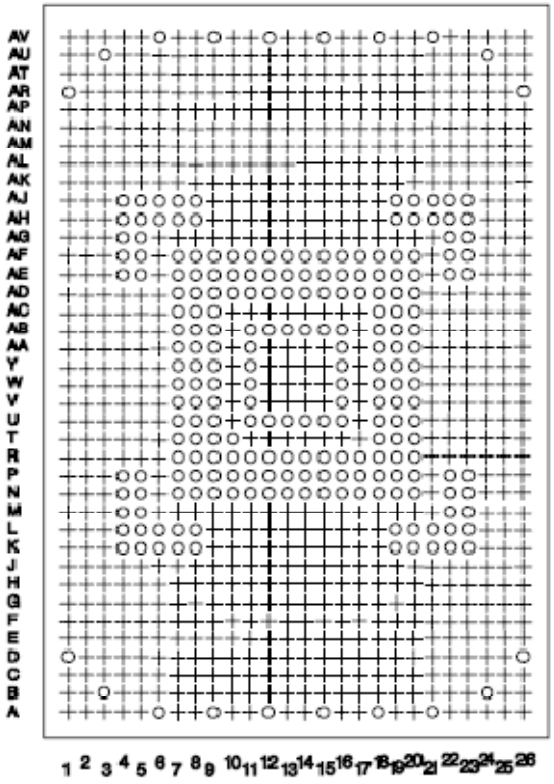
FOOTPRINT 1

Variant AC – 169 Balls



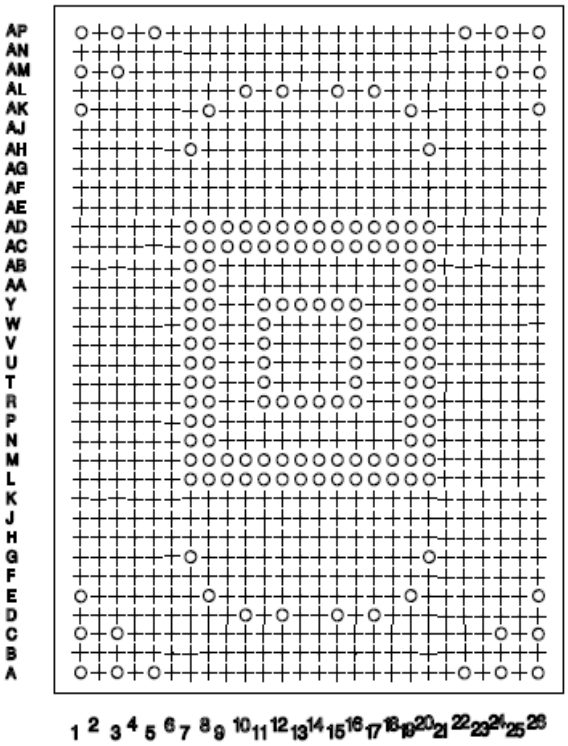
FOOTPRINT 9

Variants AK & CB – 193 Balls



FOOTPRINT 10

Variant AL – 237 Balls



FOOTPRINT 11

Variants AM & CA – 156 Balls

6.7.2 BGA SSD Ballout - Functional Signal Definition

Table x defines the signal assignment of the BGA SSD connection for each of the package types defined in Section 6.6.1.

- VSP - Vendor Specific
- RESERVED - Reserved for future standardization (SATA V3.1, Section 4.2.2.8)
- DNU (Do Not Use) - Internal test only; shall not be connected on host.
- TEST - May be connected for test/diagnostic use, but not used during normal device operation.

Table x - Signal Assignments for BGA SSD Device

BALL ASSIGNMENT # Balls (Footprint #)				BALL NAME	TYPE	DESCRIPTIONS
156 (11)	169 (1)	193 (9)	237 (10)			
SATA Interface Signals						
R7	M1	R7	U7	SATA_RX_N	Input	Differential Signal Pair A (SATA Device Receive Signal Differential Pair)
P7	L1	P7	T7	SATA_RX_P		
U7	P1	U7	W7	SATA_TX_N	Output	Differential Signal Pair B (SATA Device Transmit Signal Differential Pair)
V7	R1	V7	Y7	SATA_TX_P		
M13	J7	M13	P13	DAS	Output	Device Activity Signal
U8	P2	U8	W8	SATA_VCC	Supply	+3.3V
V8	R2	V8	Y8	SATA_VCC	Supply	+3.3V
P8	L2	P8	T8	SATA_VDD	Supply	+1.2V
R8	M2	R8	U8	SATA_VDD	Supply	+1.2V
N7	K1	N7	R7	SATA_VSS	GND	Signal Ground
T7	N1	T7	V7	SATA_VSS	GND	Signal Ground
W7	T1	W7	AA7	SATA_VSS	GND	Signal Ground
Control Signals						
L9	H3	L9	N9	XTAL_OUT	Output	System Clock output[1]
M10	J4	M10	P10	XTAL_IN	Input	System Clock input[2]
M9	J3	M9	P9	PWR_RESETN	Input	Hardware Reset[3]
Optional Signals						
AD16	AA10	AD16	AF16	SPI_MISO	Input	Master In Slave Out
AD15	AA9	AD15	AF15	SPI_CS0	Output	Chip Select
AC16	Y10	AC16	AE16	SPI_CLK	Output	Clock
AD18	AA12	AD18	AF18	SPI_CS1	Output	Chip Select
AD17	AA11	AD17	AF17	SPI_MOSI	Ouput	Master Out Slave In
AA8	V2	AA8	AC8	TEST		
L15	H9	L15	N15	TEST		
L16	H10	L16	N16	TEST		
L17	H11	L17	N17	TEST		

BALL ASSIGNMENT # Balls (Footprint #)				BALL NAME	TYPE	DESCRIPTIONS
156 (11)	169 (1)	193 (9)	237 (10)			
L18	H12	L18	N18	TEST		
AA20	V14	AA20	AC20	VSP		
M12	J6	M12	P12	VSP		
AC9	Y3	AC9	AE9	RESERVED		Future Low Power (PHYSLP)
AC11	Y5	AC11	AE11	RESERVED		Future Low Power
L13	H7	L13	N13	RESERVED		Future Low Power
Power Supply Signals						
R13	M7	R13	U13	VCC	Supply	+3.3V
R14	M8	R14	U14	VCC	Supply	+3.3V
R15	M9	R15	U15	VCC	Supply	+3.3V
R16	M10	R16	U16	VCC	Supply	+3.3V
T16	N10	T16	V16	VCC	Supply	+3.3V
U16	P10	U16	W16	VCC	Supply	+3.3V
M11	J5	M11	P11	VCC	Supply	+3.3V
L12	H6	L12	N12	VCC	Supply	+3.3V
R19	M13	R19	U19	VCC	Supply	+3.3V
R20	M14	R20	U20	VCC	Supply	+3.3V
V11	R5	V11	Y11	VCC	Supply	+3.3V
Y20	U14	Y20	AB20	VCC	Supply	+3.3V
Y19	U13	Y19	AB19	VCC	Supply	+3.3V
AA19	V13	AA19	AC19	VCC	Supply	+3.3V
AC8	Y2	AC8	AE8	VCC	Supply	+3.3V
V16	R10	V16	Y16	VCCQ	Supply	+1.8V
W16	T10	W16	AA16	VCCQ	Supply	+1.8V
Y16	U10	Y16	AB16	VCCQ	Supply	+1.8V
W11	T5	W11	AA11	VDDC	Supply	+1.2V
Y11	U5	Y11	AB11	VDDC	Supply	+1.2V
Y12	U6	Y12	AB12	VDDC	Supply	+1.2V
Y13	U7	Y13	AB13	VDDC	Supply	+1.2V
R11	M5	R11	U11	VDD	Supply	+1.2V
T11	N5	T11	V11	VDD	Supply	+1.2V
GND signals						
R12	M6	R12	U12	VSS	GND	Ground
U11	P5	U11	W11	VSS	GND	Ground
L7	H1	L7	N7	VSS	GND	Ground

BALL ASSIGNMENT # Balls (Footprint #)				BALL NAME	TYPE	DESCRIPTIONS
156 (11)	169 (1)	193 (9)	237 (10)			
L8	H2	L8	N8	VSS	GND	Ground
M7	J1	M7	P7	VSS	GND	Ground
L11	H5	L11	N11	VSS	GND	Ground
L19	H13	L19	N19	VSS	GND	Ground
L20	H14	L20	N20	VSS	GND	Ground
M19	J13	M19	P19	VSS	GND	Ground
M20	J14	M20	P20	VSS	GND	Ground
N19	K13	N19	R19	VSS	GND	Ground
P19	L13	P19	T19	VSS	GND	Ground
AC20	Y14	AC20	AE20	VSS	GND	Ground
AD20	AA14	AD20	AF20	VSS	GND	Ground
AD19	AA13	AD19	AF19	VSS	GND	Ground
AD8	AA2	AD8	AF8	VSS	GND	Ground
AD7	AA1	AD7	AF7	VSS	GND	Ground
T8	N2	T8	V8	VSS	GND	Ground
Y14	U8	Y14	AB14	VSS	GND	Ground
Y15	U9	Y15	AB15	VSS	GND	Ground
U19	P13	U19	W19	VSS	GND	Ground
P20	L14	P20	T20	VSS	GND	Ground
U20	P14	U20	W20	VSS	GND	Ground
V19	R13	V19	Y19	VSS	GND	Ground
AC7	Y1	AC7	AE7	VSS	GND	Ground
AB7	W1	AB7	AD7	VSS	GND	Ground
N8	K2	N8	R8	VSS	GND	Ground
Other Signals						
AD11	AA5	AD11	AF11	DNU		
AD9	AA3	AD9	AF9	DNU		
AC13	Y7	AC13	AE13	DNU		
AD13	AA7	AD13	AF13	DNU		
AC14	Y8	AC14	AE14	DNU		
M16	J10	M16	P16	DNU		
M14	J8	M14	P14	RESERVED		
M8	J2	M8	P8	RESERVED		
L10	H4	L10	N10	RESERVED		
L14	H8	L14	N14	RESERVED		

BALL ASSIGNMENT # Balls (Footprint #)				BALL NAME	TYPE	DESCRIPTIONS
156 (11)	169 (1)	193 (9)	237 (10)			
T19	N13	T19	V19	RESERVED		
V20	R14	V20	Y20	RESERVED		
T20	N14	T20	V20	RESERVED		
N20	K14	N20	R20	RESERVED		
M17	J11	M17	P17	RESERVED		
M18	J12	M18	P18	RESERVED		
AB8	W2	AB8	AD8	RESERVED		
AB19	W13	AB19	AD19	RESERVED		
AB20	W14	AB20	AD20	RESERVED		
AC17	Y11	AC17	AE17	RESERVED		
AD14	AA8	AD14	AF14	RESERVED		
AC15	Y9	AC15	AE15	RESERVED		
AD12	AA6	AD12	AF12	RESERVED		
AC19	Y13	AC19	AE19	RESERVED		
AC18	Y12	AC18	AE18	RESERVED		
W20	T14	W20	AA20	RESERVED		
W19	T13	W19	AA19	RESERVED		
AA7	V1	AA7	AC7	RESERVED		
Y7	U1	Y7	AB7	RESERVED		
W8	T2	W8	AA8	RESERVED		
Y8	U2	Y8	AB8	RESERVED		
AD10	AA4	AD10	AF10	RESERVED		
AC12	Y6	AC12	AE12	RESERVED		
M15	J9	M15	P15	RESERVED		
AC10	Y4	AC10	AE10	RESERVED		
	K3	N9	R9	RESERVED		
	L3	P9	T9	RESERVED		
	M3	R9	U9	RESERVED		
	N3	T9	V9	RESERVED		
	P3	U9	W9	RESERVED		
	R3	V9	Y9	RESERVED		
	T3	W9	AA9	RESERVED		
	U3	Y9	AB9	RESERVED		
	V3	AA9	AC9	RESERVED		
	W3	AB9	AD9	RESERVED		

BALL ASSIGNMENT # Balls (Footprint #)				BALL NAME	TYPE	DESCRIPTIONS
156 (11)	169 (1)	193 (9)	237 (10)			
	K12	N18	R18	RESERVED		
	L12	P18	T18	RESERVED		
	M12	R18	U18	RESERVED		
	N12	T18	V18	RESERVED		
	P12	U18	W18	RESERVED		
	R12	V18	Y18	RESERVED		
	T12	W18	AA18	RESERVED		
	U12	Y18	AB18	RESERVED		
	V12	AA18	AC18	RESERVED		
	W12	AB18	AD18	RESERVED		
	K4	N10	R10	RESERVED		
	K5	N11	R11	RESERVED		
	K6	N12	R12	RESERVED		
	K7	N13	R13	RESERVED		
	K8	N14	R14	RESERVED		
	K9	N15	R15	RESERVED		
	K10	N16	R16	RESERVED		
	K11	N17	R17	RESERVED		
	W4	AB10	AD10	RESERVED		
	W5	AB11	AD11	RESERVED		
	W6	AB12	AD12	RESERVED		
	W7	AB13	AD13	RESERVED		
	W8	AB14	AD14	RESERVED		
	W9	AB15	AD15	RESERVED		
	W10	AB16	AD16	RESERVED		
	W11	AB17	AD17	RESERVED		
	L4	P10	T10	RESERVED		

Notes:

1) Optional pin reserved for system clock output to drive crystal or other system requirements. Frequency is system implementation dependent.
2) Optional pin reserved for system clock input. Frequency is system implementation dependent.
3) Optional pin reserved for Hardware Reset. Implementation is system dependent. For detailed timing information, consult device data sheet.

7.4.1.1.3 BGA SSD Lab Load

Due to the embedded application of the BGA SSD, two different types of BGA SSD adaptors are required as laboratory loads. The device shall be mated to an adaptor as shown in Figure aaa and the host shall be mated to an adaptor as shown in Figure bbb, respectively. It is not possible to test the BGA SSD host if the BGA SSD Device is soldered in place.

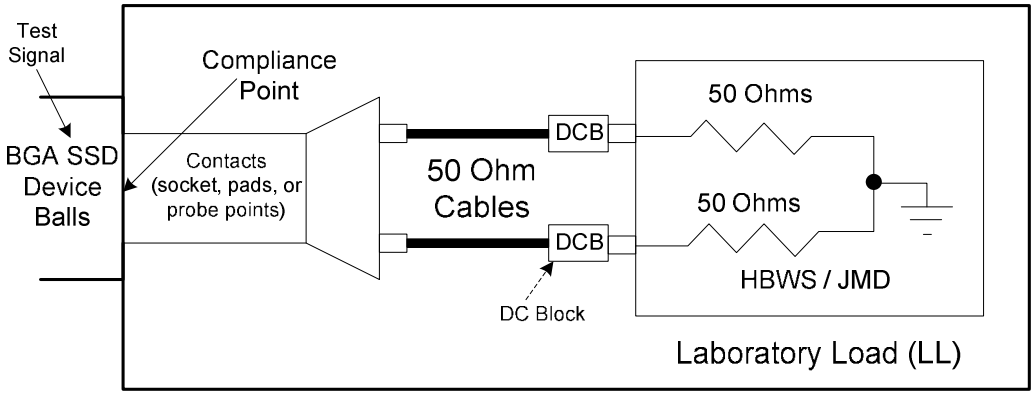


Figure aaa – LL Laboratory Load for BGA SSD Device

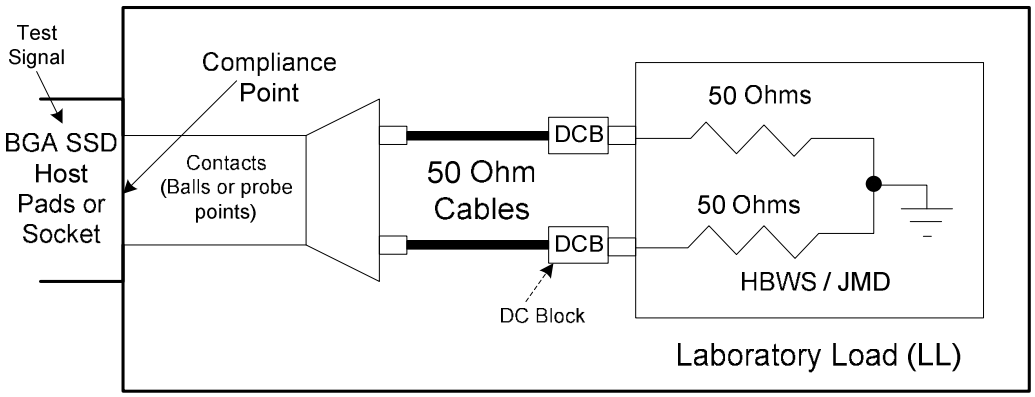


Figure bbb – LL Laboratory Load for BGA SSD Host

The electrical characteristics of the LL shall be greater than the required performance of the parameter being measured such that the LL effects on the parameter under test may be successfully compensated for, or de-embedded, in the measured data.

In a test environment, a test fixture and methodology may be used which makes it possible to deembed the signal attenuation effects of the text fixture, and thus measure compliance at the solder balls on the Device and/or the socket/pads on the Host.

7.4.1.2.3 BGA SSD Lab-Sourced Signal

As described in BGA SSD Lab Load 7.4.1.1.3, to properly provide a SATA signaling to BGA SSD devices and hosts, both types of BGA SSD adaptors are required for device and host, as shown in Figure ccc and Figure ddd, respectively. It is not possible to test the BGA SSD host if the BGA SSD Device is soldered in place.

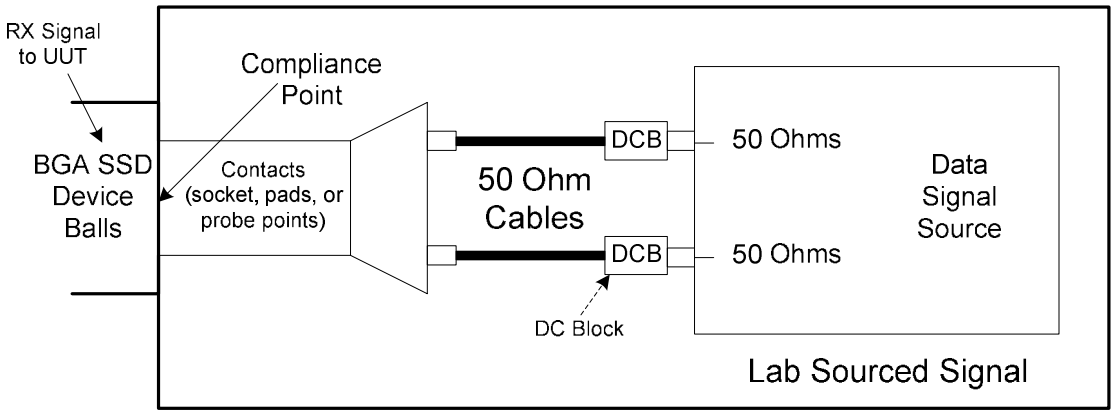


Figure ccc – Lab-Sourced Signal for SATA BGA SSD Device

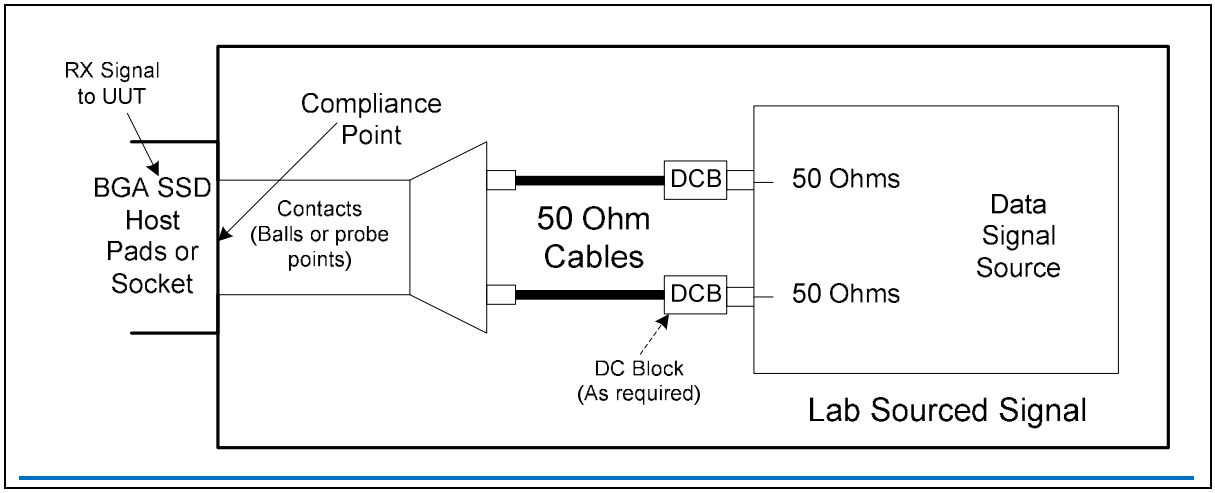


Figure ddd – LSS Lab-Sourced Signal for BGA SSD Host

The Lab-Sourced signal is a laboratory generated signal which is calibrated into an impedance matched load of 100 Ohms differential and 25 Ohms common mode and then applied to the RX+ and RX- signals of the Receiver Under Test. The LSS represents the output of a device transmitter. In the case of Gen3i, the Gen3i CIC is used to calibrate the Lab-Sourced Signal as required, but removed from the signal path when applied to the UUT RX. When the Lab-Sourced Signal is signal is applied to the Receiver Under Test, the Frame Error Rate specifications of Table 35 shall be met.

In a test environment, a test fixture and methodology may be used which makes it possible to deembed the signal attenuation effects of the text fixture, and thus measure compliance at the solder balls on the Device and/or the socket/pads on the Host.

7.2.2.1.8 AC Coupled Common Mode Voltage

The SATA interfaces, defined as Gen1i, may be AC or DC coupled as shown in Figure 128. The SATA interfaces defined as Gen1m, Gen1u, Gen2i, Gen2m, Gen2u, Gen3i, and Gen3u shall be AC-coupled. Figure 129 shows an example of a fully AC-coupled system. The BGA SSD application shall use the configuration shown in Figure 129.5.

Compliance points for SATA are defined at the connector. The AC coupled common mode voltage in Table 35 defines the open circuit DC voltage level of each single-ended signal at the IC side of the coupling capacitor in an AC coupled Phy and it shall be met during all possible power and electrical conditions of the Phy including power off and power ramping. Since the Gen1m, Gen1u, Gen2i, Gen2m, Gen2u, Gen3i, and Gen3u specification defines only the signal characteristics as observable at the connector, this value is not applicable to those specifications. The common mode transient requirements defined in Table 35 were determined sufficient to limit stresses on the attached components under transient conditions, which was the sole intent of the AC, coupled common mode voltage requirement. Due to this, the following is true even for Gen1i where $V_{cm,ac\ coupled}$ applies: AC coupled common mode voltage levels outside the specified range may be used provided that the transient voltage requirements of Table 35 are met.

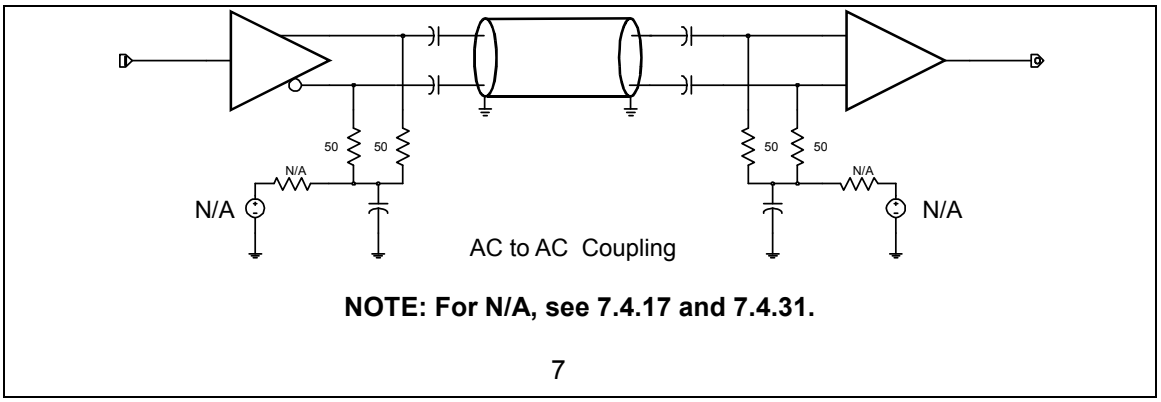


Figure 129 – Common Mode Biasing for Gen1m, Gen1u, Gen2i, Gen2m, Gen2u, Gen3i, and Gen3u

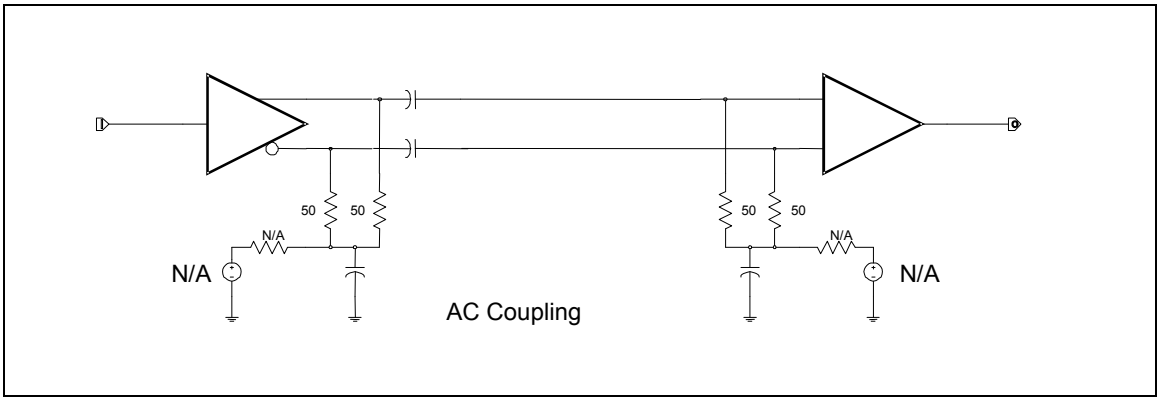


Figure 129.5 – Common Mode Biasing for BGA SSD