Proposed Draft Serial ATA International Organization

Revision 1.0a
10/~~19~~24/2011

Serial ATA Technical Proposal: SATA31_TPR_C108
Title: Device Sleep
Sponsors: SanDisk, Samsung, Intel, Microsoft

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Document History

Version	Date	Comments
00	06/24/2011	• Initial release.
01	07/15/2011	• Tweaks to state machines • Updated electrical description • Added SSP preservation • Added exclusion for ODD devices
02	07/25/2011	• Miscellaneous updates
03	8/14/2011	• Changed name from PHYSLP to DEVSLP. • Removed all PHY state machine changes. • Rewrote informative protocol description as normative text. • Added Micro and LIF SATA connector pin assignments. • Changed standard connector pin assignment away from Pin 11. • Removed stipulation that HFC is disabled if DEVSLP enabled. • Added parameterization of tDSI • Added COMWAKE-after-DEVSLP supported bit
04	8/24/2011	• Added descriptions of COMWAKE vs. COMRESET exit protocol. • Added notes to describe behavior on timing violations. • Enhanced definition of COMWAKE_After_DEVSLP. • Max tDSW now 255ms; all 8 bits in Identify Device Data log field.
V05	09/07/2011	• Misc mostly editorial changes after initial Digital Group review. • Accepted changes and starting fresh cycle. • Removed micro SATA connector per input from CabCon
V06	09/16/2011	• Naming/Text to distinguish between Feature, I/F State, and signal. • Separated host and device requirements for DevSleep • Continued refinement of entry/exit conditions.
V07	9/22/2011	• Included most comment resolutions from 9/19 Digital group review. • Updated/distinct naming for Feature, State, and Signal. • New naming for timing variables (tDSW, tDSO). • Added timing requirement for device detect of DEVSLP assertion. • Added new conditions for device entering DevSleep.
V08	9//30/2011	• Updated many editorial comments from various reviewers.
V09	10/06/2011	• Removed Standard SATA and LIF connectors (will do later) • Put DETO and MDAT in new Qword: DEVSLP Timing Variables • Moved “DevSleep_to_ReducedPwrState” to IDENTIFY DEVICE word 77 • Updated timing picture. • Updated electrical table
V0.9a	10/09/2011	• Update on 8.3 (electrical) to address 1.8V hosts, and move pull-up to host.
V1.0	10/19/2011	• Separated DEVSLP timing picture and variables table and put in overview section. • Embedded timing diagram and table as native objects instead of JPEG. • Updated device entry conditions (DI0, no commands outstanding) • Replaced value of “10 us” with reference to DMDT definition in device entry/exit. • Padded DETO and MDAT to be on byte boundaries. • Updated DEVSLP timing diagram. • Update on 8.3 (electrical): Still low voltage, but moved pull-up back to device.
V1.0a	10/24/2011	• Made changes to require support of Identify Device data log. • Eliminated note re: MDAT violation (not needed).

1 Introduction

This proposal defines a new host-controlled SATA interface power state, DevSleep, and a new host-controlled HW signal, DEVSLP, which together enable a SATA host and device to enter an ultra-low interface power state, including the possibility of completely powering down host and device PHYs.

The DevSleep interface power state and DEVSLP signal are enabled/disabled by a new SATA feature, Device Sleep, controlled by the SET FEATURES command.

2 Technical Specification Changes

The following additions are based on the content of Serial ATA Revision 3.1, 18-July-2011 and Serial ATA Technical Proposal #035, SATA BGA SSD, 01-June-2011. Proposed additions to SATA 3.1 and Technical Proposal #035 are marked in blue. Proposed deletions are marked in ~~red~~. Black text is original text. Section headers correspond to the section in SATA 3.1 and Technical Proposal #035, into which the proposed text is to be inserted.

6 Cables and Connectors

6.3 Internal Slimline cables and connectors

This section provides capabilities required to enable Serial ATA in “Slimline” optical disk drives.

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The definition has the following constraints:

- No device activity signal support
- No support for DevSleep interface power state
- Analog audio is not supported
- External cable and connector are not supported
- No hot plug support
- Warm plug support is usage model dependent

6.5 mSATA Connector

Table 19 defines the signal assignment of the mSATA connection. This connection does not support hot plug capability, so there is no connection sequence specified. There are a total of 52 pins.

- 5 pins for 3.3V source
- 3 pins for 1.5V source
- 13 pins for GND
- 4 pins for transmitter/receiver differential pairs
- 1 pin for device activity / disable staggered spin-up
- 1 pin for presence detection
- 2 pins for Vendor Specific / Manufacturing
- 2 pins for Two Wire Interface
- ~~20~~19 reserved pins (no connect)
- 1 pin to indicate mSATA use (no connect)

Table 17 – Signal Assignments for mSATA

Pin #	Type	Description
…	…	…
P44	~~Reserved~~ DEVSLP	~~No Connect~~ Enter/Exit DevSleep
…	…	…

6.6 [editor’s note: 6.3.2 in Serial ATA Technical Proposal #035] BGA SSD Ballout - Functional Signal Definition

Table x - Signal Assignments for BGA SSD Device

BALL ASSIGNMENT # Balls (Footprint #)				BALL NAME	TYPE	DESCRIPTIONS
156 (11)	169 (1)	193 (9)	237 (10)			
Optional Signals						
…	…	…	…	…	…	…
AC9	Y3	AC9	AE9	~~RESERVED~~DEVSLP	Input	~~Future Low Power~~ Enter/Exit DevSleep
…	…	…	…	…	…	…

7 PHY Layer

7.5 Interface States

7.5.1 Out of Band Signaling

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Any spacing less than or greater than the COMWAKE detector off threshold in Table 42 shall negate the COMWAKE detector output. The COMWAKE OOB signaling is used to bring the Phy out of the Partial or Slumber power down state ~~a power-down state (Partial or Slumber)~~ as described in section 8.4.3.2. The interface shall be held inactive for at least the maximum COMWAKE detector off threshold in Table 42 after the last burst to ensure far-end detector detects the negation properly. The device shall hold the interface inactive no more than the maximum COMWAKE detector off threshold plus two Gen1 Dwords (approximately 228.3 ns) at the end of a COMWAKE to prevent susceptibility to crosstalk.

7.5.1.4 COMWAKE

…

Any spacing less than 35 ns or greater than 175 ns shall invalidate the COMWAKE detector output. The COMWAKE OOB signaling is used to bring the Phy out of the Partial or Slumber interface power down state ~~a power-down state (Partial or Slumber)~~ as described in section 8.1. The interface shall be held inactive for at least 175 ns after the last burst to ensure far-end detector detects the negation properly. The device shall hold the interface inactive no more then 228.3 ns (175 ns + two Gen1 Dwords) at the end of a COMWAKE to prevent susceptibility to crosstalk.

8 OOB and Phy Power States

8.1 Interface Power States

Serial ATA interface power states are controlled by the device and host controller. The interface power states are defined as described in Table 59.

Table 59 – Interface Power States

State	Description
PHYRDY	The Phy logic and main PLL are both on and active. The interface is synchronized and capable of receiving and sending data.
Partial	The Phy logic is powered, but is in a reduced power state. Both signal lines on the interface are at a neutral logic state (common mode voltage). The exit latency from this state shall be no longer than 10 us unless when Automatic Partial to Slumber transitions is supported. When Automatic Partial to Slumber Transitions are enabled the exit latency from this state shall be no longer than the maximum Slumber exit latency.
Slumber	The Phy logic is powered but is in a reduced power state. The common mode level of the AC coupled transmitter is allowed to float (while maintaining zero differential) as long as it remains within the limits cited in Table 35 entry for AC coupled common mode voltage. The exit latency from this state shall be no longer than 10 ms.
DevSleep	The Phy logic may be powered down. The common mode level of the AC coupled transmitter is allowed to float (while maintaining zero differential) as long as it remains within the limits cited in Table 35 entry for AC coupled common mode voltage. The exit latency from this state shall be no longer than 20 ms, unless otherwise specified by DETO in Identify Device Data log (see 13.7.7.1.DEVSLPTimingVariables).

8.2 Asynchronous Signal Recovery (optional)

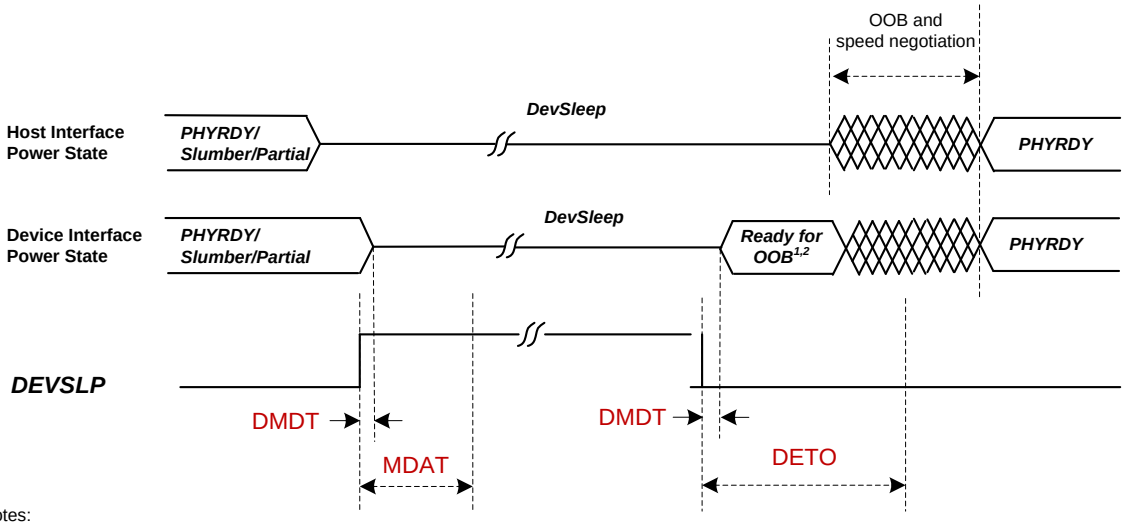
8.2.1 [8.2.new] Device Sleep and ASR

If the host supports the Device Sleep feature (see 13.3), then the host should support Asynchronous Signal Recovery. If the device supports Device Sleep feature, then the device should support Asynchronous Signal Recovery.

8.3 [8.new] DEVSLP Signal Protocol and Timing

8.3.1 [8.new.Overview] DEVSLP Overview

Figure xx and Table xx provide an overview of the DEVSLP protocol.



Notes:
1. The interface power state is in Partial/Slumber if DevSleep_to_ReducedPwrState = 1 and DEVSLP was asserted while device was in Partial/Slumber.
2. The interface is in active state if DevSleep_to_ReducedPwrState = 0 or DEVSLP was asserted while device was in active state.

Figure xx – DEVSLP Protocol Overview

Table xx – DevSleep Timing Parameters

Symbol	Parameter	Value
MDAT	**Minimum DEVSLP Assertion Time**: Minimum time for which the host shall assert DEVSLP, once it has been asserted.	10ms unless otherwise specified in Identify Device Data log.
DMDT	**DEVSLP Minimum Detection Time**: Minimum time the device needs to de-bounce the DEVSLP signal after detecting it has been asserted.	10 uSec
DETO	**DevSleep Exit Timeout**: Maximum time from when DEVSLP is negated, to when the device shall be ready to detect OOB signals.	20ms unless otherwise specified in Identify Device Data Log.

8.3.2 [8.new.Host] Host Requirements for DEVSLP

The host shall assert DEVSLP to request a device to enter the DevSleep interface power state (see 8.1). The host shall negate DEVSLP to request a device to exit from the DevSleep interface power state.

DEVSLP shall be asserted for the entire duration that a host wishes the device to remain in the DevSleep interface power state.

The host should not assert DEVSLP unless all of the following conditions are true:

a) the Device Sleep feature is supported (i.e., IDENTIFY DEVICE data word 78 bit 8 is set to one);
b) the Device Sleep feature is enabled (i.e., IDENTIFY DEVICE data word 79 bit 8 is set to one);
c) the Shadow register block reflects command completion (see 4.1.1.18); and
d) the SActive register is cleared to zero.

If the host asserts DEVSLP:

a) the host may power down its Phy or any other subsystems (e.g., PLL's, clocks, etc);
b) the host shall not initiate any host to device communications; and
c) the host shall ignore any device to host communications.

Once asserted, the host shall keep DEVSLP asserted for a minimum of 10ms unless otherwise specified in the MDAT field (bits 4:0) of the DEVSLP Timing Variables quad word in Identify Device Data log (see 13.7.7.1.DEVSLPTimingVariables).

After negating DEVSLP, the host shall keep it negated until the host Phy has reached the PHYRDY interface power state (see 8.1).

8.3.3 [8.new.Device] Device Requirements for DEVSLP

If the Device Sleep feature is supported (i.e., IDENTIFY DEVICE data word 78 bit 8 is set to one), then the requirements specified in this sub-clause shall apply.

After power up, the device shall ignore DEVSLP until the Device Sleep feature is enabled by a SET FEATURES command from the host (see 3.3).

If:

a) the Device Sleep feature is enabled (i.e., IDENTIFY DEVICE data word 79 bit 8 is set to one);
b) the device detects that DEVSLP has been asserted for greater than or equal to ~~>=~~ DMDT ~~ms~~ (see Table xx);
c) no commands are outstanding; and
d) the device is in the DI0: Device_Idle state,

then:

a) the device shall enter the DevSleep interface power state;
b) the device may power down its Phy and any other subsystems (e.g., PLL's, clocks, media);
c) the device shall not initiate any device to host communications; and
d) the device shall ignore any host to device communications.~~;~~

o~~O~~therwise the device shall not enter the DevSleep interface power state, and shall not return an error to the host.

If the device detects that DEVSLP has been negated for greater than or equal to ~~>=~~ DMDT ~~ms~~ (see Table xx), then:

a) the device shall be ready to detect OOB signals in less than or equal to 20ms unless otherwise specified in the DETO field (bits 12:5) of the DEVSLP Timing Variables quad word in Identify Device Data log (see 13.7.7.1.DEVSLPTimingVariables);
b) if DevSleep_to_ReducedPwrState is not supported (see 13.2.1.17), then the device shall resume operation in the DP1: DR_Reset state; and
c) if DevSleep_to_ReducedPwrState is supported (see 13.2.1.17), then
    i. the device shall transition to the DP8: DR_Partial state if the DEVSLP signal was asserted while the device was in the DP8: DR_Partial state;
    ii. the device shall transition to the DP9: DR_Slumber state if the DEVSLP signal was asserted while the device was in the DP9: DR_Slumber state; or
    iii. the device shall transition to the DP1: DR_Reset state.

~~Note: If the device is not ready to detect OOB signals within the time required by the specification, the system may experience performance/power degradation during host/device renegotiation.~~

8.3.4 [8.new.2] DEVSLP Signal Electrical Characteristics

The DEVSLP signal shall be implemented with the electrical constraints in table yy and table zz. DEVSLP is a level triggered signal, asserted high.

The device shall tolerate the DEVSLP signal being shorted to ground. The device shall tolerate a no-connect floating DEVSLP signal.

Figure yy is an example of a DEVSLP implementation for illustrative purposes. Note that the host should not rely on particular device resistor values.

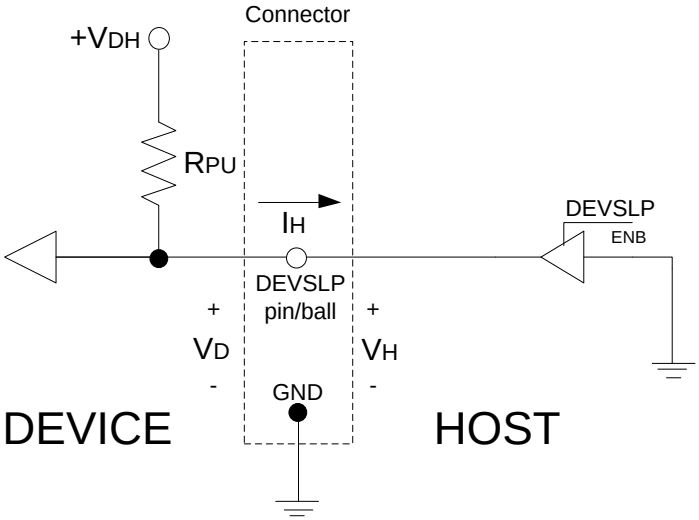


Figure yy – Example DEVSLP electrical block diagram

All voltage references in table yy and table zz are to ground pin on the host connector.
All voltages and currents in table yy and table zz are measured at DEVSLP pin on the host connector.

Table yy – Device side DEVSLP Electrical Parameters

Parameter	Min value	Max value	Description & Conditions
V_{DIn}	-0.5 V	3.6 V	Tolerated input voltage
$V_{HAssert}$		2.1 V	Voltage presented to host when signal not driven low. Value specified for all allowable $I_{HAssert}$
$I_{HNegate}$		100 uA	Device current delivered to host when host driving signal low. Value specified at $V_{HNegate}$ voltage of 0 V

Table zz – Host side DEVSLP Electrical Parameters

Parameter	Min value	Max value	Description & Conditions
V_{HIn}	-0.5 V	2.1 V	Tolerated input voltage
$I_{HAssert}$	-1 uA	10 uA	Host leakage current when signal not driven. Value specified for all voltages between 0 V and $V_{HAssert}$ of 2.1 V
$V_{HNegate}$	0 V	0.225 V	Host voltage presented to device when the signal driven low Value specified for all allowable $I_{HNegate}$

13 Application Layer

13.2 IDENTIFY (PACKET) DEVICE

13.2.1 IDENTIFY DEVICE

Table 84 – IDENTIFY DEVICE information

Word	O/M	F/V	
...	...	...	...
77	O		Serial ATA Additional capabilities
		R	15-~~7~~8 Reserved
		F	7 DevSleep_to_ReducedPwrState
			6 Supports RECEIVE FPDMA QUEUED and SEND FPDMA QUEUED commands
		F	5 Supports NCQ Queue Management Command
		F	4 Supports NCQ Streaming
		V	3-1 Coded value indicating current negotiated Serial ATA signal speed
		F	0 Shall be cleared to zero
78	O		Serial ATA features supported
		R	15-~~8~~9 Reserved
		F	8 1= Device Sleep supported
		F	7 1 = Supports NCQ Autosense
		F	6 1 = Supports software settings preservation
		F	5 1 = Hardware Feature Control is supported
		F	4 1 = Supports in-order data delivery
		F	3 1 = Device supports initiating interface power management
		F	2 1 = Supports DMA Setup Auto-Activate optimization
		F	1 1 = Supports non-zero buffer offsets in DMA Setup FIS
		F	0 Shall be cleared to zero
79	O		Serial ATA features enabled
		R	15-~~8~~9 Reserved
		V	8 1 = Device Sleep enabled
			7 1 = Device Automatic Partial to Slumber transitions enabled
		V	6 1 = Software settings preservation enabled
		V	5 1 = Hardware Feature Control ~~is~~ enabled
		V	4 1 = In-order data delivery enabled
		V	3 1 = Device initiating interface power management enabled
		V	2 1 = DMA Setup Auto-Activate optimization enabled
		V	1 1 = Non-zero buffer offsets in DMA Setup FIS enabled
		F	0 Shall be cleared to zero
...	...	...	...

Key:
M = Support of the word is mandatory.
O = Support of the word is optional.
F = the content of the bit, field, or word is fixed and does not change. For removable media devices, these values may change when media is removed or changed.
V = the contents of the bit, field, or word is variable and may change depending on the state of the device or the commands executed by the device.
R = the content of the bit, field, or word is reserved and shall be zero.

13.2.1.17 Word 77: Serial ATA Additional Capabilities

Word 77 reports additional optional capabilities supported by the device. Support for this word is optional and if not supported, the word shall be zero indicating the device has no support for additional Serial ATA capabilities.

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Bit 7 indicates whether the device supports the DevSleep_to_ReducedPwrState capability. When cleared to zero, then the device does not support remembering whether it was in Partial or Slumber after detection of assertion, and subsequent detection of negation, of DEVSLP. When set to one, then the device supports remembering whether it was in Partial or Slumber after detection of assertion, and subsequent detection of negation, of DEVSLP.

Bit ~~7~~8-15 are reserved and shall be cleared to zero.

13.2.1.18 Word 78: Serial ATA features supported

Word 78 reports the optional features supported by the device. Support for this word is optional and if not supported the word shall be zero indicating the device has no support for new Serial ATA capabilities.

...

Bit 8 indicates whether the device supports the Device Sleep feature (see 8.new). When set to one:

a) the device supports the Device Sleep feature;
b) the device shall support the Identify Device data log; and
c) the DEVSLP Timing Variables field Valid bit shall be set to 1.

When cleared to zero, the device does not support the Device Sleep feature.

Bit ~~8~~9-15 are reserved and shall be cleared to zero.

13.2.1.19 Word 79: Serial ATA features enabled

Word 79 reports which optional features supported by the device are enabled. This word shall be supported if optional Word 78 is supported and shall not be supported if optional Word 78 is not supported.

...

Bit 8 indicates whether or not the Device Sleep feature is enabled (see 13.3.new). When set to one, the Device Sleep feature is enabled. When cleared to zero, the Device Sleep feature is disabled.

Bit ~~8~~9-15 are reserved and shall be cleared to zero.

13.3 SET FEATURES

Devices are informed of host capabilities and have optional features enabled/disabled through the SET FEATURES command defined in the ATA8-ACS standard. Serial ATA features are controlled using a features value as defined in Table 87.

Table 87 – Features enable/disable values

Features(7:0) Value	Description
10h	Enable use of Serial ATA feature
90h	Disable use of Serial ATA feature

Count(7:0) contains the specific Serial ATA feature to enable or disable. The specific Serial ATA features in which SET FEATURES is applicable are defined in Table ble 88.

Table 88 – Feature identification values

Count(7:0) Value	Description
00h	Reserved
01h	Non-zero buffer offset in DMA Setup FIS
02h	DMA Setup FIS Auto-Activate optimization
03h	Device-initiated interface power state transitions
04h	Guaranteed In-Order Data Delivery
05h	Asynchronous Notification
06h	Software Settings Preservation
07h	Device Automatic Partial to Slumber transitions
08h	Enable Hardware Feature Control
09h	Device Sleep
~~09~~0Ah - FFh	Reserved for future Serial ATA definition

13.3.1 [editor's note: 13.3.NEW] Device Sleep

A Count(7:0) value of 09h is used by the host to enable or disable Device Sleep. If the value in Features(7:0) is set to 10h, then the device shall set IDENTIFY DEVICE word 79, bit 8, to one. If the value in Features (7:0) is set to 90h, then the device shall clear IDENTIFY DEVICE word 79, bit 8, to zero, As a result of processing a power on reset, the Device Sleep feature shall be disabled.

If:

a) the host attempts to enable or disable the Device Sleep feature; and
b) the Device Sleep feature is not supported (i.e., IDENTIFY DEVICE data word 78 bit 8 is cleared to zero),

then the device shall return command aborted.

13.5 Software Settings Preservation (Optional)

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The software settings that shall be preserved across COMRESET are listed below. The device is only required to preserve the indicated software setting if it supports the particular feature/command the setting is associated with.

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SET FEATURES (Device Sleep): Device Sleep enable/disable setting established by the SET FEATURES command with a Subcommand code of 10h or 90h.

...

13.7 SATA Logs

13.7.1 Identify Device Data Log (30h)

13.7.1.1 Serial ATA Settings (page 08h)

Table 95 – Identify Device Data log (log 30h page 08h)

Byte	O/M	F/V	
00h..27h			As defined in the ~~ATA8-ACS~~ATA/ATAPI Command Set - 3 (ACS-3) standard
28h..29h	O	V	Current Hardware Feature Control Identifier (Word)
2Ah..2Bh	O	F	Supported Hardware Feature Control Identifier (Word)
2Ch..2Fh	O	R	Reserved
30h..37h	O		DEVSLP Timing Variables (Qword)
		F	63 Valid
		R	62:16 Reserved
		F	15:8 DevSleep Exit Timeout, in ms (DETO)
		R	5:7 Reserved
		F	4:0 Minimum DEVSLP Assertion Time, in ms (MDAT)
~~2C~~38h..FFh		R	Reserved
O Support of the word is optional. M Support of the word is mandatory. F The content of the field is fixed and does not change. The DCO command may change the value of a fixed field. V The contents of the field are variable and may change depending on the state of the device or the commands processed by the device. R = the content of the bit, field, or word is reserved and shall be zero.			

13.7.1.1.1 [13.7.7.1.DEVSLPTimingVariables] DEVSLP Timing Variables

Bits 15:8 contain the DevSleep Exit Timeout value (DETO), the maximum time, in ms, from when DEVSLP is negated, to when the device shall be ready to detect OOB signals. If the value in DETO is zero, then the host should use 20 ms as the value of DETO.

Bits 4:0 contain the Minimum DEVSLP Assertion time (MDAT), the minimum time, in ms, for which the host shall assert DEVSLP, once it has been asserted. If the value in MDAT is zero, then the host should use 10 ms as the value of MDAT.

14 Host Adapter Register Interface

14.1 Status and Control Registers

14.1.1 SStatus Register

The Serial ATA interface Status register - SStatus - is a 32-bit read-only register that conveys the current state of the interface and host adapter. The register conveys the interface state at the time it is read and is updated continuously and asynchronously by the host adapter. Writes to the register have no effect.

DET The DET value indicates the interface device detection and Phy state.
- 0000b No device detected and Phy communication not established
- 0001b Device presence detected but Phy communication not established
- 0011b Device presence detected and Phy communication established
- 0100b Phy in offline mode as a result of the interface being disabled or running in a BIST loopback mode

All other values reserved

SPD The SPD value indicates the negotiated interface communication speed established
- 0000b No negotiated speed (device not present or communication not established)
- 0001b Generation 1 communication rate negotiated
- 0010b Generation 2 communication rate negotiated
- 0011b Generation 3 communication rate negotiated

All other values reserved

IPM The IPM value indicates the current interface power management state
- 0000b Device not present or communication not established
- 0001b Interface in active state
- 0010b Interface in Partial power management state
- 0110b Interface in Slumber power management state
- 1000b Interface in DevSleep power management state

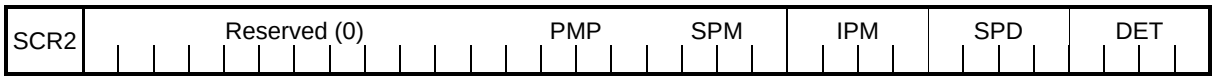
All other values reserved

Reserved All reserved fields shall be cleared to zero.

NOTE – The interface needs to be in the active state for the interface device detection value (DET field) to be accurate. When the interface is in the Partial, ~~or~~ Slumber, or DevSleep state no communication between the host and target is established resulting in a DET value corresponding to no device present or no communication established. As a result the insertion or removal of a device may not be accurately detected under all conditions such as when the interface is quiescent as a result of being in the Partial, ~~or~~ Slumber, or DevSleep state. This field alone may therefore be insufficient to satisfy all the requirements for device attach or detach detection during all possible interface states.

14.1.2 SControl Register

The Serial ATA interface Control register - SControl - is a 32-bit read-write register that provides the interface by which software controls Serial ATA interface capabilities. Writes to the SControl register result in an action being taken by the host adapter or interface. Reads from the register return the last value written to it.



DET The DET field controls the host adapter device detection and interface initialization.
- 0000b No device detection or initialization action requested
- 0001b Perform interface communication initialization sequence to establish communication. This is functionally equivalent to a hard reset and results in the interface being reset and communications reinitialized. Upon a write to the SControl register that sets the DET field to 0001b, the host interface shall transition to the HP1: HR_Reset state and shall remain in that state until the DET field is set to a value other than 0001b by a subsequent write to the SControl register.
- 0100b Disable the Serial ATA interface and put Phy in offline mode.
- All other values reserved

SPD The SPD field represents the highest allowed communication speed the interface is allowed to negotiate when interface communication speed is established
- 0000b No speed negotiation restrictions
- 0001b Limit speed negotiation to a rate not greater than Gen 1 communication rate
- 0010b Limit speed negotiation to a rate not greater than Gen 2 communication rate
- 0011b Limit speed negotiation to a speed not greater than Gen3 communication speed
- All other values reserved

IPM The IPM field represents the enabled interface power management states that may be invoked via the Serial ATA interface power management capabilities
- 0000b No interface power management state restrictions
- 0001b Transitions to the Partial power management state disabled
- 0010b Transitions to the Slumber power management state disabled
- 0011b Transitions to both the Partial and Slumber power management states disabled
- 0100b Transitions to the DevSleep power management state are disabled
- 0101b Transitions to the Partial and DevSleep power management states are disabled
- 0110b Transitions to the Slumber and DevSleep power management states are disabled
- 0111b Transitions to the Partial, Slumber and DevSleep power management states are disabled