Proposed Draft **Serial ATA International Organization**

Revision 01
01/02/2012

Serial ATA Technical Proposal: 039
Title: DEVSLP Assignment on Standard SATA Connector
Sponsor: SanDisk

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Document History

Version	Date	Comments
00	12/07/2011	• Initial release.
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1 Introduction

This proposal assigns a pin for the DEVSLP signal to the standard SATA connector.

2 Technical Specification Changes

The following additions are based on the content of Serial ATA Revision 3.1, 18-July-2011; Serial ATA Technical Proposal #035, SATA BGA SSD, 01-June-2011; and Serial ATA Technical Proposal #037, Standard SATA Connector 3.3V Power Pin Assignments, 12-Oct-2011. Proposed additions existing text are marked in blue. Proposed deletions are marked in ~~red~~. Black text is original text.

6 Cables and Connectors

6.1 Internal cables and connectors

6.1.3 Mating Interfaces

6.1.3.2 Standard SATA Connector (3.5-inch & 2.5-inch HDD)

Table 3 – Standard SATA Connector (3.5-inch & 2.5-inch HDD)

	Name	Type	Description	Cable Usage[2, 3]	Backplane Usage[3]
Signal Segment Key					
Signal Segment	S1	GND		1st Mate	2nd Mate
	S2	A+	Differential Signal Pair A	2nd Mate	3rd Mate
	S3	A-		2nd Mate	3rd Mate
	S4	GND		1st Mate	2nd Mate
	S5	B-	Differential Signal Pair B	2nd Mate	3rd Mate
	S6	B+		2nd Mate	3rd Mate
	S7	GND		1st Mate	2nd Mate
Signal Segment "L"					
Central Connector Gap[4]					
Power Segment "L"					
Power Segment	P1	Retired[5,6]		2nd Mate	3rd Mate
	P2	Retired[5,6]		2nd Mate	3rd Mate
	P3	DEVSLP~~Retired~~[5]	Enter/Exit DevSleep	1st Mate	2nd Mate
	P4	GND		1st Mate	1st Mate
	P5	GND		1st Mate	2nd Mate
	P6	GND		1st Mate	2nd Mate
	P7	V_5	5 V Power, Pre-charge	1st Mate	2nd Mate
	P8	V_5	5 V Power	2nd Mate	3rd Mate
	P9	V_5	5 V Power	2nd Mate	3rd Mate
	P10	GND		1st Mate	2nd Mate
	P11	DAS/DSS/DHU	Device Activity Signal / Disable Staggered Spinup/ Direct Head Unload / Vendor Specific[1]	2nd Mate	3rd Mate
	P12	GND		1st Mate	1st Mate
	P13	V_{12}	12 V Power, Pre-charge	1st Mate	2nd Mate
	P14	V_{12}	12 V Power	2nd Mate	3rd Mate
	P15	V_{12}	12 V Power	2nd Mate	3rd Mate
Power Segment Key					

NOTE:
1. For specific optional usage of pin P11 see section **Error! Reference source not found.**.
2. Although the mate order is shown, hot plugging is not supported when using the cable connector receptacle.
3. All mate sequences assume zero angular offset between connectors.
4. The signal segment and power segment may be separate.
5. Previous versions of this specification assigned 3.3V to pins P1, P2 and P3. In addition, device plug pins P1, P2, and P3 were required to be bused together.
6. When using DEVSLP, it is recommended to have P1 and P2 tied together for purpose of legacy functionality.