Proposed **Serial ATA**

Draft **International Organization**

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Title: Synch with ACS-3

Proposed changes to Serial ATA Revision 3.1

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Document History

Version	Date	Comments
0	03/06/2012	Initial draft
1	03/14/2012	Included removal of DCO material
2	5/14/2012	1. Included removal of Sense Data Reporting from Software Settings Preservation, 2. added SATA Revision 3.2 to IDENTIFY DEVICE data word 222 3. added SATA Revision 3.1 and 3.2 to IDENTIFY PACKET DEVICE data word 222 4. Replaced the DCO section with a note saying it is obsolete in ACS-3, and to see SATA Revision 3.1 for details, while keeping the subheading (instead of just removing the subheading also)
3	07/17/2012	1. Minor grammar and punctuation comments from Harvey Newman 2. Word 78: a. Defined bit 9 b. added editor notes about which ratified TPRs new bits came from 3. IDENTIFY DEVICE Data Log, Qword starting at byte 8: a. Moved DEVSLEEP_TO_REDUCEDPWRSTATE_CAPABILITY_SUPPORTED from bit 18 to bit 26 b. Shifted bits 19-26 in reaction to the above c. Defined bit 27: DIPM_PRESERVATION_SUPPORTED 4. Added the word ‘bit’ to the end of subsection headings

		5. Synched with the final revision of T13/f12108r2 that T13 approved
4	08/01/2012	1. Globally change 'Reserved for serial ATA' to 'Reserved' 2. Indicate Fixed for some bits in IDENTIFY DEVICE data word 222 3. Limit the global change of "ATA8-ACS" to "ACS-3" to only clauses 2, 4, 10, 11 and 13
5	08/20/2012	1. Update ID word 78 bits 9 and 10 because of ECN D158 2. Added 'F' to IDENTIFY PACKET DEVICE word 222, bit 0 3. Inserted editors notes for unresolved cross references 4. Added clause 12 to the list of clauses for global change from ATA8-ACS to ACS-3 5. Removed redundant 'the device' in subclause 13.7.7.3.3 6. Removed "SATA Revision 3.2" from IDENTIFY DEVICE data word 222 (and IDENTIFY PACKET DEVICE)
6	10/05/2012	Corrections from member review comments 1. IDENTIFY DEVICE a. restored specification of word 76 bit 3 b. renamed word 77 bits (3:1) from "CURRENT SERIAL ATA SIGNAL SPEED" to "CURRENT NEGOTIATED SERIAL ATA SIGNAL SPEED" c. moved word 78 bit 9 to word 78 bit 10, per ECN 065 d. renamed word 78 bit 2 from "DMA SETUP AUTO-ACTIVATION ENABLED" to "DMA SETUP FIS AUTO-ACTIVATE ENABLED" 2. IDENTIFY PACKET DEVICE a. deleted all changes to this command, except for changing ATA8-ACS to ACS-2 3. Identify Device Data log a. moved (qword 8..15, bit 27) to (qword 8..15, bit 28) in anticipation of approval of the Hybrid Information feature b. renamed word (qword 8..15, bit 19) from "DMA SETUP AUTO-ACTIVATION ENABLED" to "DMA SETUP FIS AUTO-ACTIVATE ENABLED" c. DEVSLEEP_TO_REDUCEDPWRSTATE CAPABILITY SUPPORTED bit: changed cross reference from "IDENTIFY DEVICE data word 78 bit 7" to "IDENTIFY DEVICE data word 77 bit 7" d. DIPM SSP PRESERVATION SUPPORTED bit: changed cross reference from "IDENTIFY DEVICE data word 78 bit 9" to "IDENTIFY DEVICE data word 78 bit 10"

7	11/12/2012	Identify Device Data log a. subclause 13.7.7.3.1: change bits (3:0) to (3:1) b. Table 4: change from having separate columns for bits 3, 2, and 1, to having a single column containing one 3-bit value per row Ratified by Digital WG Nov. 12, 2012

1 Introduction

This proposal synchronizes the SATA specification with ACS-3

2 Summary of the problem

T13 periodically adds and removes features.

ACS-3 obsoleted these features:

1. TLC technical report (Time Limited Commands)
2. Device Configuration Overlay feature set (DCO)
3. Host Protected Area feature set (HPA)
4. NV Cache feature set
5. NV Cache Power Management feature set

ACS-3 added these features:

1. IDENTIFY DEVICE data log
2. Accessible Max Address feature set
3. Sanitize Device feature set

3 Proposed corrections

[editor note: Old unmodified text is in black. New text is marked as underlined in blue color. Material to be deleted ~~is red with strikethrough markings.~~]

[editor note: references to SATA Revision 3.1 and to proposals ratified for SATA Revision 3.2 are marked with ‘xxx’. On incorporation, please insert the appropriate cross references.]

[editor note: (global) change all occurrences of “ATA8-ACS” with “ACS-3” in clauses 2, 4, 10, 11, 12 and 13]

4 dummy

5 dummy

6 dummy

7 dummy

8 dummy

9 dummy

10 dummy

11 dummy

12 dummy

13 dummy

13.1 dummy

13.2 IDENTIFY DEVICE

13.2.1 IDENTIFY DEVICE

Table 84 – IDENTIFY DEVICE information

Word	O/M	F/V		
0-46			Set as indicated in ~~ATA8-ACS~~ACS-3	
47	M		Multiple Count	
		F	15-8	80h
		R	7-0	00h = Reserved
				01h-10h = Maximum number of sectors that shall be transferred per interrupt on READ/WRITE MULTIPLE commands
				11h-FFh = Reserved
48			Set as indicated in ~~ATA8-ACS~~ACS-3	
49	M		Capabilities	
			15-12	Set as indicated in ~~ATA8-ACS~~ACS-3
		F	11	Shall be set to one
		F	10	Shall be set to one
			9-0	Set as indicated in ~~ATA8-ACS~~ACS-3
50-52			Set as indicated in ~~ATA8-ACS~~ACS-3	
53	M		Field validity	
		R	15-3	Reserved
		F	2	1=the fields reported in word 88 are valid
				0=the fields reported in word 88 are not valid
		F	1	1=the fields reported in words (70:64) are valid
				0=the fields reported in words (70:64) are not valid
		F	0	Obsolete
54-62			Set as indicated in ~~ATA8-ACS~~ACS-3	
63	M		Multiword DMA transfer	
			15-3	Set as indicated in ~~ATA8-ACS~~ACS-3
		F	2	1= Multiword DMA mode 2 and below are supported
		F	1	1= Multiword DMA mode 1 and below are supported
		F	0	1= Multiword DMA mode 0 is supported
64	M		PIO transfer modes supported	
			15-2	Set as indicated in ~~ATA8-ACS~~ACS-3
		F	1-0	PIO modes 3 and 4 supported

Word	O/M	F/V		
65	M		Minimum Multiword DMA transfer cycle time per word	
		F	15-0	Cycle time in nanoseconds
66	M		Manufacturer's recommended Multiword DMA transfer cycle time	
		F	15-0	Cycle time in nanoseconds
67	M		Minimum PIO transfer cycle time without flow control	
		F	15-0	Cycle time in nanoseconds
68	M		Minimum PIO transfer cycle time with IORDY flow control	
		F	15-0	Cycle time in nanoseconds
69-74			Set as indicated in ~~ATA8-ACS~~ACS-3	
75	O		Queue depth	
		R	15-5	Reserved
		F	4-0	Maximum queue depth - 1
76	O		Serial ATA capabilities	
		F	15	Supports READ LOG DMA EXT as equivalent to READ LOG EXT
		F	14	Supports Device Automatic Partial to Slumber transitions
		F	13	Supports Host Automatic Partial to Slumber transitions
		F	12	Supports Native Command Queuing priority information
		F	11	Supports Unload while NCQ commands outstanding
		F	10	Supports Phy event counters
		F	9	Supports receipt of host-initiated interface power management requests
		F	8	Supports Native Command Queuing
		R	7-4	Reserved for future Serial ATA signaling speed grades
		F	3	1 = Supports Serial ATA Gen3 signaling speed (6.0 Gbps)
		F	2	1 = Supports Serial ATA Gen2 signaling speed (3.0 Gbps)
		F	1	1 = Supports Serial ATA Gen1 signaling speed (1.5 Gbps)
		F	0	Shall be cleared to zero
77	O			Serial ATA Additional capabilities
		R	15-~~7~~8	Reserved
		F	7	~~Reserved~~ Supports DevSleep to reduced power state capability [editors note: added in TPR038]
		F	6	Supports RECEIVE FPDMA QUEUED and SEND FPDMA QUEUED commands
		F	5	Supports NCQ Queue Management Command

Word	O/M	F/V		
		F	4	Supports NCQ Streaming
		V	3-1	Coded value indicating current negotiated Serial ATA signal speed
		F	0	Shall be cleared to zero
78	O		Serial ATA features supported	
		R	15-~~8~~11	Reserved
		F	10	1 = Device Supports Device Initiated Interface Power Management Software Settings Preservation [editors note: added in TPR040, modified in ECN D158]
			9	Reserved
		F	8	1 = Supports Device Sleep [editors note: added in TPR038]
		F	7	1 = Supports NCQ Autosense
		F	6	1 = Supports software settings preservation
		F	5	1 = Hardware Feature Control is supported
		F	4	1 = Supports in-order data delivery
		F	3	1 = Device supports initiating interface power management
		F	2	1 = Supports DMA Setup Auto-Activate optimization
		F	1	1 = Supports non-zero buffer offsets in DMA Setup FIS
		F	0	Shall be cleared to zero
79	O		Serial ATA features enabled	
		R	15-~~8~~9	Reserved
		V	8	1 = Device Sleep Enabled [editors note: added in TPR038]
		V	7	1 = Device Automatic Partial to Slumber transitions enabled
		V	6	1 = Software settings preservation enabled
		V	5	1 = Hardware Feature Control is enabled
		V	4	1 = In-order data delivery enabled
		V	3	1 = Device initiating interface power management enabled
		V	2	1 = DMA Setup Auto-Activate optimization enabled
		V	1	1 = Non-zero buffer offsets in DMA Setup FIS enabled
		F	0	Shall be cleared to zero
80-87			Set as indicated in ~~ATA8-ACS~~ACS-3	
88			15-6	Set as indicated in ~~ATA8-ACS~~ACS-3

Word	O/M	F/V	
		F	5 1=Ultra DMA mode 5 and below are supported
		F	4 1=Ultra DMA mode 4 and below are supported
		F	3 1=Ultra DMA mode 3 and below are supported
		F	2 1=Ultra DMA mode 2 and below are supported
		F	1 1=Ultra DMA mode 1 and below are supported
		F	0 1=Ultra DMA mode 0 is supported
89-92			Set as indicated in ~~ATA8-ACS~~ACS-3
93		V	COMRESET result. The contents of this word shall be cleared to zero.
94-221			Set as indicated in ~~ATA8-ACS~~ACS-3
222			Transport Major Revision 0000h or FFFFh = device does not report version **Bits** **Description** F 15:12 Transport Type 0h = Parallel 1h = Serial 2h - Fh = Reserved R 11:7 Reserved F 6 SATA Rev 3.1 F 5 SATA Rev 3.0 F 4 SATA Rev 2.6 F 3 SATA Rev 2.5 F 2 SATA II: Extensions F 1 SATA 1.0a F 0 ATA8-AST
223		F	Transport Minor Revision
224-255			Set as indicated in ~~ATA8-ACS~~ACS-3

Key:

M = Support of the word is mandatory.

O = Support of the word is optional.

F = the content of the word is fixed and does not change. For removable media devices, these values may change when media is removed or changed.

V = the contents of the word is variable and may change depending on the state of the device or the commands executed by the device.

X = the content of the word is vendor specific and may be fixed or variable.

R = the content of the word is reserved and shall be zero.

13.2.1.1 Word 0 - 46: Set as indicated in ~~ATA8-ACS~~ACS-3

13.2.1.2 Word 47: Multiword PIO transfer

Bits 15 through 8 of word 47 shall be set as indicated in ~~ATA8-ACS~~ACS-3.

Bits 7 through 0 are used to indicate the maximum number of sectors that shall be transferred per interrupt on READ/WRITE MULTIPLE commands. This field shall be set to 16 or less. See section Editor's note 10.3.10.1.

13.2.1.3 Word 48: Set as indicated in ~~ATA8-ACS~~ACS-3

13.2.1.4 Word 49: Capabilities

Bits 15 through 12 of word 49 shall be set as indicated in ~~ATA8-ACS~~ACS-3.

Bit 11 of word 49 is used to determine whether a device supports IORDY. This bit shall be set to one, indicating the device supports IORDY operation.

Bit 10 of word 49 is used to indicate a device's ability to enable or disable the use of IORDY. This bit shall be set to one, indicating the device supports the disabling of IORDY. Disabling and enabling of IORDY is accomplished using the SET FEATURES command.

Bits 9 - 0 of word 49 shall be set as indicated in ~~ATA8-ACS~~ACS-3.

13.2.1.5 Words 50 - 52: Set as indicated in ~~ATA8-ACS~~ACS-3

13.2.1.6 Word 53: Field validity

Bit 0 shall be set to one. Bit 1 of word 53 shall be set to one, the values reported in words 64 through 70 are valid. Any device that supports PIO mode 3 or above, or supports Multiword DMA mode 1 or above, shall set bit 1 of word 53 to one and support the fields contained in words 64 through 70. Bit 2 of word 53 shall be set to one indicating the device supports Ultra DMA and the values reported in word 88 are valid. Bits 15-3 are reserved.

13.2.1.7 Word 54 - 62: Set as indicated in ~~ATA8-ACS~~ACS-3

13.2.1.8 Word 63: Multiword DMA transfer

Bits 2 - 0 of word 63 shall be set to one indicating that the device supports Multiword DMA modes 0, 1, and 2. Bits 15 – 3 shall be set as indicated in ~~ATA8-ACS~~ACS-3.

13.2.1.9 Word 64: PIO transfer modes supported

Bits 1 - 0 of word 64 shall be set to one indicating that the device supports PIO modes 3 and 4. Bits 15 – 2 shall be set as indicated in ~~ATA8-ACS~~ACS-3.

13.2.1.10 Word 65: Minimum Multiword DMA transfer cycle time per word

Shall be set to indicate 120 ns.

13.2.1.11 Word 66: Device recommended Multiword DMA cycle time

Shall be set to indicate 120 ns.

13.2.1.12 Word 67: Minimum PIO transfer cycle time without flow control

Shall be set to indicate 120 ns.

13.2.1.13 Word 68: Minimum PIO transfer cycle time with IORDY

Shall be set to indicate 120 ns.

13.2.1.14 Words 69-74: Set as indicated in ~~ATA8-ACS~~ACS-3

13.2.1.15 Word 75: Queue depth

This word is as defined in the ~~ATA8-ACS~~ACS-3 standard. The Native Command Queuing protocol supports at most 32 queued commands. With Native Command Queueing, the host shall issue only unique tag values for queued commands that have a value less than or equal to the value reflected in this field (e.g., for device reporting a value in this field of 15, corresponding to a maximum of 16 outstanding commands, the host shall never use a tag value greater than 15 when issuing Native Command Queueing commands).

13.2.1.16 Word 76: Serial ATA capabilities

If not 0000h or FFFFh, the device claims compliance with the Serial ATA specification and supports the signaling speed indicated in bits 1-3. Since Serial ATA supports generational compatibility, multiple bits may be set. Bit 0 is reserved and shall be cleared to zero (thus a Serial ATA device has at least one bit cleared in this field and at least one bit set providing clear differentiation). If this field is not 0000h or FFFFh, words 77 through 79 shall be valid. If this field is 0000h or FFFFh the device does not claim compliance with the Serial ATA specification and Words 76 through 79 are not valid and shall be ignored.

Bit 15 is a copy of READ LOG DMA EXT AS EQUIVALENT TO READ LOG EXT SUPPORTED (see 13.7.7.2.11).

Bit 14 is a copy of DEVICE AUTOMATIC PARTIAL TO SLUMBER TRANSITIONS SUPPORTED (see 13.7.7.2.10).

Bit 13 is a copy of HOST AUTOMATIC PARTIAL TO SLUMBER TRANSITIONS SUPPORTED (see 13.7.7.2.9).

Bit 12 is a copy of NCQ PRIORITY INFORMATION SUPPORTED (see 13.7.7.2.8).

Bit 11 is a copy of UNLOAD WHILE NCQ COMMANDS ARE OUTSTANDING SUPPORTED (see 13.7.7.2.7).

Bit 10 is a copy of SATA PHY EVENT COUNTERS LOG SUPPORTED (see 13.7.7.2.6).

Bit 9 is a copy of RECEIPT OF HOST INITIATED POWER MANAGEMENT REQUESTS SUPPORTED (see 13.7.7.2.5).

Bit 8 is a copy of NCQ FEATURE SET SUPPORTED (see 13.7.7.2.4).

Bits (7:4) are reserved~~ for Serial ATA~~.

Bit 3 is a copy of SATA GEN3 SIGNALING SPEED SUPPORTED (see 13.7.7.2.3).

Bit 2 is a copy of SATA GEN2 SIGNALING SPEED SUPPORTED (see 13.7.7.2.2).

Bit 1 is a copy of SATA GEN1 SIGNALING SPEED SUPPORTED (see 13.7.7.2.1).

Bit 0 shall be cleared to zero.

~~Bit 1 when set to one indicates that the device is a Serial ATA device and supports the Gen1 signaling speed of 1.5 Gbps. See 7.4.26.1.2..~~

~~Bit 2 when set to one indicates that the device is a Serial ATA device and supports the Gen2 signaling speed of 3.0 Gbps. See 7.4.26.1.2..~~

~~Bit 3 when set to one indicates that the device is a Serial ATA device and supports the Gen3 signaling speed of 6.0 Gbps. See 7.4.26.1.2.~~

~~Bit 4-7 are reserved for future Serial ATA signaling speed grades and shall be cleared to zero.~~

~~Bit 8 when set to one indicates that the Serial ATA device supports the Native Command Queuing scheme defined in section **Error! Reference source not found.**.~~

~~Bit 9 when set to one indicates that the Serial ATA device supports the Partial and Slumber interface power management states when initiated by the host.~~

~~Bit 10 when set to one indicates that the Serial ATA device supports Phy event counters. If the device supports Phy event counters, it shall support the Phy Event Counter Log (see **Error! Reference source not found.**)~~

~~Bit 11 when set to one indicates that the device supports performing an unload/park of the heads upon reception of the IDLE IMMEDIATE command with the Unload Feature specified while NCQ commands are outstanding. This bit shall only be set to one if the device supports NCQ as shown in bit 8 of Word 76.~~

~~Bit 12 when set to one indicates that the device supports the Priority field in the READ FPDMA QUEUED and WRITE FPDMA QUEUED commands and optimization based on this information. This bit shall only be set to one if the device supports NCQ as shown in bit 8 of Word 76.~~

~~Bit 13 indicates that the device supports host Automatic Partial to Slumber transitions. The device shall tolerate a Partial exit latency up to the max Slumber exit latency. This allows the host to asynchronously transition from Partial to Slumber.~~

~~If Word 76, bit 9 (supports receipt of host-initiated interface power management requests) is cleared to zero, then bit 13 shall be cleared to zero.~~

~~Bit 14 indicates that the device supports Automatic Partial to Slumber transitions and may asynchronously transition from Partial to Slumber when enabled.~~

~~If Word 78, bit 3 (supports initiating interface power management) is cleared to zero, then Word 76 bit 14 shall be cleared to zero.~~

~~Bit 15 when set to one indicates that either the READ LOG DMA EXT and READ LOG EXT commands may be used in all cases with identical results (see **Error! Reference source not found.**). If IDENTIFY DEVICE word 119 bit 3 is cleared to zero, this bit shall be cleared to zero. If bit 15 is cleared to zero and the host issues the READ LOG DMA EXT command to read the Queued Error Log or the Phy Event Counters log, the device shall return command aborted.~~

13.2.1.17 Word 77: Serial ATA Additional capabilities

Word 77 reports additional optional capabilities supported by the device. Support for this word is optional and if not supported, the word shall be zero indicating the device has no support for additional Serial ATA capabilities.

Bits 15:8 are reserved and shall be cleared to zero.

Bit 7 is a copy of DEVSLEEP_TO_REDUCEDPWRSTATE CAPABILITY SUPPORTED (see 13.7.7.2.23).

Bit 6 is a copy of SEND AND RECEIVE QUEUED COMMANDS SUPPORTED (see 13.7.7.2.14).

Bit 5 is a copy of NCQ QUEUE MANAGEMENT COMMAND SUPPORTED (see 13.7.7.2.13).

Bit 4 is a copy of NCQ STREAMING SUPPORTED (see 13.7.7.2.12).

Bits (3:1) are a copy of CURRENT NEGOTIATED SERIAL ATA SIGNAL SPEED (see 13.7.7.3.1).

Bit 0 shall be cleared to zero

~~Bits 1-3 are a coded value that indicates the Serial ATA Phy speed at which the device is currently communicating. Table 1 defines these values:~~

~~Coded Values~~	~~Description~~

Bit 3	Bit 2	Bit 1	
0	0	0	Signaling speed is not reported
0	0	1	Gen1 signaling speed of 1.5 Gbps
0	1	0	Gen2 signaling speed of 3.0 Gbps
0	1	1	Gen3 signaling speed of 6.0 Gbps
All Non-Defined Values			Reserved for future Serial ATA signaling speeds

Table 1 - Coded Values for Negotiated Serial ATA Signaling Speed

Note: In the case of system configurations that have more than one Phy link in the data path (eg. port multiplier), the indicated speed is only relevant for the link between the device Phy and its immediate host Phy. It is possible for each link in the data path to negotiate a different Serial ATA signaling speed.

Bit 4, when set to one, indicates that the device supports NCQ Streaming. See the use of the ICC field by the READ FPDMA QUEUED and WRITE FPDMA QUEUED commands. This bit shall only be set to one if the device supports NCQ as shown in bit 8 of Word 76.

Bit 5, when set to one indicates that the device supports use of the NCQ QUEUE MANAGEMENT command by the host. This bit shall only be set to one if the device supports NCQ as shown in bit 8 of Word 76.

Bit 7-15 are reserved and shall be cleared to zero

13.2.1.18 Word 78: Serial ATA features supported

Word 78 reports the optional features supported by the device. Support for this word is optional and if not supported the word shall be zero indicating the device has no support for new Serial ATA capabilities.

Bits 15:11 are reserved and shall be cleared to zero.

Bit 10 is a copy of DIPM SSP PRESERVATION SUPPORTED (see 13.7.7.2.24)

Bit 9 is reserved and shall be cleared to zero.

Bit 8 is a copy of DEVICE SLEEP SUPPORTED (see 13.7.7.2.22).

Bit 7 is a copy of NCQ AUTOSENSE SUPPORTED (see 13.7.7.2.21).

Bit 6 is a copy of SOFTWARE SETTINGS PRESERVATION SUPPORTED (see 13.7.7.2.20).

Bit 5 is a copy of HARDWARE FEATURE CONTROL SUPPORTED (see 13.7.7.2.19).

Bit 4 is a copy of IN-ORDER DATA DELIVERY SUPPORTED (see 13.7.7.2.18).

Bit 3 is a copy of DEVICE INITIATED POWER MANAGEMENT SUPPORTED (see 13.7.7.2.17).

Bit 2 is a copy of DMA SETUP AUTO-ACTIVATION SUPPORTED (see 13.7.7.2.16).

Bit 1 is a copy of NON-ZERO BUFFER OFFSETS SUPPORTED (see 13.7.7.2.15).

Bit 0 shall be cleared to zero.

Bit 1 indicates whether the device supports the use of non-zero buffer offsets in the DMA Setup FIS. When set to one, the device supports transmission and reception of DMA Setup FISes with a non-zero value in the Buffer Offset field of the FIS. When cleared to zero, the device supports transmission and reception of the DMA Setup FIS only with the Buffer Offset field cleared to zero.

Bit 2 indicates whether the device supports the use of the DMA Setup FIS Auto-Activate optimization as described in section **Error! Reference source not found.**. When set to one the

~~device supports use of the Auto-Activate optimization and when cleared to zero the device does not support the Auto-Activate optimization.~~

~~Bit 3 indicates whether the device supports initiating power management requests to the host. When set to one the device supports initiating interface power management requests and when cleared to zero the device does not support initiating power management requests. A device may support reception of power management requests initiated by the host as described in the definition of bit 9 of Word 76 without supporting initiating such power management requests as indicated by this bit.~~

~~Bit 4 indicates whether the device supports guaranteed in-order data delivery when non-zero buffer offsets are used in the DMA Setup FIS. When set to one, the device guarantees in-order data delivery for READ FPDMA QUEUED or WRITE FPDMA QUEUED commands when non-zero buffer offsets are used with multiple DMA Setup FIS. Target data is delivered in order, starting with the first LBA through command completion. When Bit 4 is cleared to zero, the device does not guarantee in-order data delivery when non-zero buffer offsets are enabled. In this case, data may be interleaved both within a command and across multiple commands. By default this field shall be zero.~~

~~Bit 5 is reserved and shall be cleared to zero.~~

~~Bit 6 indicates whether the device supports software settings preservation as defined in section **Error! Reference source not found.**. When set to one the device supports software settings preservation across COMRESET. When cleared to zero the device clears all software settings when a COMRESET occurs.~~

~~Bit 8 indicates whether the device supports the Device Sleep feature (see 8.5).~~

~~If set to one:~~

~~a) the device supports the Device Sleep feature;~~

~~b) the device shall support the Identify Device data log; and~~

~~c) the DEVSLP Timing Variables field Valid bit shall be set to 1.~~

~~If cleared to zero, the device does not support the Device Sleep feature.~~

~~Bit 9 indicates that the device supports persistence of the Device Initiated Interface Power Management enable/disable setting via Software Settings Preservation.~~

~~Bit 10-15 are reserved and shall be cleared to zero~~

13.2.1.19 Word 79: Serial ATA features enabled

Word 79 reports which optional features supported by the device are enabled. This word shall be supported if optional Word 78 is supported and shall not be supported if optional Word 78 is not supported.

Bits 15:9 are reserved and shall be cleared to zero.

Bit 8 is a copy of DEVICE SLEEP ENABLED (see 13.7.7.3.9).

Bit 7 is a copy of AUTOMATIC PARTIAL TO SLUMBER TRANSITIONS ENABLED (see 13.7.7.3.8).

Bit 6 is a copy of SOFTWARE SETTINGS PRESERVATION ENABLED (see 13.7.7.3.7).

Bit 5 is a copy of HARDWARE FEATURE CONTROL IS ENABLED (see 13.7.7.3.6).

Bit 4 is a copy of IN-ORDER DATA DELIVERY ENABLED (see 13.7.7.3.5).

Bit 3 is a copy of DEVICE INITIATED POWER MANAGEMENT ENABLED (see 13.7.7.3.4).

Bit 2 is a copy of DMA SETUP FIS AUTO-ACTIVATE ENABLED (see 13.7.7.3.3).

Bit 1 is a copy of NON-ZERO BUFFER OFFSETS ENABLED (see 13.7.7.3.2).

Bit 0 shall be cleared to zero.

~~Bit 1 indicates whether device support for use of non-zero buffer offsets in the DMA Setup FIS is enabled. When set to one, device transmission of DMA Setup FISes with a non-zero value in the Buffer Offset field of the FIS is enabled. When cleared to zero, the device is permitted to transmit DMA Setup FIS only with the Buffer Offset field cleared to zero. By default this field shall be zero.~~

~~Bit 2 indicates whether device support for use of the DMA Setup FIS Auto-Activate optimization as described in section **Error! Reference source not found.** is enabled. When set to one, the device may utilize the Auto-Activate optimization. When cleared to zero the device shall not utilize the Auto-Activate optimization. By default, this field shall be zero.~~

~~Bit 3 indicates whether device support for initiating power management requests to the host is enabled. When set to one the device may initiate power management transition requests. When cleared to zero the device shall not initiate interface power management requests to the host. This field shall be zero by default.~~

~~Bit 4 indicates whether device support for guaranteed in-order data delivery when non-zero buffer offsets are used in the DMA Setup FIS is enabled. When set to one and non-zero buffer offset is enabled, the device may satisfy a READ FPDMA QUEUED or WRITE FPDMA QUEUED command by transmitting multiple DMA Setup FISes with non-zero buffer offset values where appropriate, provided that the target data is delivered in order, starting with the first LBA through command completion. When Bit 4 is cleared to zero, the device may interleave data both in a command and across multiple commands using non-zero buffer offsets if non-zero buffer offsets are enabled. By default this field shall be zero.~~

~~Bit 5 is reserved and shall be cleared to zero.~~

~~Bit 6 indicates whether device support for software settings preservation is enabled. When set to one the device shall preserve software settings across COMRESET. When cleared to zero the device shall clear software settings when COMRESET occurs. If the device supports software settings preservation this field shall be one by default. If the device does not support software settings preservation this field shall be zero by default.~~

~~Bit 7 indicates whether or not device Automatic Partial to Slumber transitions are enabled. When enabled the device may asynchronously transition from Partial to Slumber. If Word 76, bit 14 (Supports Device Automatic Partial to Slumber transitions) is cleared to zero, then bit 7 shall be cleared to zero. If Word 79, bit 3 (Device initiating interface power management enabled) is cleared to zero, then bit 7 shall be cleared to zero.~~

~~Bit 8 indicates whether or not the Device Sleep feature is enabled (see 13.3.10). If set to one, the Device Sleep feature is enabled. If cleared to zero, the Device Sleep feature is disabled.~~

~~Bits 9-15 are reserved and shall be cleared to zero.~~

13.2.1.20 Words 80-87: Set as indicated in ~~ATA8-ACS~~ACS-3

13.2.1.21 Word 88: Ultra DMA modes

Bits 5 - 0 of Word 88 shall be set to one indicating that the device supports Ultra DMA modes 0, 1, 2, 3, 4, and 5. Bits 15 – 5 shall be set as indicated in ~~ATA8-ACS~~ACS-3.

13.2.1.22 Words 89 - 92: Set as indicated in ~~ATA8-ACS~~ACS-3

13.2.1.23 Word 93: Hardware configuration test results

Word 93 shall be set to 0000h indicating that the word is not supported.

13.2.1.24 Words 94-221: Set as indicated in ~~ATA8-ACS~~ACS-3.

13.2.1.25 Word 222: Transport Major Revision

Bits (15:12) shall be set to 1h.

13.2.1.26 Word 223: Transport Minor Revision

Set as indicated in ~~ATA8-ACS~~ACS-3.

13.2.1.27 Words 224-255:

Set as indicated in ~~ATA8-ACS~~ACS-3.

13.2.2 IDENTIFY PACKET DEVICE

[editors note: make no changes other than the global changes mentioned above]

13.3 dummy

13.4 Device Configuration Overlay

[editors note: replace all of subclause 13.4 with the following]

For information on the Device Configuration Overlay feature set and commands, see SATA Revision 3.1. The feature set is obsolete in ACS-3.

~~13.4.1 Device Configuration Overlay Identify~~

~~Figure 1 defines additional features and capabilities that support may be controlled for using the DEVICE CONFIGURATION IDENTIFY command in the ATA8-ACS standard. The device is only required to support setting these features if the device reports support for Device Configuration Overlay in either IDENTIFY DEVICE or IDENTIFY PACKET DEVICE, respectively.~~

Word	Description
0-7	As defined in the ATA8-ACS standard
8	Serial ATA command / feature sets supported 15-8 Reserved 7 1 = Reporting support for RECEIVE FPDMA QUEUED[1], and SEND FPDMA QUEUED[1] is changeable 6 1 = Reporting support for NCQ QUEUE MANAGEMENT[1] is changeable 5 1 = Reporting support for Automatic Partial to Slumber transitions is changeable 4 1 = Reporting support for software settings preservation is changeable 3 1 = Reporting support for asynchronous notification is changeable 2 1 = Reporting support for interface power management is changeable 1 1 = Reporting support for non-zero buffer offsets in DMA Setup FIS[1] is changeable 0 1 = Reporting support for Native Command Queuing[1] is changeable
9	Reserved for Serial ATA
10-255	As defined in the ATA8-ACS standard
NOTE: 1. Applicable to non-PACKET devices only – i.e. IDENTIFY DEVICE.	

Figure 1 - DEVICE CONFIGURATION IDENTIFY data structure

WORD 8: Serial ATA command / feature sets supported

This word describes which features for which support is changeable. A feature may be supported but not be changeable. If bit 0 of word 8 is set to one, then support for Native Command Queuing is changeable. The setting of this bit is applicable to non-PACKET devices only.

If bit 1 of word 8 is set to one, then support for non-zero buffer offsets in the DMA Setup FIS is changeable. The setting of this bit is applicable to non-PACKET devices only.

If bit 2 of word 8 is set to one, then suport receiving host initiated power management requests and/or sending device initiated power management requests is changeable.

If bit 3 of word 8 is set to one, then support for asynchronous notification is changeable.

If bit 4 of word 8 is set to one, then support for software settings preservation is changeable.

If bit 5 of word 8 is set to one, then support for Automatic Partial to Slumber transitions is changeable.

If bit 6 of word 8 is set to one, then support for the NCQ QUEUE MANAGEMENT command is changeable. The setting of this bit is applicable to non-PACKET devices only.

If bit 7 of Word 8 is set to one, then support for RECEIVE FPDMA QUEUED, and SEND FPDMA QUEUED is changeable. The setting of this bit is applicable to non-PACKET devices only.

Bits 87-15 are reserved and shall be cleared to zero.

WORD 9: Reserved for Serial ATA

This word is reserved for Serial ATA and all bits shall be cleared to zero.

13.4.2 Device Configuration Overlay Set

Figure 2 defines additional features and capabilities that support may be controlled for using the DEVICE CONFIGURATION SET command in the ATA8-ACS standard. The device is only required to support setting these features if the device reports support for Device Configuration Overlay in either IDENTIFY DEVICE or IDENTIFY PACKET DEVICE, respectively.

Word	Description
0-7	As defined in the ATA8-ACS standard
8	Serial ATA command / feature sets supported 15-8 Reserved 7 1 = Reporting support for RECEIVE FPDMA QUEUED[1], and SEND FPDMA QUEUED[1] is allowed 6 1 = Reporting support for the NCQ QUEUE MANAGEMENT command[1] is allowed 5 1 = Reporting support for Automatic Partial to Slumber transitions is allowed 4 1 = Reporting support for software settings preservation is allowed 3 1 = Reporting support for asynchronous notification is allowed 2 1 = Reporting support for interface power management is allowed 1 1 = Reporting support for non-zero buffer offsets in DMA Setup FIS[1] is allowed 0 1 = Reporting support for Native Command Queuing[1] is allowed
9	Reserved for Serial ATA
10-255	As defined in the ATA8-ACS standard
NOTE: 1. Applicable to non-PACKET devices only – i.e. IDENTIFY DEVICE.	

Figure 2 - DEVICE CONFIGURATION SET data structure

WORD 8: Serial ATA command / feature sets supported

This word enables configuration of command sets and feature sets.

If bit 0 of word 8 is cleared to zero, then the device shall:

a) disable support for Native Command Queuing;
b) clear word 76 bits 8,11,and 12 in the IDENTIFY DEVICE data to zero;
c) clear word 77, bits 4 and 5 in the IDENTIFY DEVICE data to zero;
d) clear word 78 bits 1, 2, and 4 in the IDENTIFY DEVICE data to zero;
e) clear word 79 bits 1, 2 and 4 in the IDENTIFY DEVICE data to zero; and
f) if NCQ is disabled and READ FPDMA QUEUED, WRITE FPDMA QUEUED, NCQ QUEUE MANAGEMENT, SEND FPDMA QUEUED, or RECEIVE FPDMA QUEUED is issued to the device, the device shall abort the command with the ERR bit set to one in the Status field and the ABRT bit set to one in the Error field.

The setting of this bit is applicable to non-PACKET devices only.

If bit 1 of word 8 is cleared to zero, then the device shall

a) disable support for non-zero buffer offsets in the DMA Setup FIS;
b) clear word 78 bits 1 and 4 in the IDENTIFY DEVICE data to zero;
c) clear word 79 bits 1 and 4in the in the IDENTIFY DEVICE data to zero; and
d) if non-zero buffer offsets in the DMA Setup FIS are disabled, the device shall only issue a DMA Setup FIS that has the DMA Buffer Offset field cleared to zero.

The setting of this bit is applicable to non-PACKET devices only.

If bit 2 of word 8 is cleared to zero, then the device shall:

a) disable support for receiving host initiated power management requests and shall not support device initiated power management requests;
b) clear word 76 bits 9, 13 and 14 of IDENTIFY DEVICE or IDENTIFY PACKET DEVICE data to zero;
c) clear word 78 bit 3 of IDENTIFY DEVICE or IDENTIFY PACKET DEVICE data to zero;
d) clear word 79 bits 3 and 7 of IDENTIFY DEVICE or IDENTIFY PACKET DEVICE data to zero; and
e) if interface power management requests are disabled, the device shall respond with $PMNAK_P$ to any interface power management requests and the device shall not issue $PMREQ\_P_P$ or $PMREQ\_S_P$ to the host.

If bit 3 of word 8 is cleared to zero, then the device shall:

a) disable support for asynchronous notification;
b) clear word 78 bit 5 of IDENTIFY PACKET DEVICE data to zero;
c) clear word 79 bit 5 of IDENTIFY PACKET DEVICE data to zero; and
d) when asynchronous notification is disabled, the device shall not initiate a Set Device Bits FIS with the Notification bit set to one.

If bit 4 of word 8 is cleared to zero, then the device shall:

a) disable support for software settings preservation;
b) clear word 78 bit 6 of IDENTIFY DEVICE or IDENTIFY PACKET DEVICE data to zero;
c) clear word 79 bit 6 of IDENTIFY DEVICE or IDENTIFY PACKET DEVICE data to zero; and
d) when software settings preservation is disabled, the device shall not preserve any software settings that are normally cleared following a COMRESET.

If bit 5 of word 8 is cleared to zero, then the device shall:

a) disable support for Automatic Partial to Slumber transitions;
b) clear word 76 bits 13 and 14 of IDENTIFY DEVICE or IDENTIFY PACKET DEVICE data to zero;
c) clear word 79 bit 7 of IDENTIFY DEVICE or IDENTIFY PACKET DEVICE data to zero; and
d) when Automatic Partial to Slumber transitions are disabled neither the device nor host may transition to Slumber from Partial without first entering Active.

If bit 5 of word 8 is set to one and bit 2 or word 8 is cleared to zero, then the device shall return command aborted.

If bit 6 of word 8 is cleared to zero, then the device shall:

a) disable support for the NCQ QUEUE MANAGEMENT command;
b) clear word 77 bit 5 of IDENTIFY DEVICE data to zero; and
c) if an NCQ QUEUE MANAGEMENT command is issued to the device, the device shall return command aborted.

If bit 6 of word 8 is set to one and bit 0 of word 8 is cleared to zero, then the device shall return command aborted.

If bit 7 of word 8 is cleared to zero, then the device shall:

a) disable support for RECEIVE FPDMA QUEUED and SEND FPDMA QUEUED
b) Clear word 77 bit 7 of IDENTIFY DEVICE data to zero; and
c) If any RECEIVE FPDMA QUEUED and/or SEND FPDMA QUEUED commands are issued to the device, the device shall return command aborted.

The setting of bit 7 of word 8 is applicable to non-PACKET devices only.

Bits (15:8) of word 8 are reserved and shall be cleared to zero.

WORD 9: Reserved for Serial ATA

This word is reserved for Serial ATA and all bits shall be cleared to zero.

13.5 Software Settings Preservation

[editors note: only remove the redlined material from this section]

SET MULTIPLE MODE: The block size established with the SET MULTIPLE MODE command.

~~SET FEATURES (Sense Data Reporting Enable/Disable): The enable/disable setting established by the SET FEATURES command with subcommand code of C3h.~~

Write-Read-Verify feature set: The contents of IDENTIFY DEVICE data word 120 bit 1, words 210-211, and word 220 bits (7:0). The device shall not return to its Write-Read-Verify factory default setting after processing a COMRESET.

13.6 dummy

13.7 SATA Logs

13.7.1 dummy

13.7.2 dummy

13.7.3 dummy

13.7.4 dummy

13.7.5 dummy

13.7.6 dummy

13.7.7 Identify Device Data Log (30h)

[editor note: replace all of subclause 13.7.7.1 Serial ATA Settings (page 08h) with the following]

13.7.7.1 Serial ATA Settings (page 08h)

13.7.7.1.1 Overview

The Serial ATA log page (see Table 2) provides information about the Serial ATA Transport.

Table 2 - Serial ATA (page 08h)

Offset	Type	Content
0..7	QWord	Serial ATA page information header.
		Bit **Meaning** 63 Shall be set to one. 62:24 Reserved 23:16 Page Number. Shall be set to 08h. 15:0 Revision number. Shall be set to 0001h
8..15	QWord	SATA Capabilities
		Bit **Meaning** 63 Shall be set to one 62:29 Reserved 28 DIPM SSP PRESERVATION SUPPORTED (see 13.7.7.2.24) 27 Reserved 26 DEVSLEEP_TO_REDUCEDPWRSTATE CAPABILITY SUPPORTED (see 13.7.7.2.23) 25 DEVICE SLEEP SUPPORTED (see 13.7.7.2.22) 24 NCQ AUTOSENSE SUPPORTED (see 13.7.7.2.21) 23 SOFTWARE SETTINGS PRESERVATION SUPPORTED (see 13.7.7.2.20) 22 HARDWARE FEATURE CONTROL SUPPORTED (see 13.7.7.2.19) 21 IN-ORDER DATA DELIVERY SUPPORTED (see 13.7.7.2.18) 20 DEVICE INITIATED POWER MANAGEMENT SUPPORTED (see 13.7.7.2.17) 19 DMA SETUP FIS AUTO-ACTIVATE SUPPORTED (see 13.7.7.2.16)

		18 NON-ZERO BUFFER OFFSETS SUPPORTED (see 13.7.7.2.15) 17 SEND AND RECEIVE QUEUED COMMANDS SUPPORTED (see 13.7.7.2.14) 16 NCQ QUEUE MANAGEMENT COMMAND SUPPORTED (see 13.7.7.2.13) 15 NCQ STREAMING SUPPORTED (see 13.7.7.2.12) 14 READ LOG DMA EXT AS EQUIVALENT TO READ LOG EXT SUPPORTED (see 13.7.7.2.11) 13 DEVICE AUTOMATIC PARTIAL TO SLUMBER TRANSITIONS SUPPORTED (see 13.7.7.2.10) 12 HOST AUTOMATIC PARTIAL TO SLUMBER TRANSITIONS SUPPORTED (see 13.7.7.2.9) 11 NCQ PRIORITY INFORMATION SUPPORTED (see 13.7.7.2.8) 10 UNLOAD WHILE NCQ COMMANDS ARE OUTSTANDING SUPPORTED (see 13.7.7.2.7) 9 SATA PHY EVENT COUNTERS LOG SUPPORTED (see 13.7.7.2.6) 8 RECEIPT OF HOST INITIATED POWER MANAGEMENT REQUESTS SUPPORTED (see 13.7.7.2.5) 7 NCQ FEATURE SET SUPPORTED (see 13.7.7.2.4) 6:3 Reserved ~~for Serial ATA~~ 2 SATA GEN3 SIGNALING SPEED SUPPORTED (see 13.7.7.2.3) 1 SATA GEN2 SIGNALING SPEED SUPPORTED (see 13.7.7.2.2) 0 SATA GEN1 SIGNALING SPEED SUPPORTED (see 13.7.7.2.1)
16..23	QWord	Current SATA Settings
		Bit **Meaning** 63 Shall be set to one 62:11 Reserved ~~for Serial ATA~~ 10 DEVICE SLEEP ENABLED (see 13.7.7.3.9) 9 AUTOMATIC PARTIAL TO SLUMBER TRANSITIONS ENABLED (see 13.7.7.3.8) 8 SOFTWARE SETTINGS PRESERVATION ENABLED (see 13.7.7.3.7) 7 HARDWARE FEATURE CONTROL IS ENABLED (see 13.7.7.3.6) 6 IN-ORDER DATA DELIVERY ENABLED (see 13.7.7.3.5) 5 DEVICE INITIATED POWER MANAGEMENT ENABLED (see 13.7.7.3.4) 4 DMA SETUP AUTO-ACTIVATION ENABLED (see 13.7.7.3.3)

		3 NON-ZERO BUFFER OFFSETS ENABLED (see 13.7.7.3.2) 2:0 CURRENT NEGOTIATED SERIAL ATA SIGNAL SPEED (see 13.7.7.3.1)
24..39		Reserved ~~for Serial ATA~~
40..41	Word	CURRENT HARDWARE FEATURE CONTROL IDENTIFIER (see 13.7.7.3.10)
42..43	Word	SUPPORTED HARDWARE FEATURE CONTROL IDENTIFIER (see 13.7.7.3.11)
44..47		Reserved ~~for Serial ATA~~
48..55	QWord	DEVSLP TIMING VARIABLES **Bit** **Meaning** 63 Shall be set to one 62:16 Reserved ~~for Serial ATA~~ 15:8 DEVSLEEP EXIT TIMEOUT (DETO) (see 13.7.7.4.1) 7:5 Reserved ~~for Serial ATA~~ 4:0 MINIMUM DEVSLP ASSERTION TIME (MDAT) (see 13.7.7.4.2)
56..511		Reserved ~~for Serial ATA~~

13.7.7.2 SATA Capabilities

13.7.7.2.1 SATA GEN1 SIGNALING SPEED SUPPORTED bit

If the SATA GEN1 SIGNALLING SPEED SUPPORTED bit is set to one, then the device supports the Gen1 signaling rate of 1.5 Gb/s.

IDENTIFY DEVICE word 77 bit 1 is a copy of this field.

13.7.7.2.2 SATA GEN2 SIGNALING SPEED SUPPORTED bit

If the SATA GEN2 SIGNALLING SPEED SUPPORTED bit is set to one, then the device supports the Gen2 signaling rate of 3.0 Gb/s.

IDENTIFY DEVICE word 77 bit 2 is a copy of this field.

13.7.7.2.3 SATA GEN3 SIGNALING SPEED SUPPORTED bit

If the SATA GEN3 SIGNALLING SPEED SUPPORTED bit is set to one, then the device supports the Gen3 signaling rate of 6.0 Gb/s.

IDENTIFY DEVICE word 77 bit 3 is a copy of this field.

13.7.7.2.4 NCQ FEATURE SET SUPPORTED bit

If the NCQ FEATURE SET SUPPORTED bit is set to one, then the device supports the NCQ feature set (see 13.6xxx).

IDENTIFY DEVICE word 77 bit 8 is a copy of this field.

13.7.7.2.5 *RECEIPT OF HOST INITIATED POWER MANAGEMENT REQUESTS SUPPORTED bit*

If the RECEIPT OF HOST INITIATED POWER MANAGEMENT REQUESTS SUPPORTED bit is set to one, then the device supports Partial and Slumber interface power management states (see 8.4xxx) when initiated by the host.

If the RECEIPT OF HOST INITIATED POWER MANAGEMENT REQUESTS SUPPORTED bit is cleared to zero, then the DEVICE INITIATED POWER MANAGEMENT SUPPORTED bit shall be set to one.

IDENTIFY DEVICE word 77 bit 9 is a copy of this field.

13.7.7.2.6 *SATA PHY EVENT COUNTERS LOG SUPPORTED bit*

If the SATA PHY EVENT COUNTERS LOG SUPPORTED bit is set to one, then the device supports the SATA Phy Event Counters log (see 13.7.4xxx).

IDENTIFY DEVICE word 77 bit 10 is a copy of this field.

13.7.7.2.7 *UNLOAD WHILE NCQ COMMANDS ARE OUTSTANDING SUPPORTED bit*

If the UNLOAD WHILE NCQ COMMANDS ARE OUTSTANDING SUPPORTED bit is set to one, then the device supports moving the heads to a safe position upon reception of the IDLE IMMEDIATE command with the Unload Feature specified while NCQ commands are outstanding. This bit shall only be set to one if the NCQ FEATURE SET SUPPORTED bit is set to one.

IDENTIFY DEVICE word 77 bit 11 is a copy of this field.

13.7.7.2.8 *NCQ PRIORITY INFORMATION SUPPORTED bit*

If the NCQ PRIORITY INFORMATION SUPPORTED bit is set to one, then the device supports the Priority field (see 13.6.1.4xxx) in the READ FPDMA QUEUED command and WRITE FPDMA QUEUED command and optimization based on this information. This bit shall only be set to one if the NCQ FEATURE SET SUPPORTED bit (see 13.7.7.2.4) is set to one.

IDENTIFY DEVICE word 77 bit 12 is a copy of this field.

13.7.7.2.9 *HOST AUTOMATIC PARTIAL TO SLUMBER TRANSITIONS SUPPORTED bit*

If the HOST AUTOMATIC PARTIAL TO SLUMBER TRANSITIONS SUPPORTED bit is set to one, then the device supports host automatic partial to slumber transitions. If the RECEIPT OF HOST INITIATED POWER MANAGEMENT REQUESTS SUPPORTED bit is cleared to zero, then the HOST AUTOMATIC PARTIAL TO SLUMBER TRANSITIONS SUPPORTED bit shall be cleared to zero. This bit shall only be set to one if the NCQ FEATURE SET SUPPORTED bit (see 13.7.7.2.4) is set to one.

The device shall tolerate a Partial exit latency up to the max Slumber exit latency. This allows the host to asynchronously transition from Partial to Slumber.

If the RECEIPT OF HOST INITIATED POWER MANAGEMENT REQUESTS SUPPORTED bit is cleared to zero, then the HOST AUTOMATIC PARTIAL TO SLUMBER TRANSITIONS SUPPORTED bit shall be cleared to zero.

IDENTIFY DEVICE word 77 bit 13 is a copy of this field.

13.7.7.2.10 *DEVICE AUTOMATIC PARTIAL TO SLUMBER TRANSITIONS SUPPORTED bit*

If the DEVICE AUTOMATIC PARTIAL TO SLUMBER TRANSITIONS SUPPORTED bit is set to one, then the device supports device automatic partial to slumber transitions and may asynchronously transition from Partial to Slumber when enabled. If the DEVICE AUTOMATIC PARTIAL TO SLUMBER TRANSITIONS SUPPORTED bit is cleared to zero (i.e., device initiating interface power management is not supported), then the DEVICE AUTOMATIC PARTIAL TO SLUMBER TRANSITIONS SUPPORTED bit shall be cleared to zero. This bit shall only be set to one if the NCQ FEATURE SET SUPPORTED bit (see 13.7.7.2.4) is set to one.

If the DEVICE INITIATED POWER MANAGEMENT SUPPORTED (see 13.7.7.2.17) bit is cleared to zero, then the DEVICE AUTOMATIC PARTIAL TO SLUMBER TRANSITIONS SUPPORTED bit shall be cleared to zero.

IDENTIFY DEVICE word 77 bit 14 is a copy of this field.

13.7.7.2.11 READ LOG DMA EXT AS EQUIVALENT TO READ LOG EXT SUPPORTED bit

If the READ LOG DMA EXT AS EQUIVALENT TO READ LOG EXT SUPPORTED bit is set to one, then the READ LOG DMA EXT command (see 7.30) and the READ LOG EXT command (see 7.29) may be used in all cases with identical results. If the GPL DMA SUPPORTED bit is cleared to zero, this bit shall be cleared to zero. This bit shall only be set to one if the NCQ FEATURE SET SUPPORTED bit (see 13.7.7.2.4) is set to one.

If the READ LOG DMA EXT AS EQUIVALENT TO READ LOG EXT SUPPORTED bit is cleared to zero and the device indicates command acceptance for a READ LOG DMA EXT command to read the Queued Error Log (see [editors note: 13.7.3]) or the Phy Event Counters log (see [editors note: 13.7.4]), then the device shall return command aborted.

IDENTIFY DEVICE word 77 bit 15 is a copy of this field.

13.7.7.2.12 NCQ STREAMING SUPPORTED bit

If the NCQ STREAMING SUPPORTED bit is set to one, then the device supports NCQ Streaming. This bit shall only be set to one if the NCQ FEATURE SET SUPPORTED bit (see 13.7.7.2.4) is set to one.

IDENTIFY DEVICE word 78 bit 4 is a copy of this field.

13.7.7.2.13 NCQ QUEUE MANAGEMENT COMMAND SUPPORTED bit

If the NCQ QUEUE MANAGEMENT COMMAND SUPPORTED bit is set to one then the device supports the NCQ QUEUE MANAGEMENT command. This bit shall only be set to one if the NCQ FEATURE SET SUPPORTED bit (see 13.7.7.2.4) is set to one.

IDENTIFY DEVICE word 78 bit 5 is a copy of this field.

13.7.7.2.14 SEND AND RECEIVE QUEUED COMMANDS SUPPORTED bit

If the SEND AND RECEIVE QUEUED COMMANDS SUPPORTED bit is set to one, then the device supports the RECEIVE FPDMA QUEUED command and the SEND PDMA QUEUED command. This bit shall only be set to one if the NCQ FEATURE SET SUPPORTED bit (see 13.7.7.2.4) is set to one.

IDENTIFY DEVICE word 78 bit 6 is a copy of this field.

13.7.7.2.15 NON-ZERO BUFFER OFFSETS SUPPORTED bit

If the NON-ZERO BUFFER OFFSETS SUPPORTED bit is set to one, then the device supports transmission and reception of DMA Setup FISes with a non-zero value in the Buffer Offset field of the FIS. If the NON-ZERO BUFFER OFFSETS SUPPORTED bit is cleared to zero, then the device supports transmission and reception of the DMA Setup FIS only with the Buffer Offset field cleared to zero..

IDENTIFY DEVICE word 78 bit 1 is a copy of this field.

13.7.7.2.16 DMA SETUP AUTO-ACTIVATION SUPPORTED bit

If the DMA SETUP AUTO-ACTIVATION SUPPORTED bit is set to one, then the device supports the use of the DMA Setup FIS Auto-Activate optimization as described in section [editors note: 10.3.8.3.1]. When set to one the device supports use of the Auto-Activate optimization. If the DMA SETUP AUTO-ACTIVATION SUPPORTED bit is cleared to zero, then the device does not support the Auto-Activate optimization.

IDENTIFY DEVICE word 78 bit 2 is a copy of this field.

13.7.7.2.17 DEVICE INITIATED POWER MANAGEMENT SUPPORTED bit

If the DEVICE INITIATED POWER MANAGEMENT SUPPORTED bit is set to one the device supports device initiated power management (DIPM) requests. If the DEVICE INITIATED POWER MANAGEMENT SUPPORTED bit is cleared to zero the device does not support device initiated power management requests.

Devices shall support either host-initiated interface power management or device-initiated interface power management. If the RECEIPT OF HOST INITIATED POWER MANAGEMENT REQUESTS SUPPORTED bit is cleared to zero, then the DEVICE INITIATED POWER MANAGEMENT SUPPORTED bit shall be set to one.

~~A device may support reception of power management requests initiated by the host as described in the definition of bit 9 of Word 76 without supporting initiating such power management requests as indicated by this bit.~~

IDENTIFY DEVICE word 78 bit 3 is a copy of this field.

13.7.7.2.18 IN-ORDER DATA DELIVERY SUPPORTED bit

If the IN-ORDER DATA DELIVERY SUPPORTED bit is set to one the device supports guaranteed in-order data delivery when non-zero buffer offsets are used for commands in the NCQ feature set. If the in-order data delivery supported bit is set to one, then the device guarantees in-order data delivery for READ FPDMA QUEUED or WRITE FPDMA QUEUED commands when non-zero buffer offsets are used with multiple DMA Setup FIS. Target data is delivered in order, starting with the first LBA through command completion. If the in-order data delivery supported bit is cleared to zero, then the device does not guarantee in-order data delivery when non-zero buffer offsets are enabled. In this case, data may be interleaved both within a command and across multiple commands. By default this field shall be zero.

IDENTIFY DEVICE word 78 bit 4 is a copy of this field.

13.7.7.2.19 HARDWARE FEATURE CONTROL SUPPORTED bit

If the HARDWARE FEATURE CONTROL SUPPORTED bit is set to one, then the device supports Hardware Feature Control (see 4.20.2). If he HARDWARE FEATURE CONTROL SUPPORTED bit is cleared to zero, then Hardware Feature Control is not supported and the HARDWARE FEATURE CONTROL ENABLED bit shall be cleared to zero.

IDENTIFY DEVICE word 78 bit 5 is a copy of this field.

13.7.7.2.20 SOFTWARE SETTINGS PRESERVATION SUPPORTED bit

If the SOFTWARE SETTINGS PRESERVATION SUPPORTED bit is set to one, then the device supports the SSP feature set (see 4.20).

IDENTIFY DEVICE word 78 bit 6 is a copy of this field.

13.7.7.2.21 NCQ AUTOSENSE SUPPORTED bit

If the NCQ AUTOSENSE SUPPORTED bit is set to one, then the device supports NCQ Autosense (see A.14). This bit shall only be set to one if the NCQ FEATURE SET SUPPORTED bit (see 13.7.7.2.4) is set to one.

IDENTIFY DEVICE word 78 bit 7 is a copy of this field.

13.7.7.2.22 DEVICE SLEEP SUPPORTED bit

If the DEVICE SLEEP SUPPORTED bit is set to one, then:

a) the device supports the Device Sleep feature;
b) the device shall support the Identify Device data log; and
c) the DEVSLP TIMING VARIABLES field VALID bit shall be set to 1.

If the DEVICE SLEEP SUPPORTED bit is cleared to zero, then the device does not support the Device Sleep feature.

IDENTIFY DEVICE word 78 bit 8 is a copy of this field.

13.7.7.2.23 DEVSLEEP_TO_REDUCEDPWRSTATE CAPABILITY SUPPORTED bit

If the DEVSLEEP_TO_REDUCEDPWRSTATE CAPABILITY SUPPORTED bit is set to one, then the device supports remembering whether it was in Partial or Slumber after detection of assertion, and subsequent detection of negation, of DEVSLP.

If the DEVSLEEP_TO_REDUCEDPWRSTATE CAPABILITY SUPPORTED bit is cleared to zero, then the device does not support remembering whether it was in Partial or Slumber after detection of assertion, and subsequent detection of negation, of DEVSLP.

IDENTIFY DEVICE word 77 bit 7 is a copy of this field.

13.7.7.2.24 DIPM SSP PRESERVATION SUPPORTED bit

If the DIPM SSP PRESERVATION SUPPORTED bit is set to one, then the device supports persistence of the Device Initiated Interface Power Management enable/disable setting via Software Settings Preservation.

IDENTIFY DEVICE word 78 bit 10 is a copy of this field.

13.7.7.3 SATA Current Settings

13.7.7.3.1 CURRENT NEGOTIATED SERIAL ATA SIGNAL SPEED

The CURRENT NEGOTIATED SERIAL ATA SIGNAL SPEED field is a coded value that indicates the Serial ATA Phy speed at which the device is currently communicating.

IDENTIFY DEVICE word 77 bits (3:1~~0~~) is a copy of this field.

Table 4 — Coded Values for Negotiated Serial ATA Signaling Speed

Coded Value	Description
000b	Reporting of current signalling speed is not supported
001b	Current signalling speed is Gen1
010b	Current signalling speed is Gen2
011b	Current signalling speed is Gen3
All other values	Reserved

NOTE 2 — In the case of system configurations that have more than one Phy link in the data path (eg. port multiplier), the indicated speed is only relevant for the link between the device Phy and its immediate host Phy. It is possible for each link in the data path to negotiate a different Serial ATA signaling speed.

13.7.7.3.2 *NON-ZERO BUFFER OFFSETS ENABLED bit*

If the NON-ZERO BUFFER OFFSETS ENABLED bit is set to one, then device transmission of DMA Setup FISes with a non-zero value in the Buffer Offset field of the FIS is enabled.

If the NON-ZERO BUFFER OFFSETS ENABLED bit is cleared to zero, then the device is permitted to transmit DMA Setup FIS only with the Buffer Offset field cleared to zero.

By default this field shall be zero.

IDENTIFY DEVICE word 79 bit 1 is a copy of this field.

13.7.7.3.3 *DMA SETUP AUTO-ACTIVATION ENABLED bit*

If the DMA SETUP AUTO-ACTIVATION ENABLED bit is set to one, then the device may utilize the DMA Setup FIS Auto-Activate optimization as described in section [editors note: 10.3.8.3.1].

If the DMA SETUP AUTO-ACTIVATION ENABLED bit is cleared to zero, then the device shall not utilize the Auto-Activate optimization.

By default, this field shall be zero.

IDENTIFY DEVICE word 79 bit 2 is a copy of this field.

13.7.7.3.4 *DEVICE INITIATED POWER MANAGEMENT ENABLED bit*

If the DEVICE INITIATED POWER MANAGEMENT ENABLED bit is set to one, then the device may initiate power management transition requests.

If the DEVICE INITIATED POWER MANAGEMENT ENABLED bit is cleared to zero, then the device shall not initiate interface power management requests to the host.

This field shall be zero by default.

IDENTIFY DEVICE word 79 bit 3 is a copy of this field.

13.7.7.3.5 *IN-ORDER DATA DELIVERY ENABLED bit*

If the IN-ORDER DATA DELIVERY ENABLED bit is set to one and NON-ZERO BUFFER OFFSETS ENABLED bit is set to one (see 13.7.7.3.2), then the device may satisfy a READ FPDMA QUEUED or WRITE FPDMA QUEUED command by transmitting multiple DMA Setup FISes with non-zero buffer offset values where appropriate, provided that the target data is delivered in order, starting with the first LBA through command completion.

If the IN-ORDER DATA DELIVERY ENABLED bit is cleared to zero, then the device may interleave data both in a command and across multiple commands using non-zero buffer offsets if the NON-ZERO BUFFER OFFSETS ENABLED bit is set to one.

By default this field shall be zero.

IDENTIFY DEVICE word 79 bit 4 is a copy of this field.

13.7.7.3.6 *HARDWARE FEATURE CONTROL ENABLED bit*

If the HARDWARE FEATURE CONTROL ENABLED bit is set to one, then device support for Hardware Feature Control feature (see 13.HardwareFeatureControlxxx) is enabled. If the HARDWARE FEATURE CONTROL ENABLED bit is cleared to zero, then Hardware Feature Control is disabled.

IDENTIFY DEVICE word 79 bit 5 is a copy of this field.

13.7.7.3.7 *SOFTWARE SETTINGS PRESERVATION ENABLED bit*

If the SOFTWARE SETTINGS PRESERVATION ENABLED bit is set to one, then the SSP feature set is enabled and the device shall preserve specified software settings across COMRESET (see 13.5xxx).

If the SOFTWARE SETTINGS PRESERVATION ENABLED bit is cleared to zero, then the SSP feature set is disabled and the device shall clear specified software settings if a COMRESET occurs (see 13.5xxx).

If the SOFTWARE SETTINGS PRESERVATION SUPPORTED (see 13.7.7.2.20) is set to one, then tSOFTWARE SETTINGS PRESERVATION ENABLED bit shall be set to one after a power on reset has been processed. If the SOFTWARE SETTINGS PRESERVATION SUPPORTED is cleared to zero, then the SOFTWARE SETTINGS PRESERVATION ENABLED bit shall be zero by default.

IDENTIFY DEVICE word 79 bit 6 is a copy of this field.

13.7.7.3.8 *AUTOMATIC PARTIAL TO SLUMBER TRANSITIONS ENABLED bit*

If the AUTOMATIC PARTIAL TO SLUMBER TRANSITIONS ENABLED bit is set to one, then the device may asynchronously transition from Partial to Slumber. If the AUTOMATIC PARTIAL TO SLUMBER TRANSITIONS ENABLED bit is cleared to zero, then shall not asynchronously transition from Partial to Slumber.

If the DEVICE INITIATED POWER MANAGEMENT ENABLED bit is cleared to zero, then the AUTOMATIC PARTIAL TO SLUMBER TRANSITIONS ENABLED bit shall be cleared to zero.

IDENTIFY DEVICE word 79 bit 7 is a copy of this field.

13.7.7.3.9 *DEVICE SLEEP ENABLED bit*

If the DEVICE SLEEP ENABLED bit is set to one, then the Device Sleep feature (see [editors note:xxx]) is enabled. If the DEVICE SLEEP ENABLED bit is cleared to zero, then the Device Sleep feature is disabled.

IDENTIFY DEVICE word 79 bit 8 is a copy of this field.

13.7.7.3.10 CURRENT HARDWARE FEATURE CONTROL IDENTIFIER

If the CURRENT HARDWARE FEATURE CONTROL IDENTIFIER bit is non-zero, then Table 89xxx describes the current Hardware Feature Control behavior. If the CURRENT HARDWARE FEATURE CONTROL IDENTIFIER is cleared to zero, then the current Hardware Feature Control behavior shall be either disable staggered spin-up (DSS) or HDD activity indication (DAS).

13.7.7.3.11 SUPPORTED HARDWARE FEATURE CONTROL IDENTIFIER

The SUPPORTED HARDWARE FEATURE CONTROL IDENTIFIER bit (see Table 89) indicates the value that is permitted for the Current Hardware Feature Control Identifier field.

13.7.7.4 DEVSLP TIMING VARIABLES

13.7.7.4.1 DEVSLEEP EXIT TIMEOUT

The DEVSLEEP EXIT TIMEOUT (DETO) field contains the maximum time, in ms, from when DEVSLP is negated, to when the device shall be ready to detect OOB signals. If the value in DETO is zero, then the host should use 20 ms as the value of DETO. See 13.DeviceSleepFeaturexxx for more information.

13.7.7.4.2 MINIMUM DEVSLP ASSERTION TIME

The MINIMUM DEVSLP ASSERTION TIME (MDAT) field contains the minimum time, in ms, for which the host shall assert DEVSLP, once it has been asserted. If the value in MDAT is zero, then the host should use 10 ms as the value of MDAT. See 13.DeviceSleepFeaturexxx for more information.

