# Proposed Draft

# Serial ATA International Organization

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## TPR050v2\_SATA31\_SATA\_MicroSSD\_Footprint\_Update Title: SATA MicroSSD Footprint Update

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## **Document History**

Version	Date	Comments
00	2/26/2013	Initial release.
01	3/20/2013	Member review
02	05/01/2013	Ratified

#### 1 Introduction

SanDisk added some new packages for MicroSSD-based products. The functional pins are identical to the other members of the package family. This TPR adds the new footprint and its ball-out to the the Serial ATA specification.

#### 2 Technical Specification Changes

The following additions are based on the content of Serial ATA TP #035, SATA-BGA-SSD, Revision 12a, 06/01/2011. Deletions to TP 038 are marked in red strike through; additions are marked in blue underline. Black is original content.

#### 6.7 BGA SATA Micro SSD Interface (to be inserted before existing Section 6.7)

#### 6.7.1 SATA MicroSSD Interface scope

This section defines the mechanical properties of the a BGA\_SATA MicroSSD device and device interface.

#### 6.7.2 **BGA SATA Micro SSD Mechanical Specification**

A BGA-SATA MicroSSD shall use package variants:

- a) AC<sub>7</sub>;
- <u>b)</u> AM,
- <u>c)</u> AK<del>,</del>;
- d) AL-;
- e) AR;
- f) CA; or
- g) CB<sub>7</sub>;
- h) DB, or
- i) <u>DC,</u>

as defined in the JEDEC document "MO-276, Standard Profile and Low Profile Rectangular Fine Pitch"; Ball Grid Array Family, 0.50 mm Pitch", revision E or later.

The rest of this section is informative only; refer to JEDEC MO-276E (or later) for the formal mechanical specification of BGA-SATA MicroSSD packages.

The specified package variants for a BGA\_SATA MicroSSD use four five distrinct package footprints. The package footprints (bottom view) are shown below. A "+" sign denotes a depopulated ball position. The functional balls (signals or power) for each footprint are the inner 3 or 4 rows on each footprint (square rows); the rest of the populated balls are mechanical only, for package stability. The normative signal assignment for the functional balls is specified in Section 6.6.2, BGA\_SATA MicroSSD Ballout.

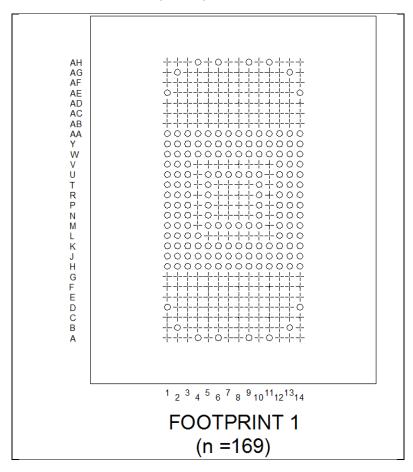


Figure 105 - Footprint 1, SATA MicroSSD variant AC, 169 balls (informative)

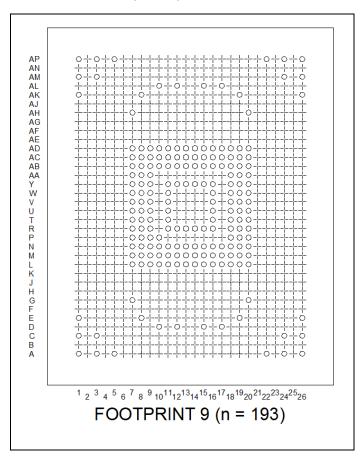


Figure 106 - Footprint 9, SATA MicroSSD variant AK and CB, 193 balls (informative)

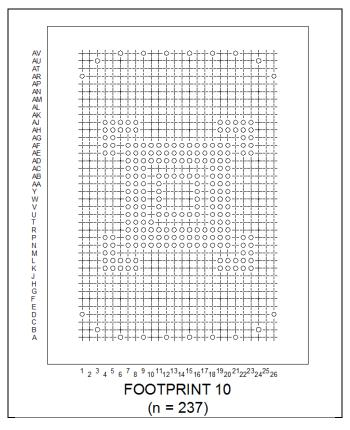


Figure 107 - Footprint 10, SATA MicroSSD variant AL, 237 balls (informative)

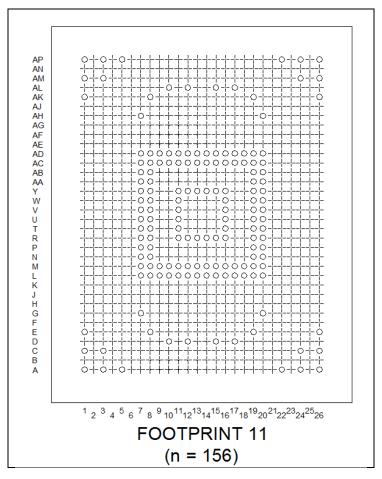


Figure 108 – Footprint 11, SATA MicroSSD variant AM and CA, 156 balls (informative)

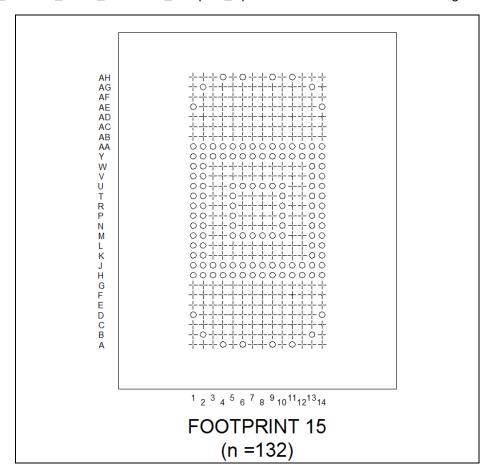


Figure 109 - Footprint 15, SATA MicroSSD variant AR, DB, and DC, 132 balls (informative)

#### 6.7.3 **BGA** MicroSSD Ballout - Functional Signal Definition

Table x defines the signal assignment of the BGA SSD connection for each of the package types defined in Section 6.6.1.

- VSP Vendor Specific
- RESERVED Reserved for future standardization (SATA V3.1, Section 4.2.2.8)
- DNU (Do Not Use) Internal test only; shall not be connected on host.
- TEST May be connected for test/diagnostic use, but not used during normal device operation.

Table 22 - Signal Assignments for BGA SSD Device (part 1 of 5)

			IMENT print #)		BALL NAME	ТҮРЕ	DESCRIPTIONS	
132 (15)	156 (11)	169 (1)	193 (9)	237 (10)				
	SATA Interface Signals							
<u>M1</u>	R7	M1	R7	U7	SATA_RX_N	Input	Differential Signal Pair A	
<u>L1</u>	P7	L1	P7	T7	SATA_RX_P	трис	(SATA Device Receive Signal Differential Pair)	
<u>P1</u>	U7	P1	U7	W7	SATA_TX_N	Output	Differential Signal Pair B	
<u>R1</u>	V7	R1	V7	Y7	SATA_TX_P	Output	(SATA Device Transmit Signal Differential Pair)	

			IMENT orint #)		BALL NAME	ТҮРЕ	DESCRIPTIONS
132	156	169	193	237		l .	
(15)	(11)	(1)	(9)	(10)			
<u>J7</u>	M13	J7	M13	P13	DAS	Output	Device Activity Signal
<u>P2</u>	U8	P2	U8	W8	SATA_VCC	Supply	+3.3 V
<u>R2</u>	V8	R2	V8	Y8	SATA_VCC	Supply	+3.3 V
<u>L2</u>	Р8	L2	P8	Т8	SATA_VDD	Supply	+1.2 V
<u>M2</u>	R8	M2	R8	U8	SATA_VDD	Supply	+1.2 V
<u>K1</u>	N7	K1	N7	R7	SATA_VSS	GND	Signal Ground
<u>N1</u>	T7	N1	T7	V7	SATA_VSS	GND	Signal Ground
<u>T1</u>	W7	T1	W7	AA7	SATA_VSS	GND	Signal Ground
						Control Sign	nals
<u>H3</u>	L9	Н3	L9	N9	XTAL_OUT	Output	System Clock output <sup>4</sup> 2
<u>J4</u>	M10	J4	M10	P10	XTAL_IN	Input	System Clock input <sup>26</sup>
<u>J3</u>	M9	J3	M9	P9	PWR_RESETN	Input	Hardware Reset <sup>3</sup>
						Optional Sig	nals
<u>AA10</u>	AD16	AA10	AD16	AF16	SPI_MISO	Input	Master In Slave Out
<u>AA9</u>	AD15	AA9	AD15	AF15	SPI_CS0	Output	Chip Select
<u>Y10</u>	AC16	Y10	AC16	AE16	SPI_CLK	Output	Clock
<u>AA12</u>	AD18	AA12	AD18	AF18	SPI_CS1	Output	Chip Select
<u>AA11</u>	AD17	AA11	AD17	AF17	SPI_MOSI	Ouput	Master Out Slave In
<u>V2</u>	AA8	V2	AA8	AC8	TEST		
<u>H9</u>	L15	Н9	L15	N15	TEST		
<u>H10</u>	L16	H10	L16	N16	TEST		
<u>H11</u>	L17	H11	L17	N17	TEST		
<u>H12</u>	L18	H12	L18	N18	TEST		
<u>V14</u>	AA20	V14	AA20	AC20	VSP		
<u>J6</u>	M12	J6	M12	P12	VSP		
<u>Y3</u>	AC9	Y3	AC9	AE9	RESERVED DEVSL P		Future Low Power (PHYSLP)Enter/Exit DevSleep
<u>Y5</u>	AC11	Y5	AC11	AE11	RESERVED		Future Low Power
<u>H7</u>	L13	H7	L13	N13	RESERVED		Future Low Power
					Po	wer Supply S	Signals
<u>M7</u>	R13	M7	R13	U13	VCC	Supply	+3.3 V
<u>M8</u>	R14	M8	R14	U14	VCC	Supply	+3.3 V
<u>M9</u>	R15	M9	R15	U15	VCC	Supply	+3.3 V
<u>M10</u>	R16	M10	R16	U16	VCC	Supply	+3.3 V
<u>N10</u>	T16	N10	T16	V16	VCC	Supply	+3.3 V
<u>P10</u>	U16	P10	U16	W16	VCC	Supply	+3.3 V

			NMENT print #)		BALL NAME	ТҮРЕ	DESCRIPTIONS
<u>132</u>	156	169	193	237			
<u>(15)</u>	(11)	(1)	(9)	(10)			
<u>J5</u>	M11	J5	M11	P11	VCC	Supply	+3.3 V
<u>H6</u>	L12	Н6	L12	N12	VCC	Supply	+3.3 V
<u>M13</u>	R19	M13	R19	U19	VCC	Supply	+3.3 V
<u>M14</u>	R20	M14	R20	U20	VCC	Supply	+3.3 V
<u>R5</u>	V11	R5	V11	Y11	VCC	Supply	+3.3 V
<u>U14</u>	Y20	U14	Y20	AB20	VCC	Supply	+3.3 V
<u>U13</u>	Y19	U13	Y19	AB19	VCC	Supply	+3.3 V
<u>V13</u>	AA19	V13	AA19	AC19	VCC	Supply	+3.3 V
<u>Y2</u>	AC8	Y2	AC8	AE8	VCC	Supply	+3.3 V
<u>R10</u>	V16	R10	V16	Y16	VCCQ	Supply	+1.8 V
<u>T10</u>	W16	T10	W16	AA16	VCCQ	Supply	+1.8 V
<u>U10</u>	Y16	U10	Y16	AB16	VCCQ	Supply	+1.8 V
<u>T5</u>	W11	T5	W11	AA11	VDDC	Supply	+1.2 V
<u>U5</u>	Y11	U5	Y11	AB11	VDDC	Supply	+1.2 V
<u>U6</u>	Y12	U6	Y12	AB12	VDDC	Supply	+1.2 V
<u>U7</u>	Y13	U7	Y13	AB13	VDDC	Supply	+1.2 V
<u>M5</u>	R11	M5	R11	U11	VDD	Supply	+1.2 V
<u>N5</u>	T11	N5	T11	V11	VDD	Supply	+1.2 V
			1			GND signa	ils
<u>M6</u>	R12	M6	R12	U12	VSS	GND	Ground
<u>P5</u>	U11	P5	U11	W11	VSS	GND	Ground
<u>H1</u>	L7	H1	L7	N7	VSS	GND	Ground
<u>H2</u>	L8	H2	L8	N8	VSS	GND	Ground
<u>J1</u>	M7	J1	M7	P7	VSS	GND	Ground
<u>H5</u>	L11	H5	L11	N11	VSS	GND	Ground
<u>H13</u>	L19	H13	L19	N19	VSS	GND	Ground
<u>H14</u>	L20	H14	L20	N20	VSS	GND	Ground
<u>J13</u>	M19	J13	M19	P19	VSS	GND	Ground
<u>J14</u>	M20	J14	M20	P20	VSS	GND	Ground
<u>K13</u>	N19	K13	N19	R19	VSS	GND	Ground
<u>L13</u>	P19	L13	P19	T19	VSS	GND	Ground
<u>Y14</u>	AC20	Y14	AC20	AE20	VSS	GND	Ground
<u>AA14</u>	AD20	AA14	AD20	AF20	VSS	GND	Ground
<u>AA13</u>	AD19	AA13	AD19	AF19	VSS	GND	Ground
<u>AA2</u>	AD8	AA2	AD8	AF8	VSS	GND	Ground

	BALL ASSIGNMENT # Balls (Footprint #)			BALL NAME	ТҮРЕ	DESCRIPTIONS	
<u>132</u>	156	169	193	237			
<u>(15)</u>	(11)	(1)	(9)	(10)			
<u>AA1</u>	AD7	AA1	AD7	AF7	VSS	GND	Ground
<u>N2</u>	T8	N2	T8	V8	VSS	GND	Ground
<u>U8</u>	Y14	U8	Y14	AB14	VSS	GND	Ground
<u>U9</u>	Y15	U9	Y15	AB15	VSS	GND	Ground
<u>P13</u>	U19	P13	U19	W19	VSS	GND	Ground
<u>L14</u>	P20	L14	P20	T20	VSS	GND	Ground
<u>P14</u>	U20	P14	U20	W20	VSS	GND	Ground
<u>R13</u>	V19	R13	V19	Y19	VSS	GND	Ground
<u>Y1</u>	AC7	Y1	AC7	AE7	VSS	GND	Ground
<u>W1</u>	AB7	W1	AB7	AD7	VSS	GND	Ground
<u>K2</u>	N8	K2	N8	R8	VSS	GND	Ground
						Other Sign	als
<u>AA5</u>	AD11	AA5	AD11	AF11	DNU		
<u>AA3</u>	AD9	AA3	AD9	AF9	DNU		
<u>Y7</u>	AC13	Y7	AC13	AE13	DNU		
<u>AA7</u>	AD13	AA7	AD13	AF13	DNU		
<u>Y8</u>	AC14	Y8	AC14	AE14	DNU		
<u>J10</u>	M16	J10	M16	P16	DNU		
<u>J8</u>	M14	J8	M14	P14	RESERVED		
<u>J2</u>	M8	J2	M8	P8	RESERVED		
<u>H4</u>	L10	H4	L10	N10	RESERVED		
<u>H8</u>	L14	Н8	L14	N14	RESERVED		
<u>N13</u>	T19	N13	T19	V19	RESERVED		
<u>R14</u>	V20	R14	V20	Y20	RESERVED		
<u>N14</u>	T20	N14	T20	V20	RESERVED		
<u>K14</u>	N20	K14	N20	R20	RESERVED		
<u>J11</u>	M17	J11	M17	P17	RESERVED		
<u>J12</u>	M18	J12	M18	P18	RESERVED		
<u>W2</u>	AB8	W2	AB8	AD8	RESERVED		
<u>W13</u>	AB19	W13	AB19	AD19	RESERVED		
<u>W14</u>	AB20	W14	AB20	AD20	RESERVED		
<u>Y11</u>	AC17	Y11	AC17	AE17	RESERVED		
<u>AA8</u>	AD14	AA8	AD14	AF14	RESERVED		
<u>Y9</u>	AC15	Y9	AC15	AE15	RESERVED		
<u>AA6</u>	AD12	AA6	AD12	AF12	RESERVED		

	BALL ASSIGNMENT # Balls (Footprint #)				BALL NAME	ТҮРЕ	DESCRIPTIONS
<u>132</u>	156	169	193	237		•	
<u>(15)</u>	(11)	(1)	(9)	(10)			
<u>Y13</u>	AC19	Y13	AC19	AE19	RESERVED		
<u>Y12</u>	AC18	Y12	AC18	AE18	RESERVED		
<u>T14</u>	W20	T14	W20	AA20	RESERVED		
<u>T13</u>	W19	T13	W19	AA19	RESERVED		
<u>V1</u>	AA7	V1	AA7	AC7	RESERVED		
<u>U1</u>	Y7	U1	Y7	AB7	RESERVED		
<u>T2</u>	W8	T2	W8	AA8	RESERVED		
<u>U2</u>	Y8	U2	Y8	AB8	RESERVED		
AA4	AD10	AA4	AD10	AF10	RESERVED		
<u>Y6</u>	AC12	Y6	AC12	AE12	RESERVED		
<u>J9</u>	M15	19	M15	P15	RESERVED		
<u>Y4</u>	AC10	Y4	AC10	AE10	RESERVED		
		К3	N9	R9	RESERVED		
		L3	Р9	Т9	RESERVED		
		M3	R9	U9	RESERVED		
		N3	T9	V9	RESERVED		
		Р3	U9	W9	RESERVED		
		R3	V9	Y9	RESERVED		
		T3	W9	AA9	RESERVED		
		U3	Y9	AB9	RESERVED		
		V3	AA9	AC9	RESERVED		
		W3	AB9	AD9	RESERVED		
		K12	N18	R18	RESERVED		
		L12	P18	T18	RESERVED		
		M12	R18	U18	RESERVED		
		N12	T18	V18	RESERVED		
		P12	U18	W18	RESERVED		
		R12	V18	Y18	RESERVED		
		T12	W18	AA18	RESERVED		
		U12	Y18	AB18	RESERVED		
		V12	AA18	AC18	RESERVED		
		W12	AB18	AD18	RESERVED		
		K4	N10	R10	RESERVED		
		K5	N11	R11	RESERVED		
		К6	N12	R12	RESERVED		

			IMENT orint #)		BALL NAME	ТҮРЕ	DESCRIPTIONS
<u>132</u>	156	169	193	237			
<u>(15)</u>	(11)	(1)	(9)	(10)			
		K7	N13	R13	RESERVED		
		К8	N14	R14	RESERVED		
		К9	N15	R15	RESERVED		
		K10	N16	R16	RESERVED		
		K11	N17	R17	RESERVED		
		W4	AB10	AD10	RESERVED		
		W5	AB11	AD11	RESERVED		
		W6	AB12	AD12	RESERVED		
		W7	AB13	AD13	RESERVED		
		W8	AB14	AD14	RESERVED		
		W9	AB15	AD15	RESERVED		
		W10	AB16	AD16	RESERVED		
		W11	AB17	AD17	RESERVED		
		L4	P10	T10	RESERVED		

#### Notes:

Optional pin reserved for system clock output to drive crystal or other system requirements. Frequency is system implementation dependent.
 Optional pin reserved for system clock input. Frequency is system implementation dependent.
 Optional pin reserved for Hardware Reset. Implementation is system dependent. For detailed timing

information, consult device data sheet.