Proposed Draft

Serial ATA International Organization

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TPR053v11_SATA31_M.2_Card_Format_for_SSDs
Title: M.2 Card Format for SSDs

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Document History

Version	Date	Comments
0	Feb 17, 2012	Initial release.
01	April 3, 2012	Various updates to dimensions. Change 40 mm card to a 42 mm card. Added in dimensional details of M.2 connector. Removed keep out near top mounting hole. Restrict top side component height to 1.35 mm. Added pad and anti-pad details. Connector finger details updated.
02	June 13, 2012	Added 60 mm card length and 110 mm length. corrected error on pins 5,7,17,19 which flipped the PCIe lanes
03	July 10, 2012	Mounting hole changed. Figure for section 1.6 redone to be clearer with more readable and larger fonts (no new data content). Added pin 21 to enable system to determine if a WWAN card or a SSD is present in a slot. Added definition of a 'socket' in section 1.2. Added power and Signal requirements section. Added keep outs on component plaM.2 CEMent near connector
04	August 14, 2012	Added "figure" text on top of each drawing. Figure 1, 2, 7 updated. Figure 8 updated and clarifying language added to explain 1.50 usage… removed antenna keep-out as that is not relevant to an SSD design. Mounting hole details figure merged with figure 1 and figure 2. Figure 9 notch tolerance loosened. Figure 12 updated to remove duplicate dimensioning information. Pins 1, 21, 69 and 75 redefined as "configuration pins". This removes the IFDET and PRESENCE pins (they are simply redefined as CONFIG pins)
05	October 30,2012	Changed name of form factor to "M.2" Added usage model Added in compliance points for connector measurements Added profile "D5" for a 1.5mm top/1.5mm bottom clearance Update to connector drawing for tolerance (editorial, no physical changes)
06	Nov 28, 2012	Pin 5 & 11 swapped. Made voiding a pullback details informative. Minor editorial text updates. Noted that PCIe signals are w.r.t. system.
07	Dec 19, 2012	Added impedance specification section. Flipped the meaning of RX and TX to be w.r.t. the mini card Updated z-height figures Corrected some header number inconsistencies
08	Jan 23, 2013	Changed DAS# to DAS (DAS remains an active low signal; the removal of the hash is to be consistent with the gold standard). Clarified anti pad dimensions on Fig 19. Added table 3 and table 4 headings. Added note 4 to table 3. Added blurb that the mechanical sections are informative. Fixed various typos. Figure 2 and Figure 3 modified to have missing line added. Delete PCIe signal call out
09	Jan 29, 2013	Added PCIe signals names back in. PCIe functions now refer to PCIe standard. Added header on 1st page which is the file name. Changed copyright date to reflect 2013. Many minor updates to missing figure numbers, and to make document consistent throughout.
10	Mar 27, 2013	Member review
11	May 1, 2013	Ratified

1 Symbols and abbreviations

GT/s Giga Transfers per second (i.e., 10^9 transfers per second)

2 Internal M.2 connector

This section defines the requirements of an M.2 connector with support for SATA as well as PCI Express signaling.

This board format is specifically designed to match commonly used SSD memory components to ensure maximum use of circuit board area.

The definition supports the following capabilities:

a) SATA transfer rates:
   A) Gen1 (i.e., 1.5 Gbps);
   B) Gen2 (i.e., 3.0 Gbps); and
   C) Gen3 (i.e., 6.0 Gbps);

and

b) PCI Express:
   A) V1 (i.e., 2.5 GT/s per lane);
   B) V2 (i.e., 5 GT/s per lane); and
   C) V3 (i.e., 8 GT/s per lane).

In addition this format supports the following concepts:

a) CONFIG pins that are set by the SSD to inform the host if the drive wishes to use the SATA or PCIe signaling scheme, as well as informing the system if a card is present and if the card is an SSD or another type of device;
b) DEVSLP (i.e., device sleep) that is a pin that the host may drive to inform an SSD that it should enter into a low power mode (if possible); and
c) MFG1/MFG2, two vendor pins for drive or SSD manufacturing usage.

2.1 M.2 mechanical (informative)

For SSD devices, the M.2 specification describes in detail a set of module sizes (e.g., 22 mm x 42 mm, 22 mm x 80 mm), connector heights (e.g., 2.25 mm, 2.75 mm, and 4.2 mm), and keying options for use in M.2 SSD modules.

A SATA device built to meet the M.2 form factor specification shall use the module sizes and connector/key combinations as described in the M.2 specification (see PCIe M.2). Implementers should refer directly to the M.2 specification for detailed normative mechanical specifications for M.2-based SATA devices.

2.2 Usage Model

The internal M.2 connector is to be used for embedded applications. As an addendum to SATA rev 3.1 Gold Table 2.

TABLE 1: Usage model

Usage model section number	**M.2**
Cable and/or backplane type	**Backplane**
Cable length	**na**
Cable Electrical	**P**
Attenuation at 4.5GHz	**P**
Host-side connector	**See** 5
Device-side connector	**See 2**
SATA Gen1i 1.5 Gbps	**D**
SATA Gen1m 1.5 Gbps	**NS**
SATA Gen1u 1.5 Gbps	**H**
SATA Gen2i 3.0 Gbps	**D**
SATA Gen2m 3.0 Gbps	**NS**
SATA Gen2u 3.0 Gbps	**H**
SATA Gen3i 6.0 Gbps	**D**
SATA Gen3u 6.0 Gbps	**H**
Hot plug support	**NS**

As an addendum to SATA Revision 3.1 specification, section 5.2.10.

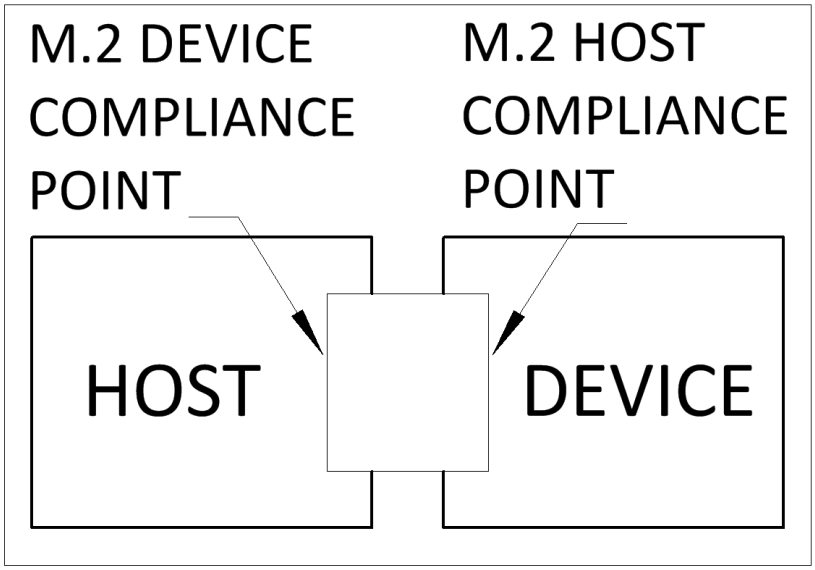


FIGURE 1 - Embedded M.2 application

1.2 Embedded applications

Applications and compliance points for M.2 devices in the embedded applications are not defined in this specification. The M.2 device shall comply with Gen1i, Gen 2i, and Gen3i specifications. The M.2 host shall comply with Gen1u, Gen2u, and Gen3u specifications.

The M.2 host and device shall comply with this standard and is equivalent to the Mobile Applications usage model.

1.3 M.2 Lab-Load

Due to the direct connect application of M.2 connection; two different types of M.2 adaptors are required as laboratory loads. The device shall be mated to a female adaptor and the host shall be mated to a male connection as shown in Figure 2 and Figure 3.

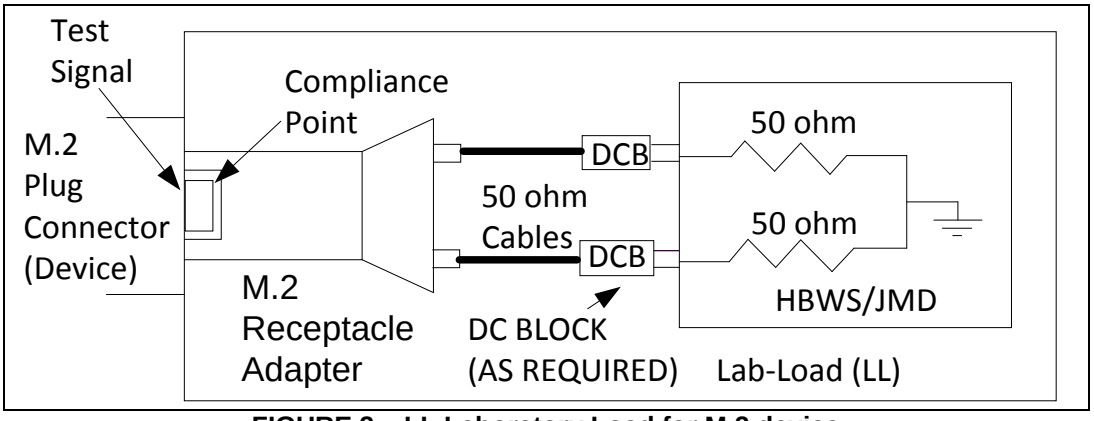


FIGURE 2 – LL Laboratory Load for M.2 device

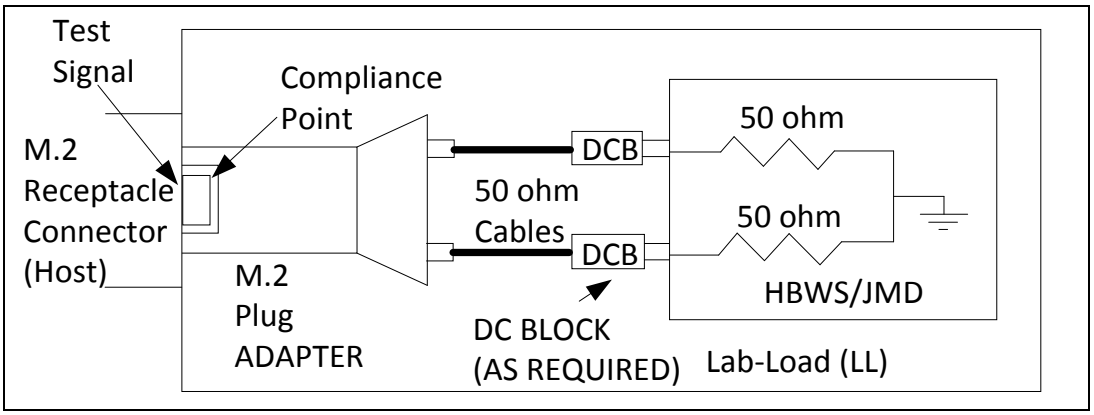


FIGURE 3 – LL Laboratory Load for M.2 host

The electrical characteristics of the LL shall be greater than the required performance of the parameter being measured such that the LL effects of the on the parameter under test may be successfully compensated for, or de-embedded, in the measured data.

1.4 M.2 Lab-Sourced Signal details

As described in Lab Load Details in (Editor's note 7.4.1.1 in SATA rev 3.1 Gold), to properly provide a SATA signal into M.2 device, both female and male type M.2 adaptors are required for device and host, respectively as shown in Figure 4 and Figure 5.

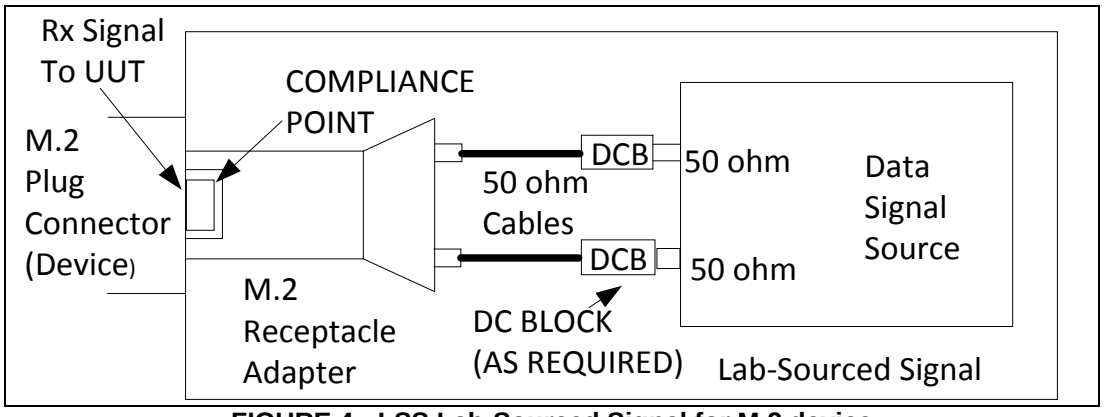


FIGURE 4 - LSS Lab-Sourced Signal for M.2 device

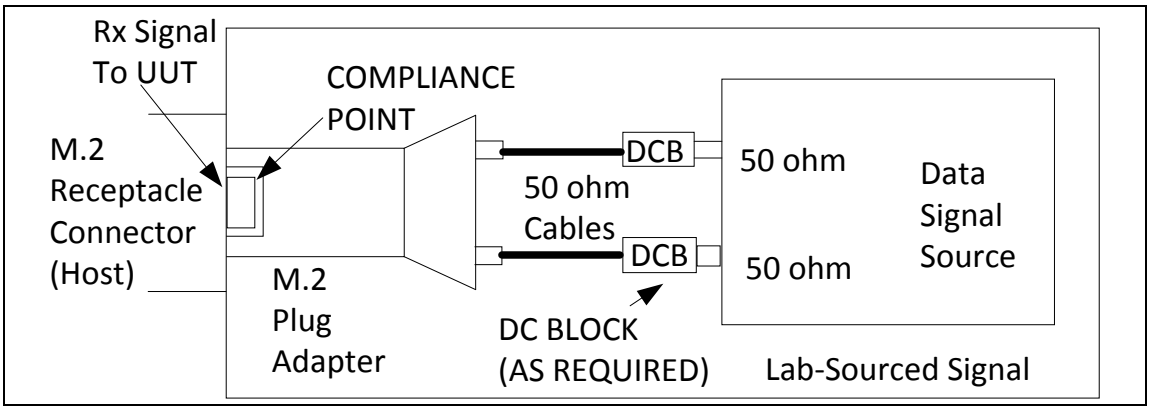


FIGURE 5 - LSS Lab-Sourced Signal for M.2 host

1.5 M.2 Connector compliance point

The compliance points of M.2 are shown in Figure 6.

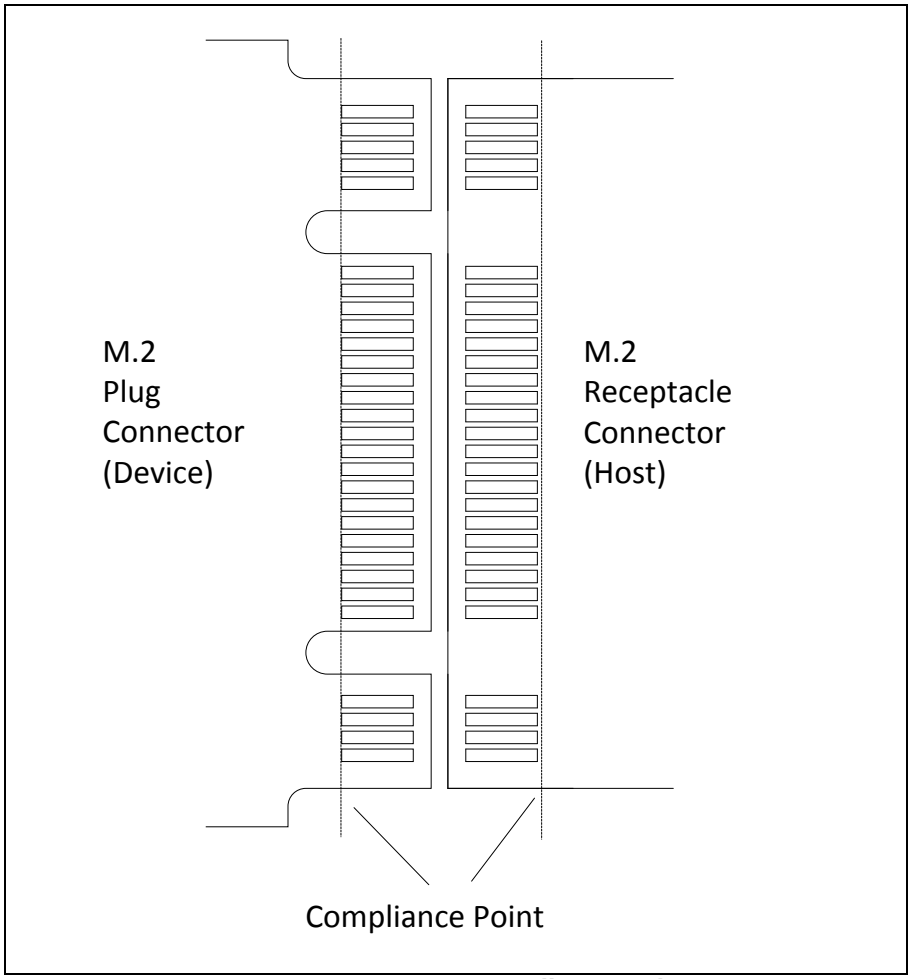


FIGURE 6 - Compliance point

3 M.2 board connector (informative)

M.2 uses a dual-sided edge card connector with a 0.5 mm contact pitch. The connector provides for 75 pin locations.

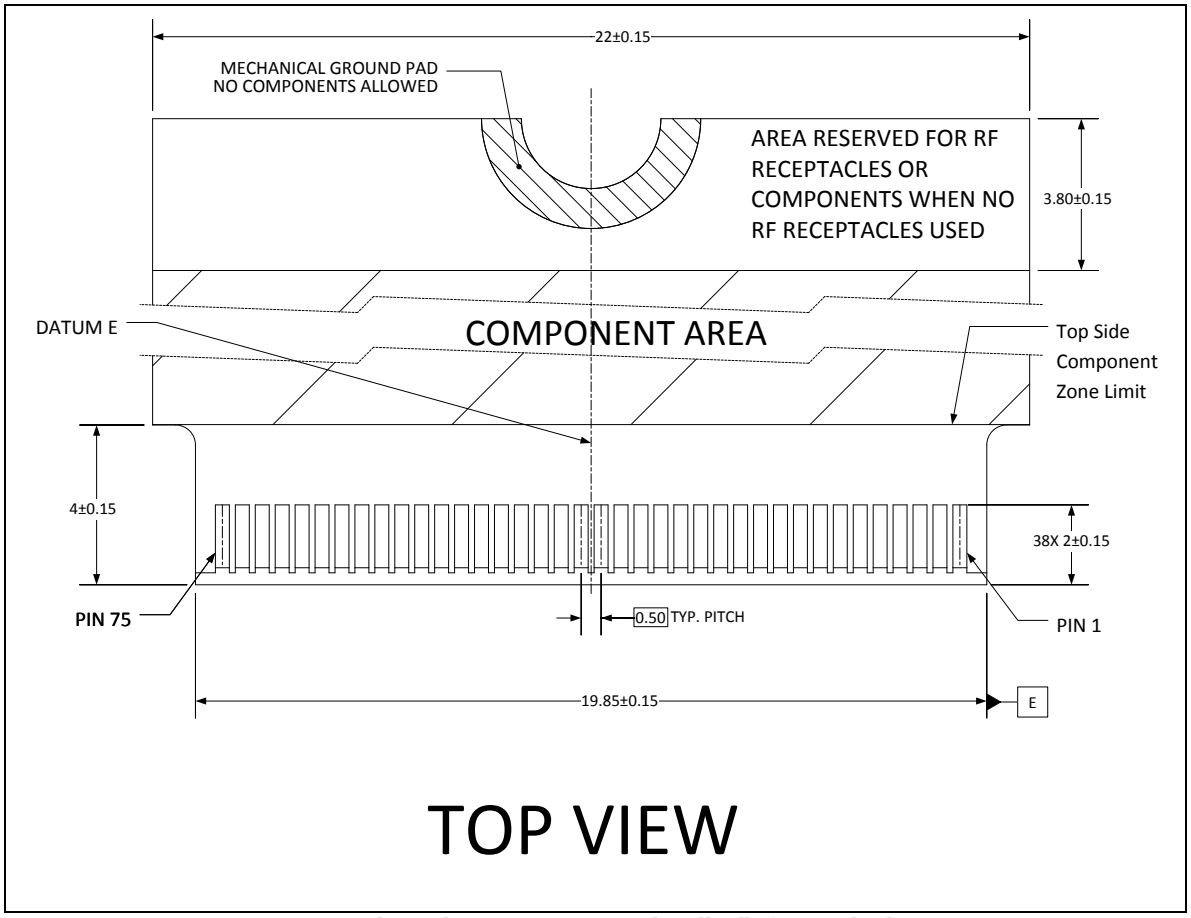


FIGURE 7: M.2 board connector top details (informative)

The reserved area for RF receptacles is only applicable if a SATA device is planned to be used in a shared use socket (see PCIe M.2). Components may be in this area for a SATA device, however be aware that a system may have antenna wires in this area.

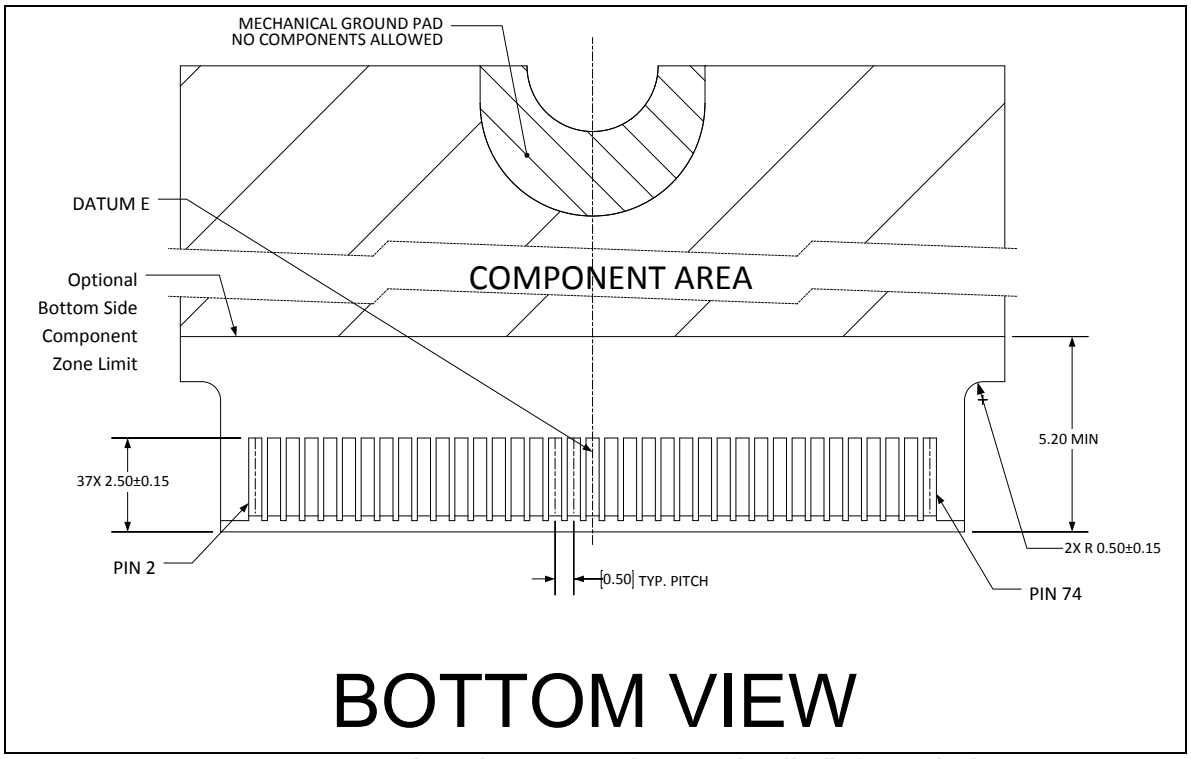
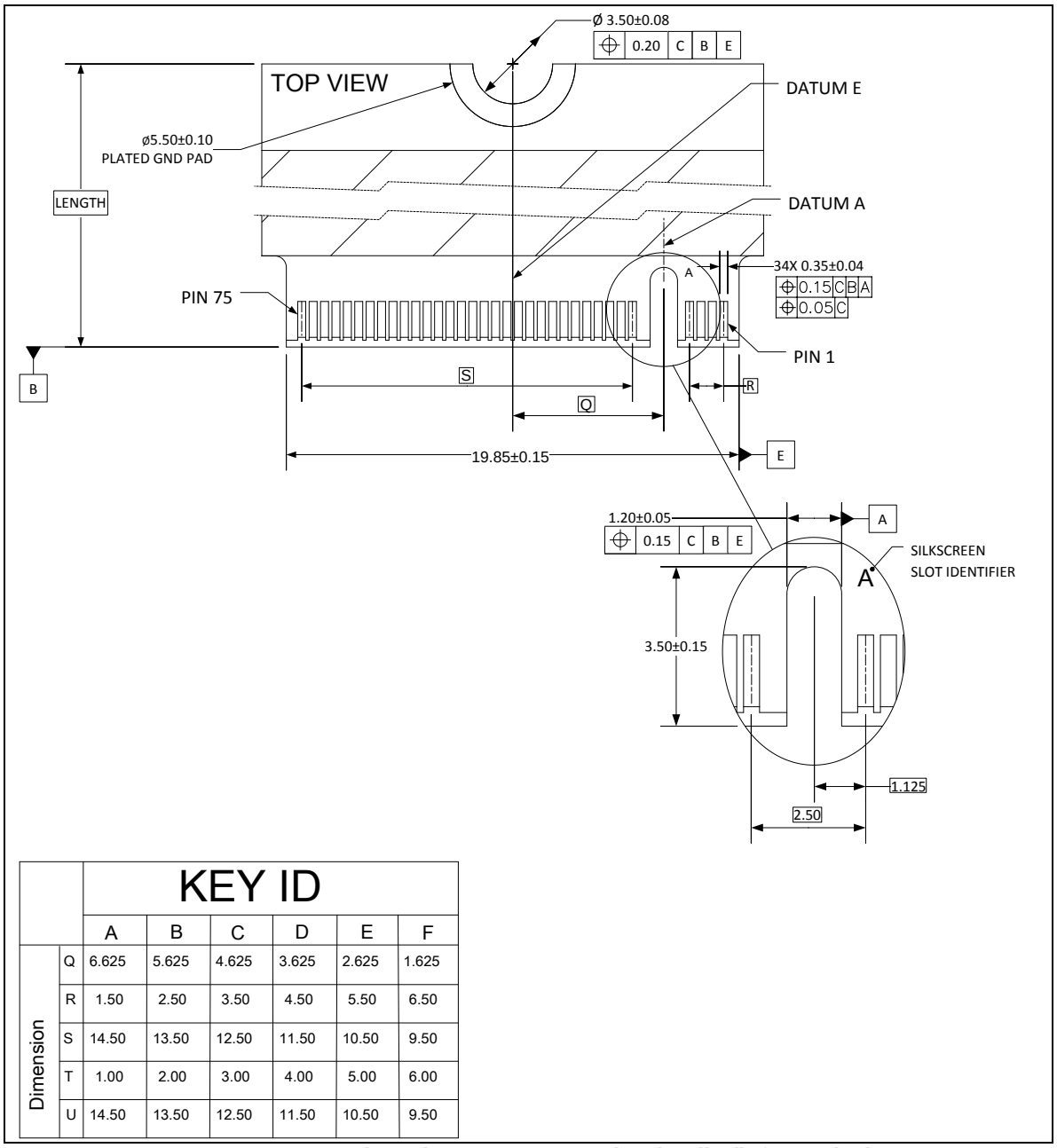
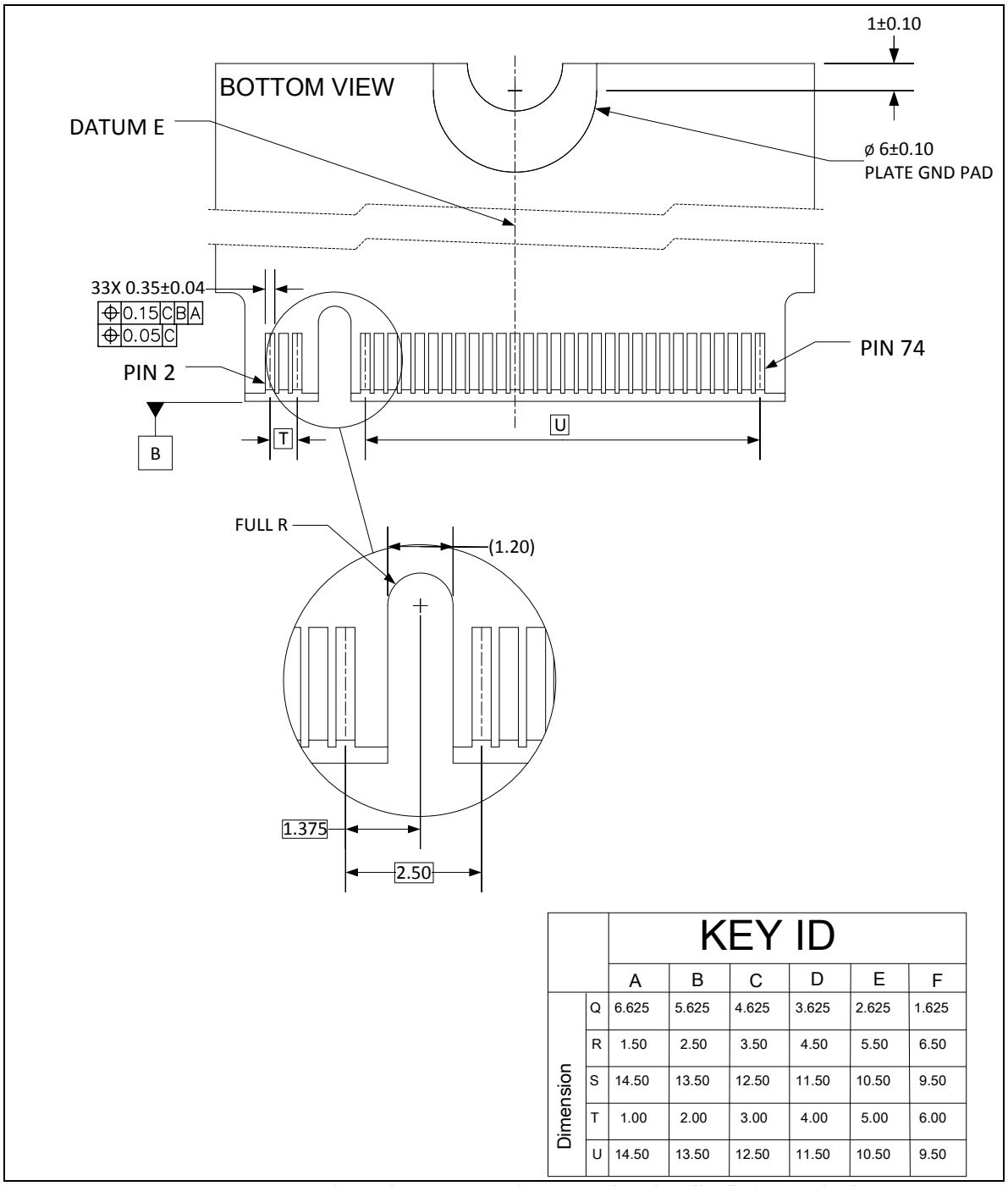


FIGURE 8 – M.2 board connector bottom details (informative)



		KEY ID					
		A	B	C	D	E	F
Dimension	Q	6.625	5.625	4.625	3.625	2.625	1.625
	R	1.50	2.50	3.50	4.50	5.50	6.50
	S	14.50	13.50	12.50	11.50	10.50	9.50
	T	1.00	2.00	3.00	4.00	5.00	6.00
	U	14.50	13.50	12.50	11.50	10.50	9.50

FIGURE 9 – M.2 board connector top slot details (informative)



		KEY ID					
		A	B	C	D	E	F
Dimension	Q	6.625	5.625	4.625	3.625	2.625	1.625
	R	1.50	2.50	3.50	4.50	5.50	6.50
	S	14.50	13.50	12.50	11.50	10.50	9.50
	T	1.00	2.00	3.00	4.00	5.00	6.00
	U	14.50	13.50	12.50	11.50	10.50	9.50

FIGURE 10 – M.2 board connector bottom slot details (informative)

4 M.2 keys (informative)

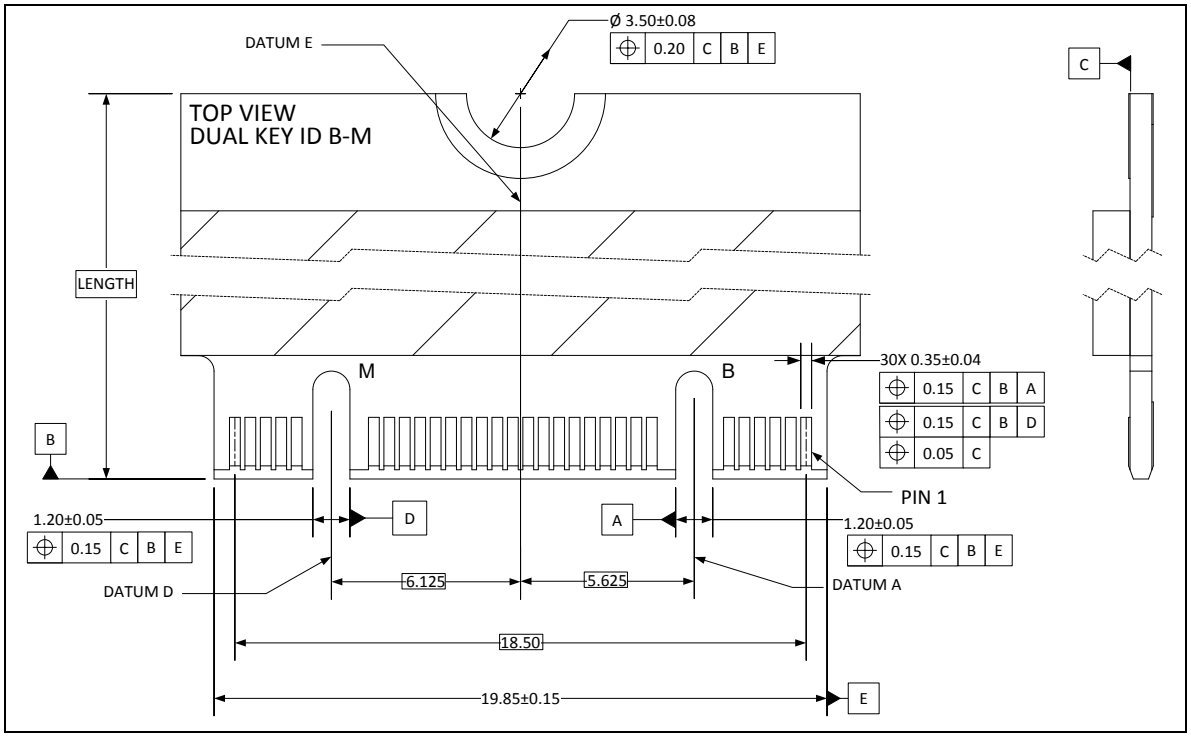


FIGURE 11 - M.2 keys (informative)

There are two mechanical keys defined for SSDs:

a) Key B pinout supports SSD/WWAN/Others:

   A) 1x SATA SSD; or

   B) 1x, 2x PCIe SSD (and WWAN) Host Interfaces;

and

b) Key M pinout supports SSDs only:

   A) 1x SATA; or

   B) 1x, 2x, or 4x PCIe Host Interfaces.

Notch Location for Key B - Pins 12 to 19
Notch Location for Key M - Pins 59 to 66

SSD solutions targeting Key B Host I/F set should also employ two notches that coincide with Key B and Key M to enable these to be pluggable into both Socket 2 and Socket 3 (see 3.1). SSD solutions targeting Key M Host I/F set should only emply Key M notch and can only plug into Socket 3. It is not possible to plug a Key M only device into Socket 2 (with Key B).

3.1 M.2 sockets

Sockets are defined as follows:

a) Socket 1, accepts cards with an “A” key notch present

b) Socket 2, accepts cards with a “B” key notch present and
c) Socket 3, accepts cards with an “M” key notch present.

5 M.2 land pattern for top mount connector motherboard (informative)

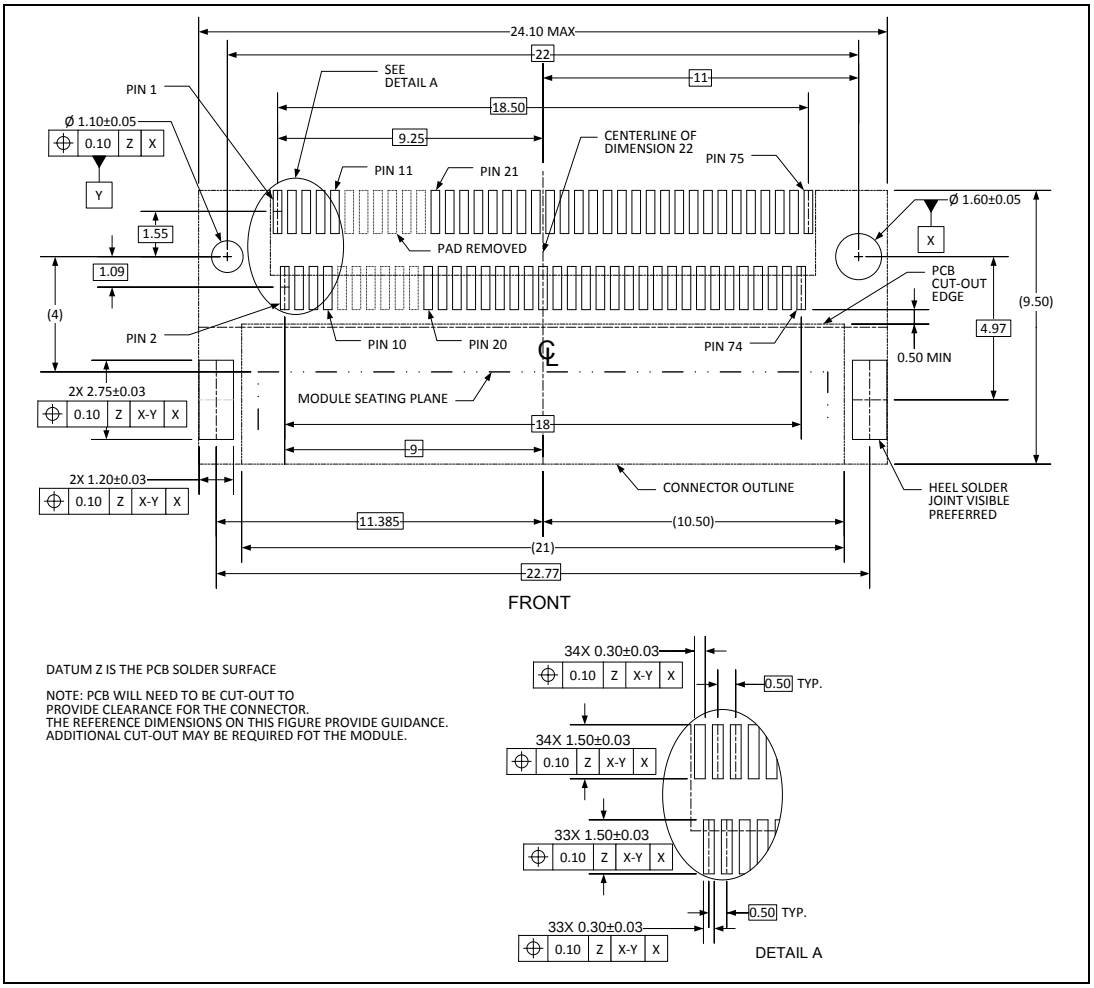


FIGURE 12 - M.2 land pattern for mother board (informative)

6 M.2 Z-height stack up (informative)

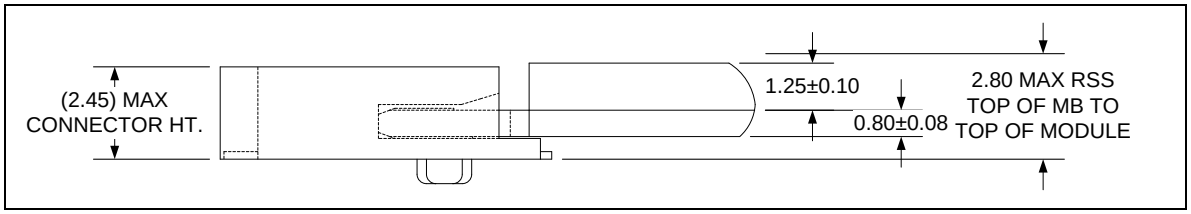


FIGURE 13 - Single sided assembly - S2 profile (informative)

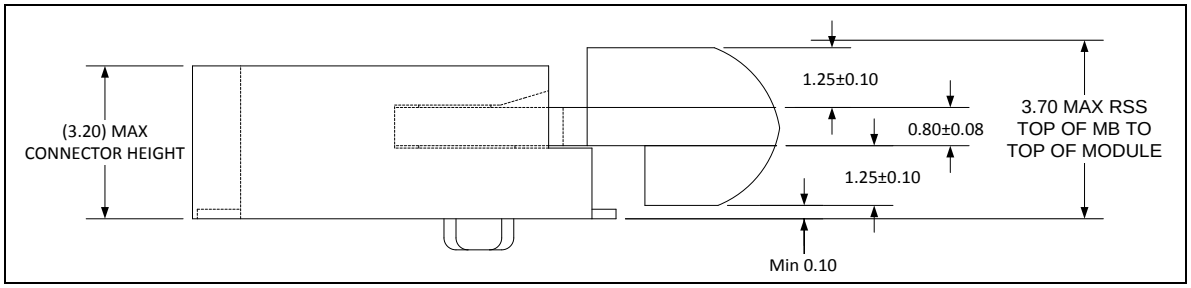


FIGURE 14 - Double sided assembly - D2 profile (informative)

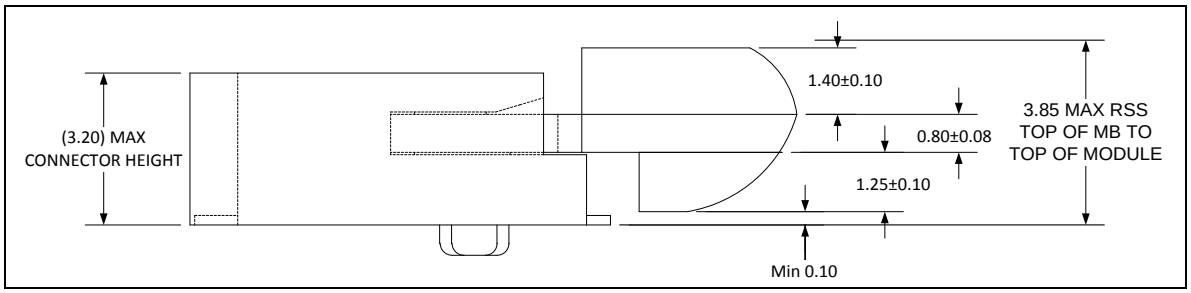


FIGURE 15 - Double sided assembly - D3 profile (informative)

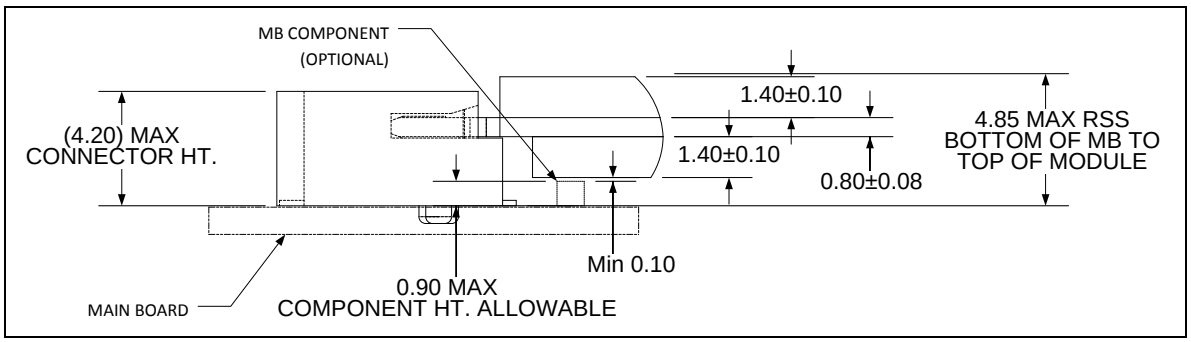


FIGURE 16 - Double sided assembly - D5 profile (informative)

7 M.2 board sizes (informative)

Five board sizes are defined:

a) 30 mm;

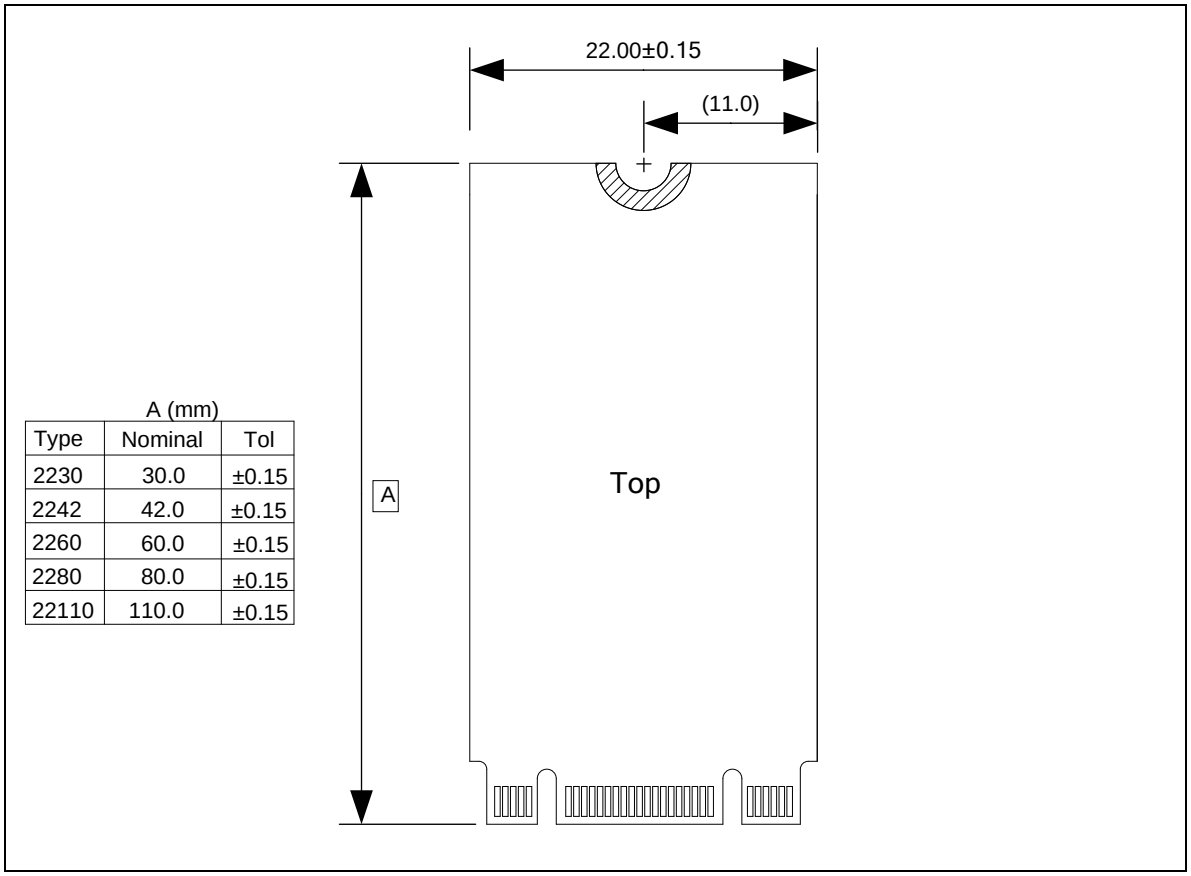
b) 42 mm;

c) 60 mm;

d) 80 mm; and

e) 110 mm,

long as shown in Figure 17 (e.g., with both notch B and notch M present). All boards are nominally 22 mm wide.

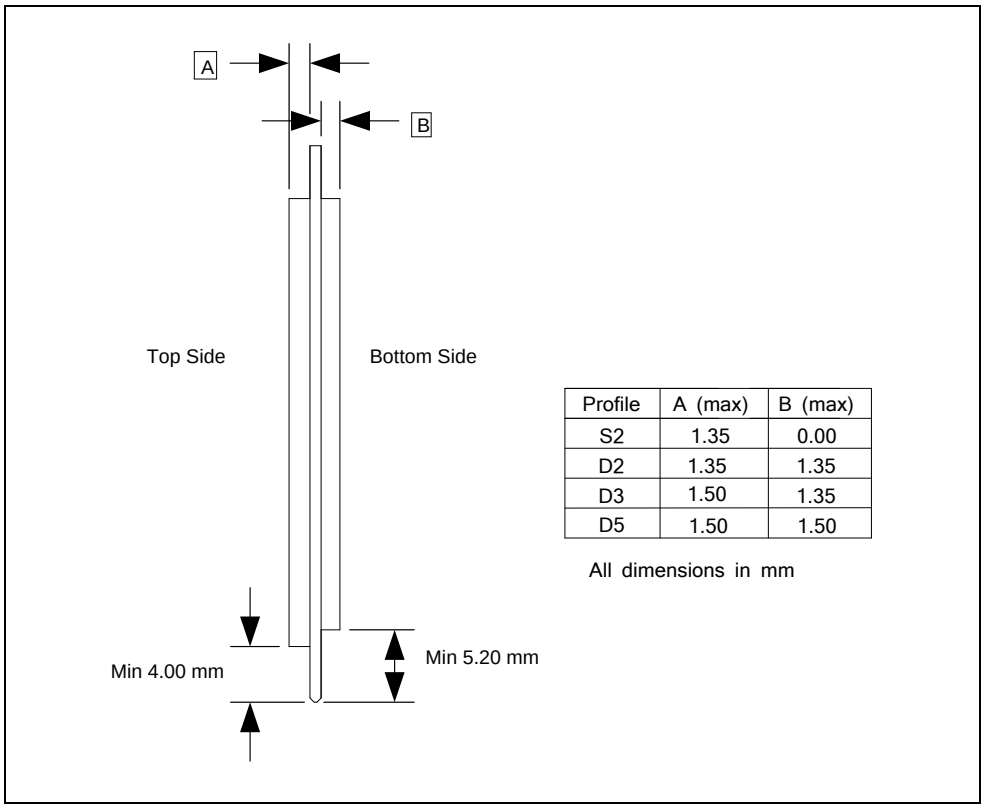


A (mm)		
Type	Nominal	Tol
2230	30.0	±0.15
2242	42.0	±0.15
2260	60.0	±0.15
2280	80.0	±0.15
22110	110.0	±0.15

FIGURE 17 – M.2 board sizes (informative)

7.1 M.2 component placement and board thickness (informative)

Boards may be constructed as a single sided assembly (e.g., for absolute lowest z-height) or as double sided assembly. Four profiles are shown below. Profile S2 is suitable for single sided SSDs. Profile D2 is suitable for SSD-only slots. Profiles D3 and D5 are suitable for slots which target multiple functions (e.g., SSDs or communication cards).



Profile	A (max)	B (max)
S2	1.35	0.00
D2	1.35	1.35
D3	1.50	1.35
D5	1.50	1.50

All dimensions in mm

FIGURE 18 – M.2 component profile and keep out zone (informative)

8 M.2 signal integrity

Table 2 – M.2 connector, electrical requirements

Parameter	Requirement
Differential impedance [a]	75 ohm to 95 ohm measured at 50 ps rise time, from the 20 % threshold to the 80 % threshold
Differential insertion loss [a, b]	≥ -0.5 dB up to 4 GHz and then ≥ -1 dB up to 8 GHz
Differential Near End Crosstalk [a, b, c]	≤ -36 dB up to 4 GHz and then ≤ -32 dB up to 8 GHz
Differential Far End Crosstalk [a, b, c]	≤ -40 dB up to 4 GHz and then ≤ -32 dB up to 8 GHz
[a] Mated connector and module including solder pad and gold finger. [b] The result is referenced to 85 ohm differential impedance. [c] The crosstalk shall be pair to pair between any two differential pairs.	

9 M.2 pad and anti-pad recommendations (informative)

Voiding planes under the pads reduces launch capacitance which improves signal integrity. The values shown in figure 18 are typical of a board constructed with mainstream commercial grade FR-4 PCB material. Dimension of recommended pad sizes are in previous figures.

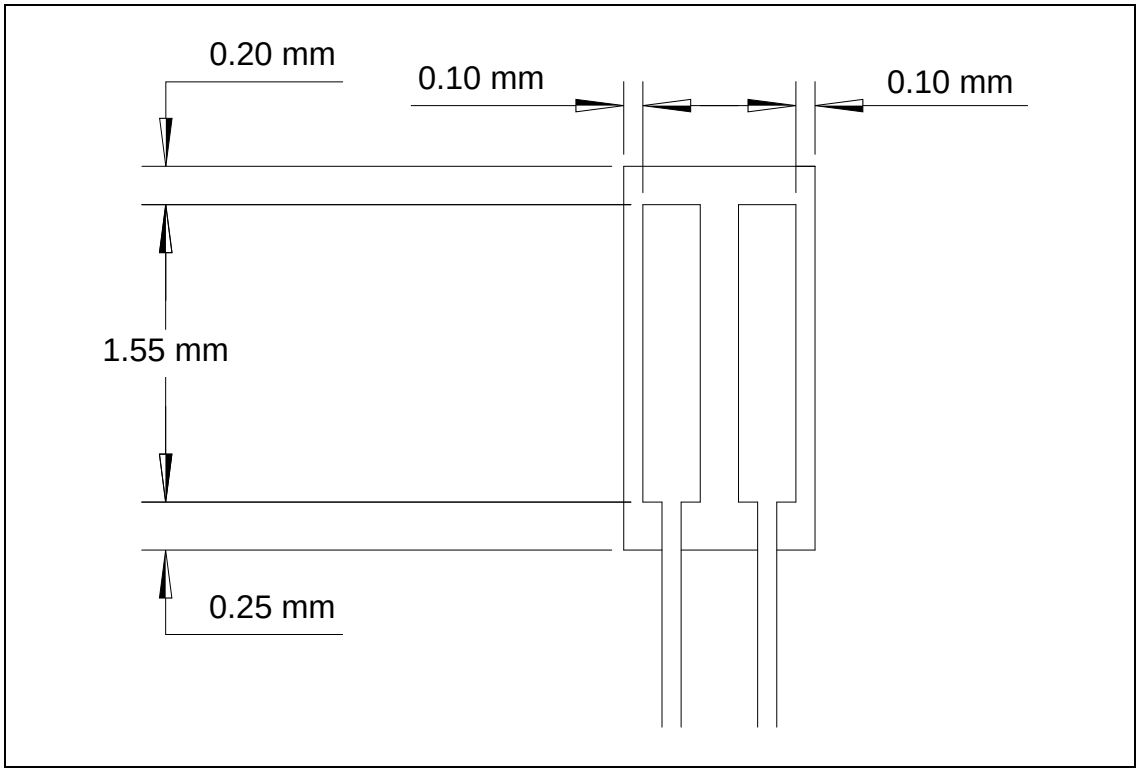


FIGURE 19 - M.2 mother board pad and void dimensions (informative)

10 Minimum plane pull back from finger (informative)

Pad pull back from fingers in a typical FR-4 circuit board should improve signal integrity.

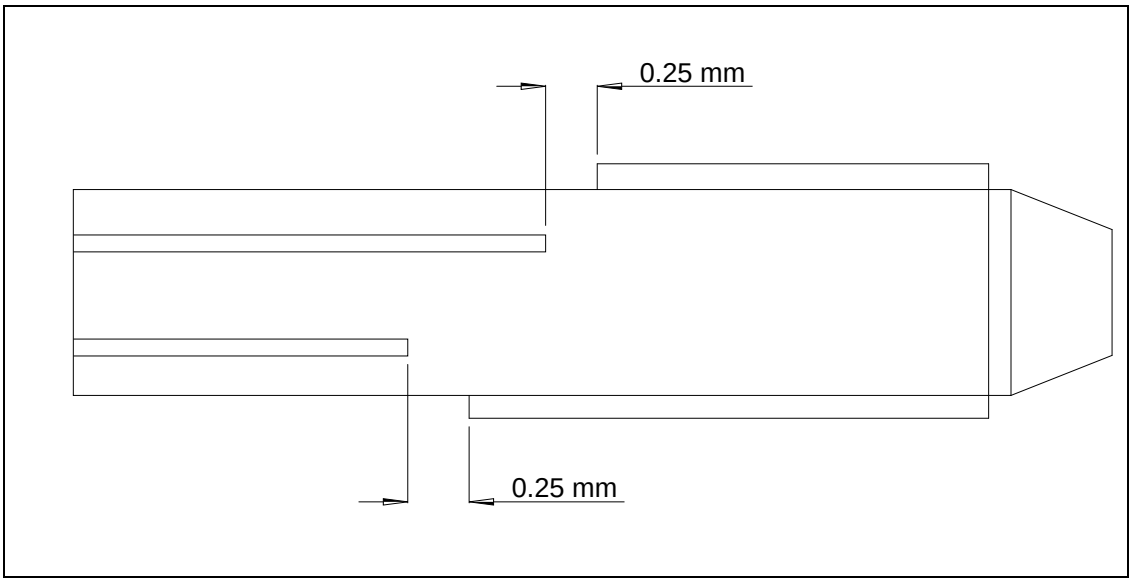


FIGURE 20 – M.2 Pull back (informative)

11 M.2 socket 2 pin definition

Table 3 defines the signal assignment of the internal M.2 connector for device usage. This connector does not support hot plug capability, so there is no connection sequence specified. There are a total of 75 pins. 12 pin locations are used for mechanical key locations; this allows such a module to plug into both Key B and Key M connectors.

Socket 2 supports either a single lane SATA device, or a PCIe device with 1 or 2 lanes.

Pin direction is with respect to the module (i.e., TX (transmit) is a signal driven by the module to the system).

Table 3 – M.2 device side signal assignments for key B (1x SATA, 2x PCIe) (part 1 of 3)

Pin Position	Type	Description
1	CONFIG_3	Defines module type (see 14)
2	3.3 V	Supply pin, 3.3 V
3	GND	Ground
4	3.3 V	Supply pin, 3.3 V
5	No connect	No connect
6	Not Available	No connect (used for other purposes)
7	Not Available	No connect (used for other purposes)
8	Not Available	No connect (used for other purposes)
9	No connect	No connect
10	DAS/DSS	Device Activity Signal / Disable Staggered Spin-up
11	No connect	No connect (used for other purposes)
12	(removed for key)	Mechanical notch B
13	(removed for key)	Mechanical notch B
14	(removed for key)	Mechanical notch B
15	(removed for key)	Mechanical notch B
16	(removed for key)	Mechanical notch B
17	(removed for key)	Mechanical notch B
18	(removed for key)	Mechanical notch B
19	(removed for key)	Mechanical notch B
20	Not Available	No connect (used for other purposes)
21	CONFIG_0	Defines module type (see 14)
22	Not Available	No connect (used for other purposes)
23	Not Available	No connect (used for other purposes)
24	Not Available	No connect (used for other purposes)
25	Not Available	No connect (used for other purposes)
26	Not Available	No connect (used for other purposes)
27	GND	Ground
28	Not Available	No connect (used for other purposes)
29	PERn1	PCIe Signal (see PCIe M.2)
30	Not Available	No connect (used for other purposes)
31	PERp1	PCIe Signal (see PCIe M.2)
32	Not Available	No connect (used for other purposes)

[a] No connect on a host.

Table 3 – M.2 device side signal assignments for key B (1x SATA, 2x PCIe) (part 2 of 3)

Pin Position	Type	Description
33	GND	Ground
34	Not Available	No connect (used for other purposes)
35	PETn1	PCIe Signal (see PCIe M.2)
36	Not Available	No connect (used for other purposes)
37	PETp1	PCIe Signal (see PCIe M.2)
38	DEVSLP	Device Sleep, input. If driven high the host is informing the SSD to enter a low power state
39	GND	Ground
40	Not Available	No connect (used for other purposes)
41	SATA-B+/PERn0	Host receiver differential signal pair. If in PCIe mode see PCIe M.2
42	Not Available	No connect (used for other purposes)
43	SATA-B-/PERp0	Host receiver differential signal pair. If in PCIe mode see PCIe M.2
44	Not Available	No connect (used for other purposes)
45	GND	Ground
46	Not Available	No connect (used for other purposes)
47	SATA-A-/PETn0	Host transmitter differential signal pair. If in PCIe mode see PCIe M.2
48	Not Available	No connect (used for other purposes)
49	SATA-A+/PETp0	Host transmitter differential signal pair. If in PCIe mode see PCIe M.2
50	PERST#	PCIe Signal (see PCIe M.2)
51	GND	Ground
52	CLKREQ#	PCIe Signal (see PCIe M.2)
53	REFCLKN	PCIe Signal (see PCIe M.2)
54	PEWAKE#	PCIe Signal (see PCIe M.2)
55	REFCLKP	PCIe Signal (see PCIe M.2)
56	MFG1	Manufacturing pin. Use determined by vendor. [a]
57	GND	Ground
58	MFG2	Manufacturing pin. Use determined by vendor. [a]
59	(removed for key)	Mechanical notch M
60	(removed for key)	Mechanical notch M
61	(removed for key)	Mechanical notch M
62	(removed for key)	Mechanical notch M
63	(removed for key)	Mechanical notch M
64	(removed for key)	Mechanical notch M
65	(removed for key)	Mechanical notch M
66	(removed for key)	Mechanical notch M
67	Not Available	No connect (used for other purposes)
68	SUSCLK	PCIe Signal (see PCIe M.2)
69	CONFIG_1	Defines module type (see 14)
70	3.3 V	Supply pin, 3.3 V

[a] No connect on a host.

Table 3 – M.2 device side signal assignments for key B (1x SATA, 2x PCIe) (part 3 of 3)

Pin Position	Type	Description
71	GND	Ground
72	3.3 V	Supply pin, 3.3 V
73	GND	Ground
74	3.3 V	Supply pin, 3.3 V
75	CONFIG_2	Defines module type (see 14)

[a] No connect on a host.

12 M.2 SSD SOCKET 3

Slot M supports a one lane SATA device or a PCIe device with 1, 2 or 4 lanes.

Table 4 Signal Assignments for card keyed for slot M (1x SATA, 1x, 2x, or 4x PCIe) (part 1 of 3)

Pin position	Type	Description
1	CONFIG_3	Defines module type (see 14)
2	3.3 V	Supply pin, 3.3 V
3	GND	Ground
4	3.3 V	Supply pin, 3.3 V
5	PERn3	PCIe Signal (see PCIe M.2)
6	Not Available	No connect (used for other purposes)
7	PERp3	PCIe Signal (see PCIe M.2)
8	Not Available	No connect (used for other purposes)
9	GND	Ground
10	DAS/DSS	Device Activity Signal / Disable Staggered Spin-up
11	PETn3	PCIe Signal (see PCIe M.2)
12	3.3 V	Supply pin, 3.3 V
13	PETp3	PCIe Signal (see PCIe M.2)
14	3.3 V	Supply pin, 3.3 V
15	GND	Ground
16	3.3 V	Supply pin, 3.3 V
17	PERn2	PCIe Signal (see PCIe M.2)
18	3.3 V	Supply pin, 3.3 V
19	PERp2	PCIe Signal (see PCIe M.2)
20	Not Available	No connect (used for other purposes)
21	CONFIG_0	Defines module type (see 14)
22	Not Available	No connect (used for other purposes)
23	PETn2	PCIe Signal (see PCIe M.2)
24	Not Available	No connect (used for other purposes)
25	PETp2	PCIe Signal (see PCIe M.2)
26	Not Available	No connect (used for other purposes)
27	GND	Ground
28	Not Available	No connect (used for other purposes)
29	PERn1	PCIe Signal (see PCIe M.2)

[a] No connect on a host.

Table 4 Signal Assignments for card keyed for slot M (1x SATA, 1x, 2x, or 4x PCIe) (part 2 of 3)

Pin position	Type	Description
30	Not Available	No connect (used for other purposes)
31	PERp1	PCIe Signal (see PCIe M.2)
32	Not Available	No connect (used for other purposes)
33	GND	Ground
34	Not Available	No connect (used for other purposes)
35	PETn1	PCIe Signal (see PCIe M.2)
36	Not Available	No connect (used for other purposes)
37	PETp1	PCIe Signal (see PCIe M.2)
38	DEVSLP	Device Sleep, Input. If driven high the host is informing the SSD to enter a low power state
39	GND	Ground
40	Not Available	No connect (used for other purposes)
41	SATA-B+/PERn0	Host receiver differential signal pair. If in PCIe mode see PCIe M.2
42	Not Available	No connect (used for other purposes)
43	SATA-B-/PERp0	Host receiver differential signal pair. If in PCIe mode see PCIe M.2
44	Not Available	No connect (used for other purposes)
45	GND	Ground
46	Not Available	No connect (used for other purposes)
47	SATA-A-/PETn0	Host Transmitter differential pair. If in PCIe mode see PCIe M.2
48	Not Available	No connect (used for other purposes)
49	SATA-A+/PETp0	Host transmitter differential pair. If in PCIe mode see PCIe M.2
50	PERST#	PCIe Signal (see PCIe M.2)
51	GND	Ground
52	CLKREQ#	PCIe Signal (see PCIe M.2)
53	REFCLKN	PCIe Signal (see PCIe M.2)
54	PEWAKE#	PCIe Signal (see PCIe M.2)
55	REFCLKP	PCIe Signal (see PCIe M.2)
56	MFG1	Manufacturing pin. Use determined by vendor. [a]
57	GND	Ground
58	MFG2	Manufacturing pin. Use determined by vendor. [a]
59	(removed for key)	Mechanical notch M
60	(removed for key)	Mechanical notch M
61	(removed for key)	Mechanical notch M
62	(removed for key)	Mechanical notch M
63	(removed for key)	Mechanical notch M
64	(removed for key)	Mechanical notch M
65	(removed for key)	Mechanical notch M
66	(removed for key)	Mechanical notch M

[a] No connect on a host.

Table 4 Signal Assignments for card keyed for slot M (1x SATA, 1x, 2x, or 4x PCIe) (part 2 of 3)

Pin position	Type	Description
67	Not Available	No connect (used for other purposes)
68	SUSCLK	PCIe Signal (see PCIe M.2)
69	CONFIG_1	Defines Module Type (see 14)
70	3.3 V	Supply pin, 3.3 V
71	GND	Ground
72	3.3 V	Supply pin, 3.3 V
73	GND	Ground
74	3.3 V	Supply pin, 3.3 V
75	CONFIG_2	Defines Module Type (see 14)

[a] No connect on a host.

13 Electrical

Signal and 3.3 V Signal Requirements are defined in Table 5.

Table 5 – M.2 voltage and current requirements

Symbol	Parameter	Conditions	Min	Max	Units
+3.3 Vaux [c]	Supply voltage		3.135	3.465	V
V_{IH}	Input high voltage		2.0	3.6	V
V_{IL} [d]	Input low voltage		-0.5	0.5	V
I_{OL} [a]	Output low current for open-drain signals	0.4 V	4		mA
I_{IN}	Input leakage current	0 V to 3.3 V	-10	+10	uA
I_{LKG}	Output leakage current	0 V to 3.3 V	-50	+50	uA
C_{IN}	Input pin capacitance			7	pF
C_{OUT}	Output pin coapacitance			30	pF
T_{RISE} [b]	Power up time			10	ms

[a] Not applicable to LED# and DAS/DSS pins.
[b] Rise time of 3.3 V supply from 0 V to its minimum voltage under maximum load.
[c] Each pin shall be capable of supplying at least 500 mA.
[d] Only applicable to CONFIG pins.

14 M.2 signal definitions, configuration pins

Configuration pins are used to inform the host system the type of card present in a socket. These pins are either 'no connect' or grounded on the card.

Table 6 – M.2 configuration pin settings

Type	CONFIG_0 (pin 21)	CONFIG_1 (pin 69)	CONFIG_2 (pin 75)	CONFIG_3 (pin 1)
SSD - SATA	Ground	Ground	Ground	Ground
PCIe	See PCIe M.2			

15 M.2 mated connector differential impedance (informative)

The purpose of the mated connector impedance requirement is to optimize signal integrity by minimizing reflections. The host may support the use of PCIe or SATA signaling over the same interconnect. The nominal characteristic differential impedance of PCIe is 85 ohm, while the nominal characteristic differential impedance of SATA is 100 ohm.

The differential impedance of a mated connector should be within 90 ohm ±12 ohm, as seen from a 50 ps rise time, measured from the 20 % threshold to 80 % threshold of a differential TDR. The impedance profile of a mated connector should fall within this range. Note that this mated connector differential requirement applies to all the connector mating interfaces defined in the M.2 specification. The measurement includes the connector footprints on both host and device PCBs (backplane application) and the cable connector wire termination area (e.g., cabled application).

16 Documents under development

The following PCI Express® Specification under development is available from http://www.pcisig.org:

a) PCI Express® M.2 Electromechanical Specification, Revision 0.9.March 29, 2013.