Proposed Draft

Serial ATA International Organization

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September 9, 2009

SATA30_TPR_C101_V20
Title: mSATA Connector

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Revision History

Revision	Date	Comments
3	10/09/2008	Initial Proposal to Suppliers
4	11/19/2008	Swapped +B and –B signals to correspond better to typical SATA-IO PCBA layouts.
5	11/20/2008	Moved pin 1 SATA assignment to Pin 30 Moved pin 20 SATA assignment to Pin 32
6	7/21/2009	Updated references to mSATA Update pin assignments to have DA/DSS on pin 49 and PD on pin 51
7	7/22/2009	Updated pin table to specify “Host” side for Transmitter/Receiver
8	8/4/2009	Removed references to PCIe
9	8/4/2009	Renamed to TPR_C101 and added compliance point figure
10	8/5/2009	Added Vendor Pins pin 45, 30, 32
11	8/12/2009	Added two wire interface notes for pins 30 and 32.
12	9/2/2009	Editorial clean up
13	9/3/2009	Adding Lab Loads and Compliance Points
14	9/4/2009	Replaced Figure 1
15	9/4/2009	Adding mSATA connector drawings
16	9/7/2009	Editorial changes
17	9/8/2009	Editorial changes for Figure 124+2 and Figure 125+2, replace Receptacle to Plug
18	9/8/2009	Editorial changes suggested by Alvin Cox
19	9/9/2009	Editorial changes on Figures
20	9/9/2009	Editorial changes, adding references to JC11-MO-XXX and JC11 SO-XXX

Introduction

This proposal is intended to define a new electrical pin-out to allow SATA to be delivered across an mSATA interface connector. This will enable the use of SATA protocol in small form-factor applications where the connectors are readily available in the industry. This proposal is being presented by Lenovo on behalf of Lenovo, SanDisk, Samsung, STEC, and Toshiba.

1 Internal mSATA Connector

This section defines the requirements of an mSATA configuration with a Serial-ATA interface.

The definition supports the following capabilities:

- Supports Gen1 (1.5 Gbps) and Gen2 (3 Gbps) transfer rates
- Support for mSATA
- Support of 3.3 V
- Support 4 vendor pins
- Support 2 vendor pins, for drive or SSD manufacturing usage

1.1 Usage model

The internal mSATA connector is to be used for embedded applications, part of SATA Rev 3 section 5.2.10 Mobile Applications.

(Proposed to be added to Table 2 in the SATA Rev 3 spec – Usage Model Descriptions)

Characteristic	mSATA
Use model section number	5.2.10
Cable and/or backplane type	BP
Cable length	
Cable Electrical	P
Attenuation at 4.5GHz	P
Host-side connector	(To be defined)
Device-side connector	(To be defined)
Gen 1i 1.5Gbps	R
Gen 1m 1.5Gbps	NS
Gen 2i 3.0Gbps	FS
Gen 2m 3.0Gbps	NS
Gen1x 1.5Gbps	NS
Gen 2x 3.0Gbps	NS
Hot plug support	NS

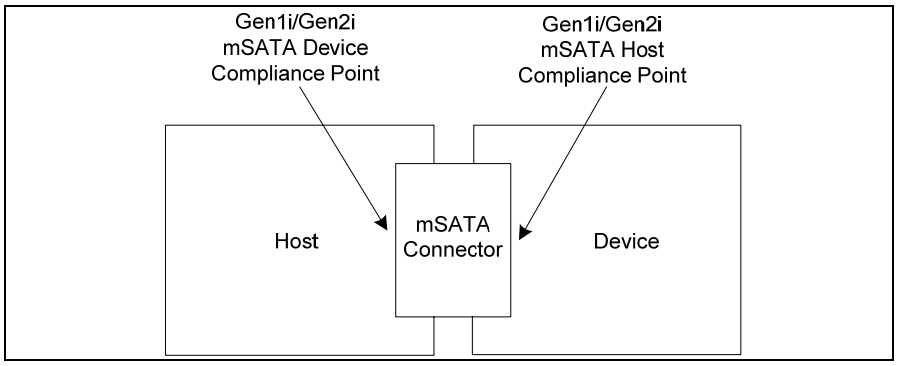


Figure 1: Embedded mSATA Application

1.1.1 Embedded Applications

Applications and compliance points for mSATA devices in the embedded applications are not defined in this specification. The mSATA interface shall comply with Gen1i and Gen2i specifications. The mSATA host and device shall comply with the SATA Rev 3 standard and is equivalent to the Mobile Applications usage model.

1.1.1.1.1 mSATA Lab Load:

Due to the direct connect application of mSATA connection, two different types of mSATA adaptors are required as laboratory loads. The device shall be mated to a female adaptor and the host shall be mated to a male connection as shown in Figure 124+1 and Figure 124+2, respectively.

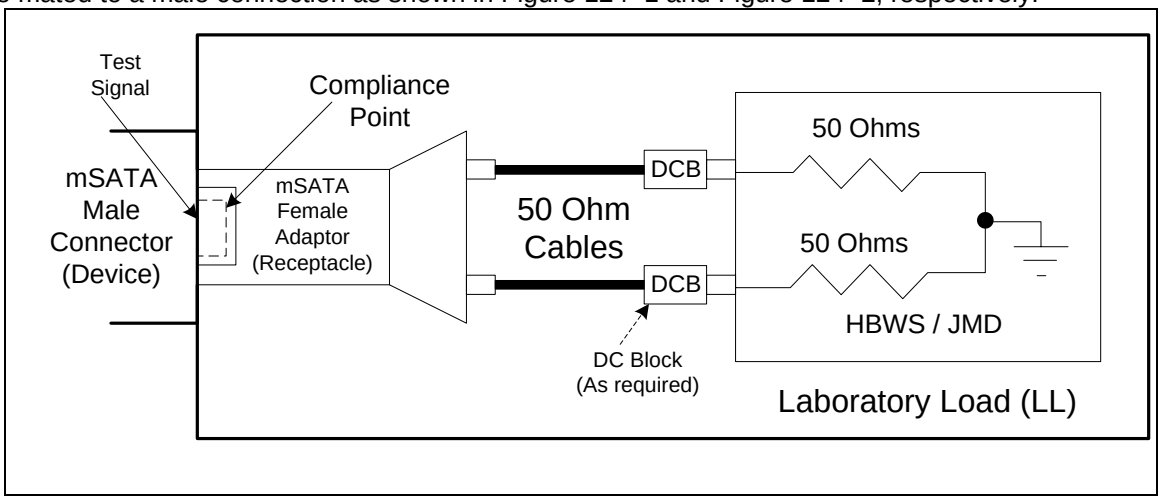


Figure 124+1 – LL Laboratory Load for mSATA Device

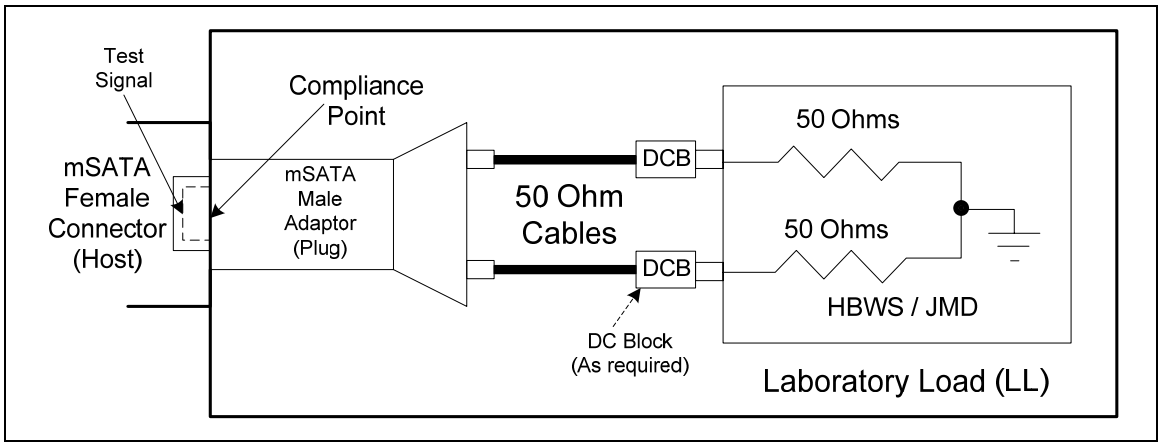


Figure 124+2 – LL Laboratory Load for mSATA Host

The electrical characteristics of the LL shall be greater than the required performance of the parameter being measured such that the LL effects of the on the parameter under test may be successfully compensated for, or de-embedded, in the measured data.

1.1.1.1.2 mSATA Lab Sourced Signal Details

As described in Lab Load Details in 1.1.1.1.1, to properly provide a SATA signal into mSATA device, both female and male type mSATA adaptors are required for device and host, respectively as shown in Figure 125+1 and Figure 125+2.

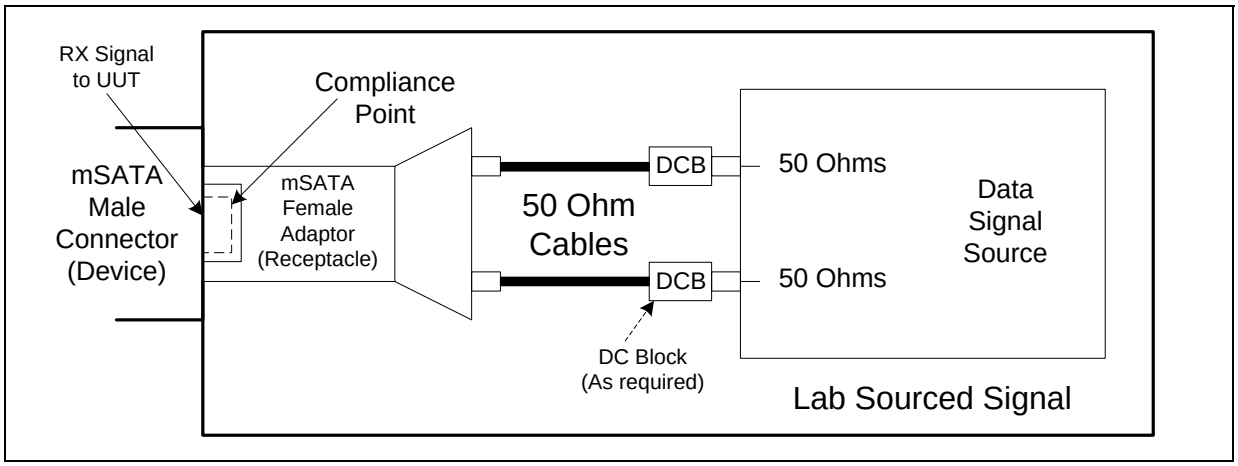


Figure 125+1 – LSS Lab-Sourced Signal for mSATA Device

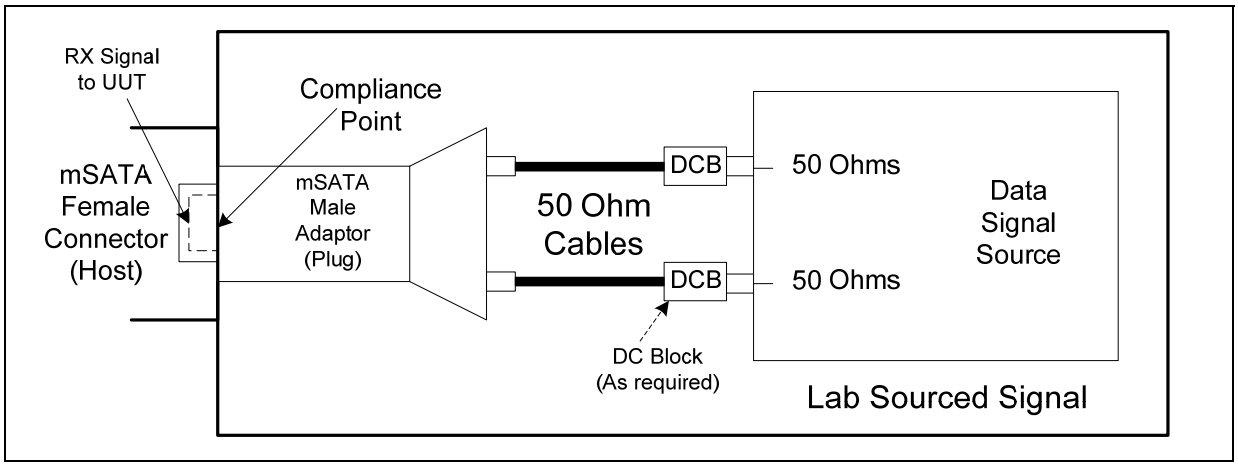


Figure 125+2 – LSS Lab-Sourced Signal for mSATA Host

The Lab-Sourced signal is a laboratory generated signal which is calibrated into an impedance matched load of 100 Ohms differential and 25 Ohms common mode and then applied to the RX+ and RX- signals of the Receiver Under Test. The load used to calibrate the LSS shall have an individual return loss greater than 20 dB over a bandwidth of 100 MHz to 5.0 GHz, and greater than 10 dB from 5 GHz to 8 GHz. During calibration, the characteristics of the Lab-Sourced signal shall comply with the specifications of Error! Reference source not found.. When this signal is then applied to the Receiver Under Test the Frame Error Rate specifications of Table 29 shall be met.

1.1.1.3.1 mSATA Connector Connection Definition

The compliance points of mSATA are shown in Figure 134+1 below. The same concepts of compliance point of SATA extends to the mSATA application. The detailed physical pin dimensions are shown in Figure 134+2.

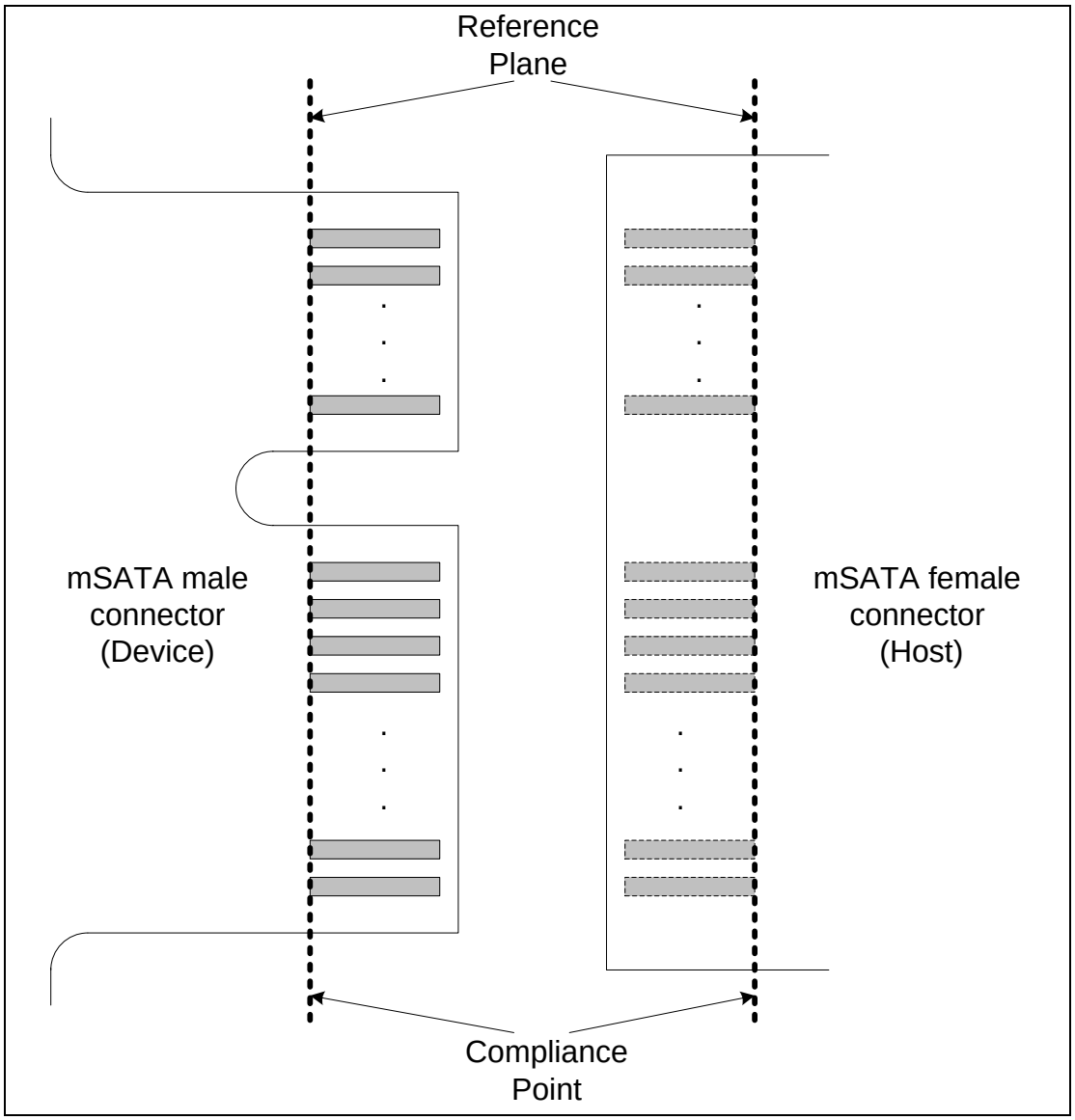


Figure 134+1– Mated Connector Pair for mSATA

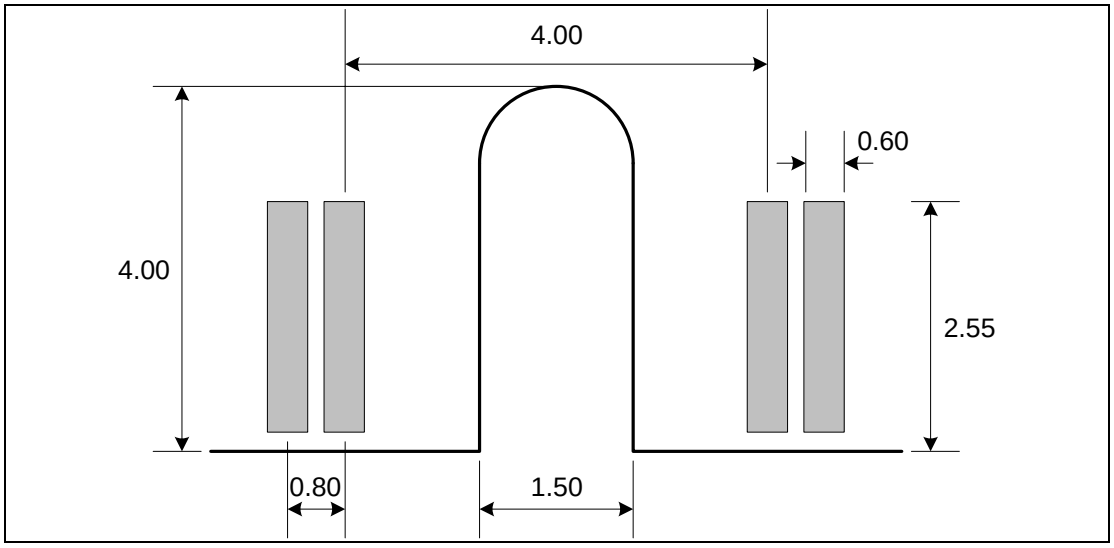


Figure 134+2– mSATA Connector Pin Detail

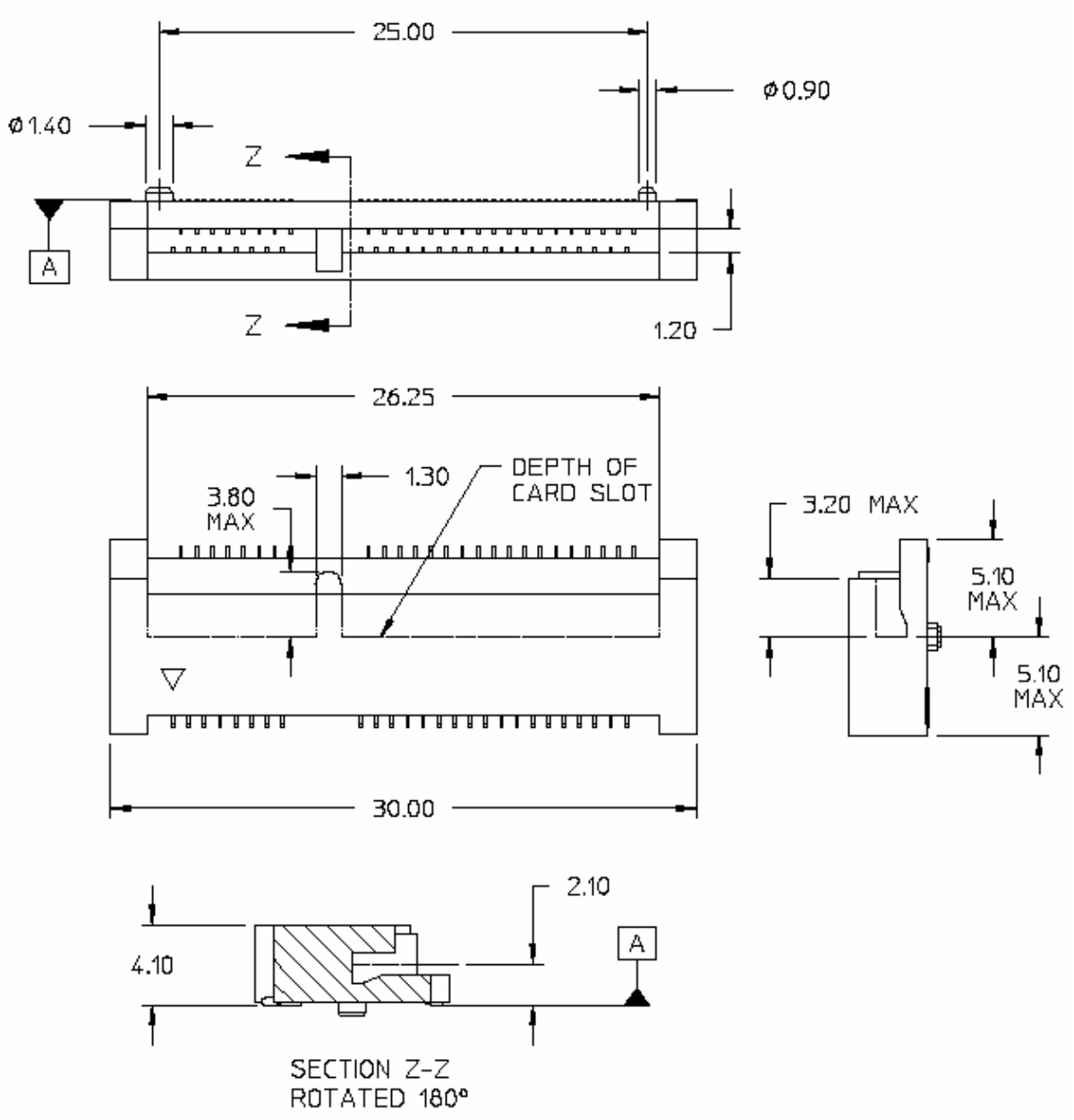
1.2 General description

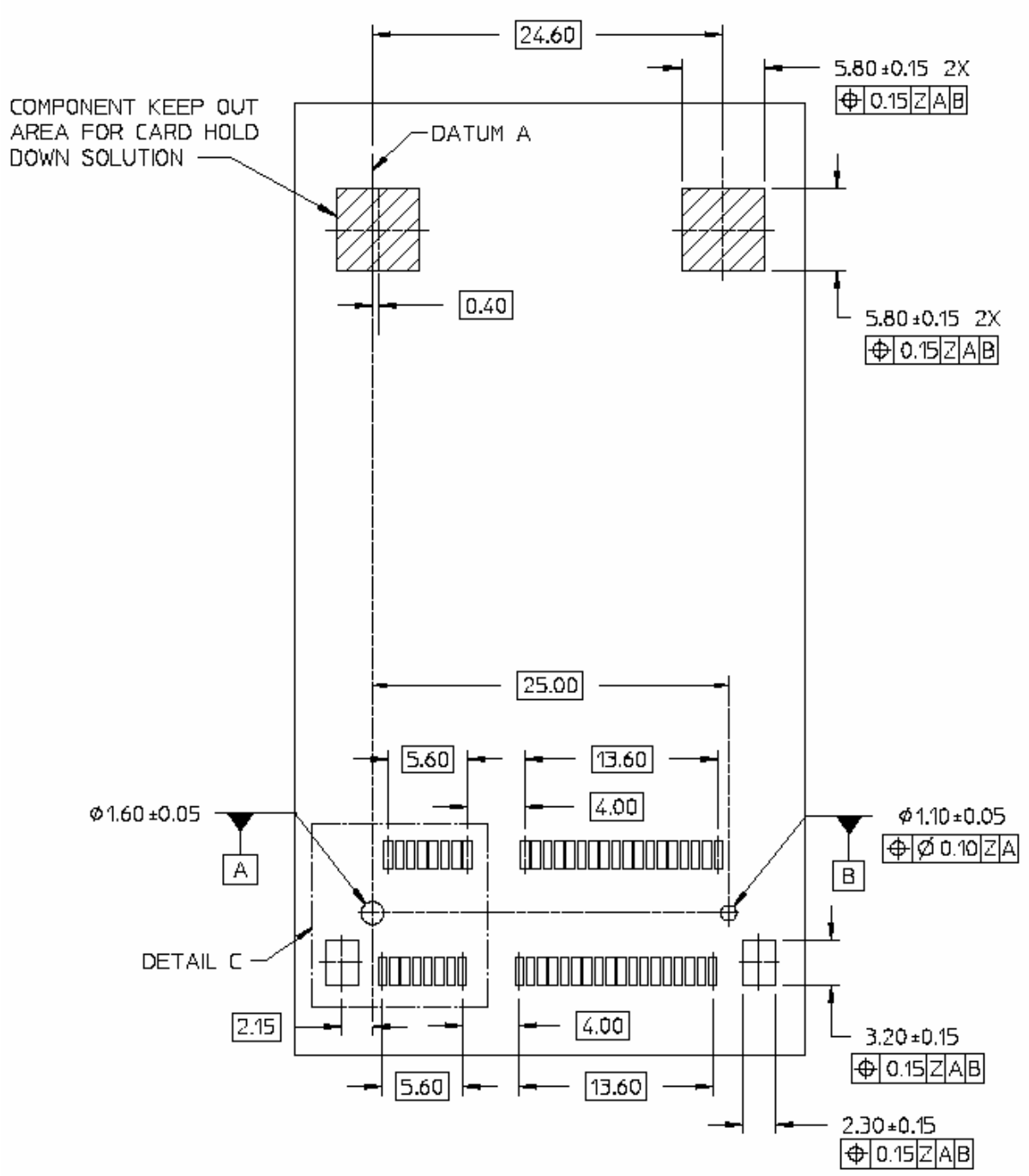
The internal mSATA connector is designed to enable connection of a new family of small form factor devices to the Serial ATA interface.

The signal assignments are outlined in the tables below. The physical dimensions are currently being developed. .

1.3 Connector location on mSATA Form Factor, - (Reference, see JC11, SO-XXX)

The connector location is defined in the drawing below.




24.60
5.80±0.15 2X
⌖ 0.15 Z A B
COMPONENT KEEP OUT AREA FOR CARD HOLD DOWN SOLUTION
DATUM A
0.40
5.80±0.15 2X
⌖ 0.15 Z A B
25.00
5.60
13.60
4.00
ϕ1.60±0.05
A
ϕ1.10±0.05
⌖ Ø 0.10 Z A
B
DETAIL C
2.15
4.00
3.20±0.15
⌖ 0.15 Z A B
5.60
13.60
2.30±0.15
⌖ 0.15 Z A B

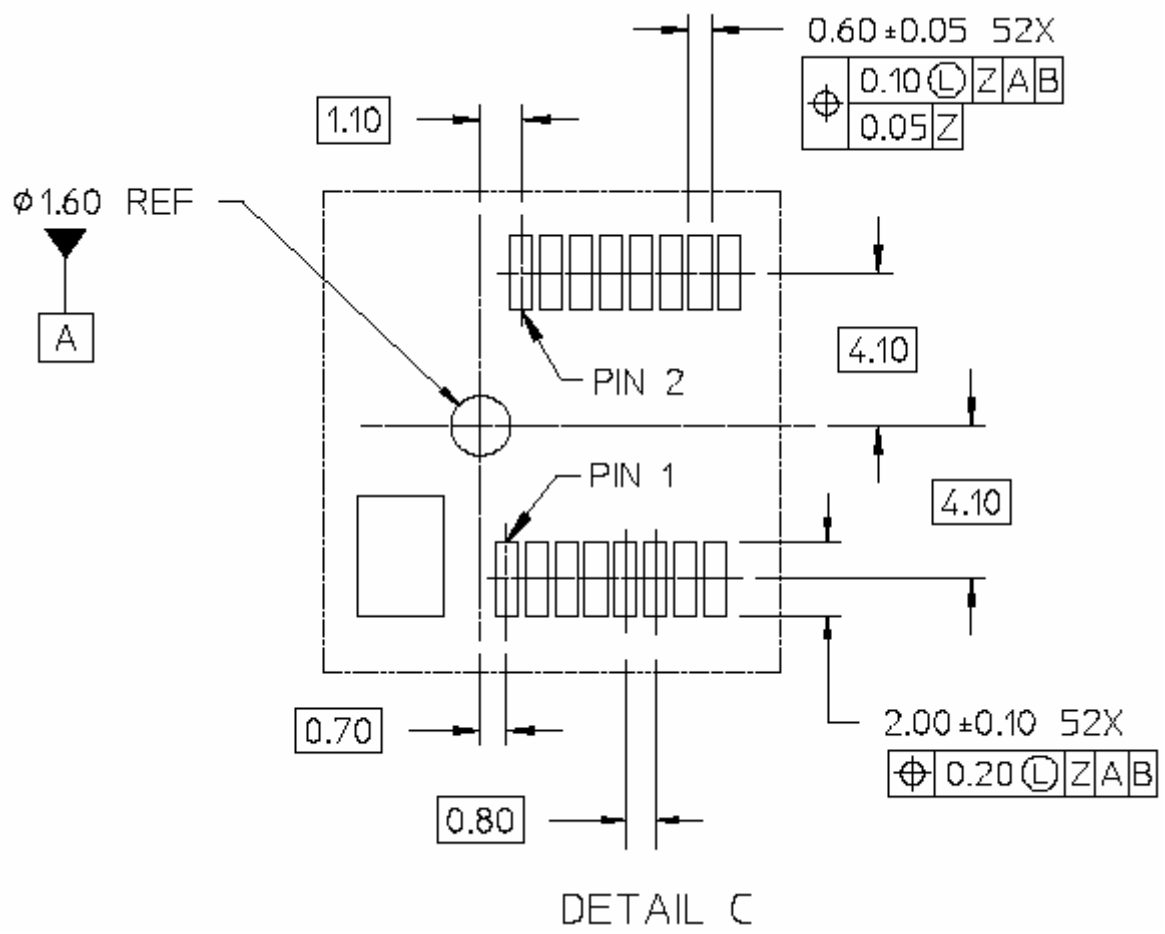
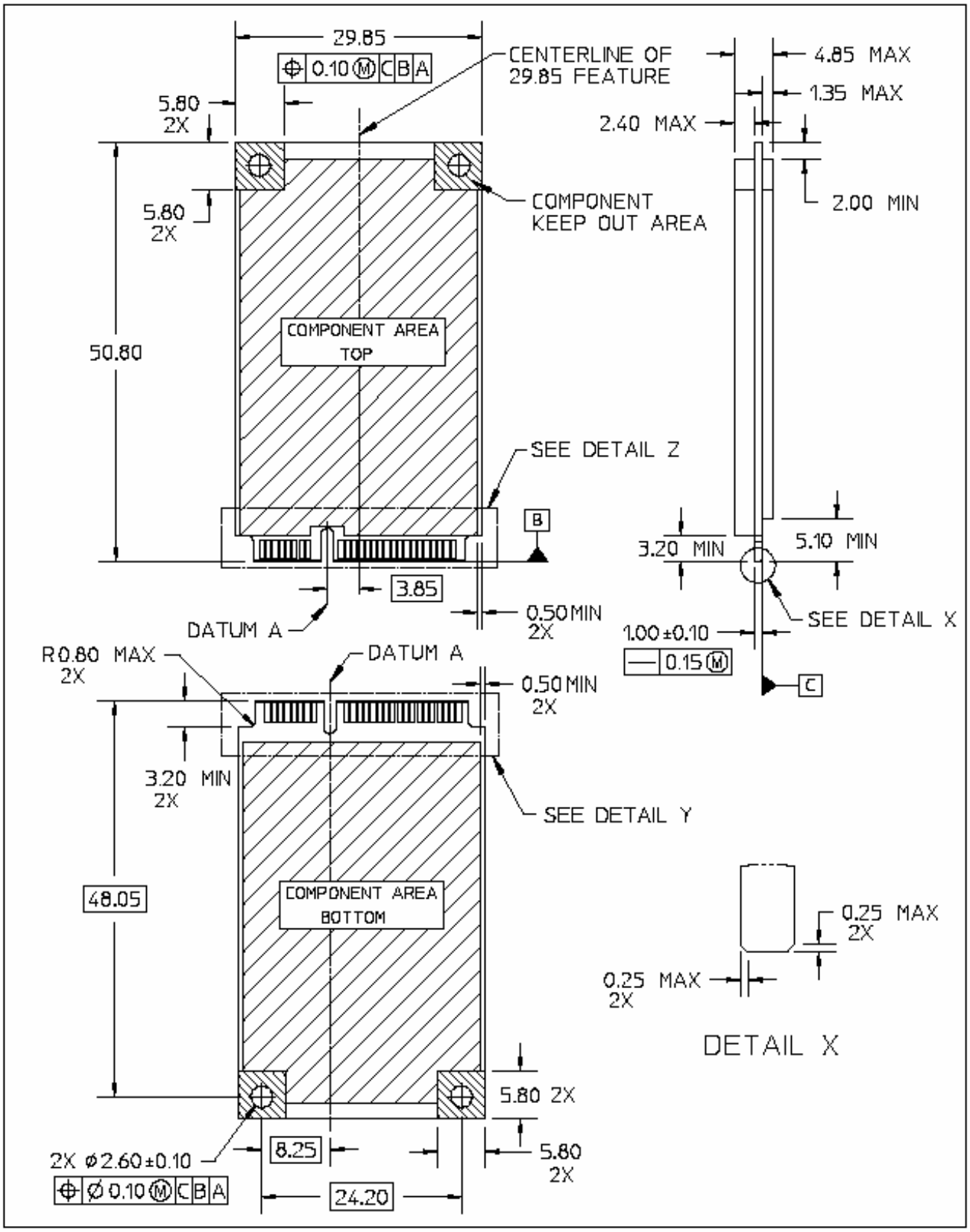


Figure 2 Internal mSATA Card connector location

1.4 Mating interfaces

1.4.1 Device internal mSATA Card embedded type connector, (Reference, see JC11, MO-XXX)

Figure 3 defines the interface dimensions for the internal mSATA connector.


29.85
0.10 M C B A
CENTERLINE OF
29.85 FEATURE
5.80
2X
5.80
2X
COMPONENT
KEEP OUT AREA
COMPONENT AREA
TOP
50.80
SEE DETAIL Z
B
3.85
DATUM A
0.50 MIN
2X
4.85 MAX
1.35 MAX
2.40 MAX
2.00 MIN
3.20 MIN
5.10 MIN
SEE DETAIL X
1.00±0.10
0.15 M
C
R0.80 MAX
2X
DATUM A
0.50 MIN
2X
3.20 MIN
2X
SEE DETAIL Y
48.05
COMPONENT AREA
BOTTOM
0.25 MAX
2X
0.25 MAX
2X
DETAIL X
5.80 2X
2X ø2.60±0.10
ø 0.10 M C B A
8.25
5.80
2X
24.20

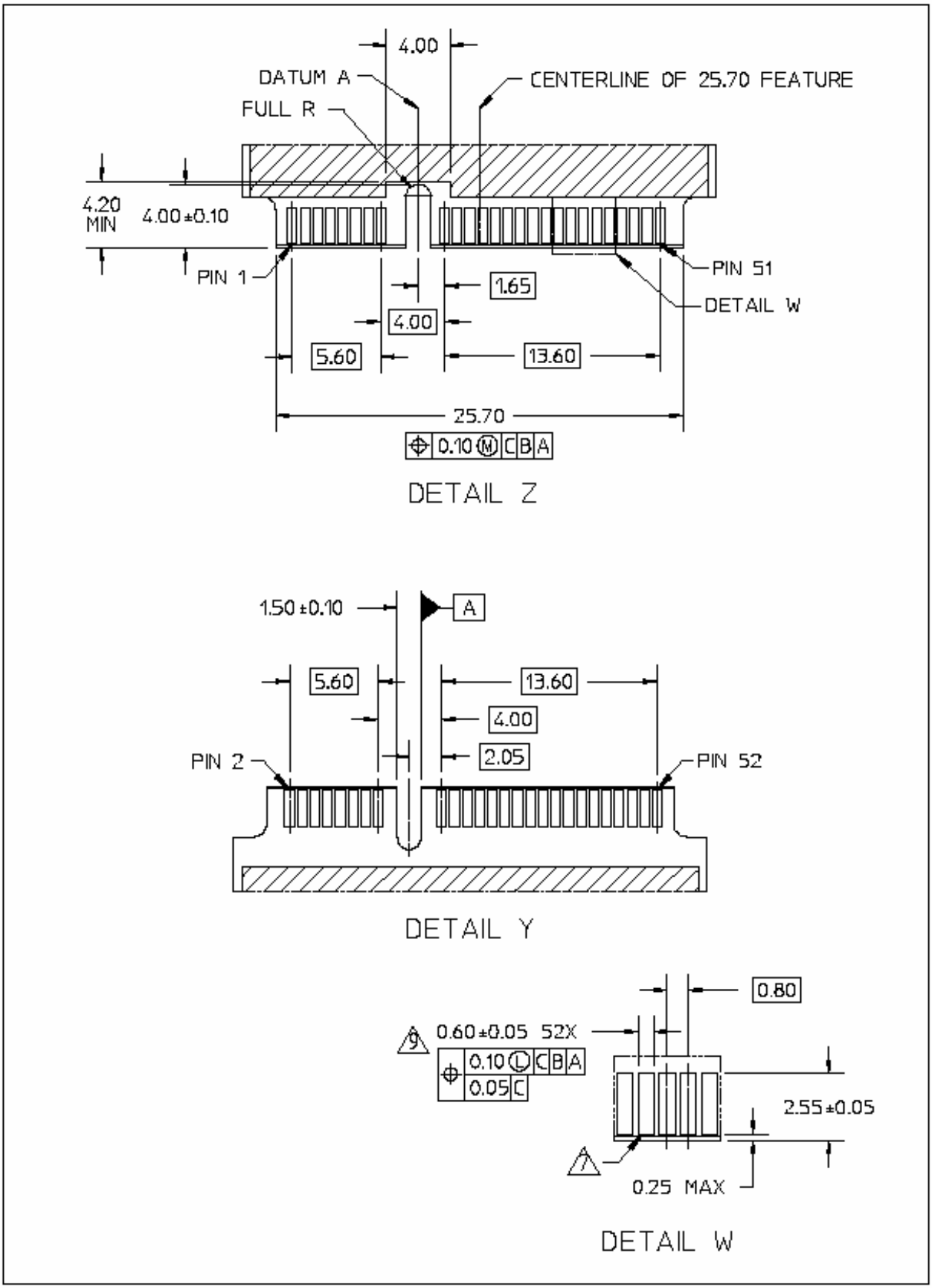


Figure 3 Device internal mSATA Card type internal connector

1.4.2 Internal mSATA pin signal definition

Table 1 defines the signal assignment of the internal mSATA connection. This connection does not support hot plug capability, so there is no connection sequence specified. There are a total of 52 pins.

- 5 pins for 3.3V source
- 3 pins for 1.5V source
- 14 pins for GND
- 4 pins for transmitter/receiver differential pairs
- 1 pin for device activity / disable staggered spin-up
- 1 pin for presence detection
- 2 pins for Vendor Specific / Manufacturing
- 5 pins for Vendor Specific
- 17 reserved pins (no connect)

Table 1 Signal Assignments for mSATA (proposed)

Pin #	Type	Description
P1	Reserved	No Connect
P2	+3.3V	3.3V Source
P3	Reserved	No Connect
P4	GND	Return Current Path
P5	Reserved	No Connect
P6	+1.5V	1.5V Source
P7	Reserved	No Connect
P8	Reserved	No Connect
P9	GND	Return Current Path
P10	Reserved	No Connect
P11	Reserved	No Connect
P12	Reserved	No Connect
P13	Reserved	No Connect
P14	Reserved	No Connect
P15	GND	Return Current Path
P16	Reserved	No Connect
P17	Reserved	No Connect
P18	GND	Return Current Path
P19	Reserved	No Connect
P20	Reserved	No Connect
P21	GND	Return Current Path
P22	Reserved	No Connect
P23	+B	Host Receiver Differential Signal Pair
P24	+3.3V	3.3V Source
P25	-B	Host Receiver Differential Signal Pair
P26	GND	Return Current Path
P27	GND	Return Current Path
P28	+1.5V	1.5V Source
P29	GND	Return Current Path
P30	Two Wire Interface	Two Wire Interface Clock[3]
P31	-A	Host Transmitter Differential Signal Pair
P32	Two Wire Interface	Two Wire Interface Data[3]
P33	+A	Host Transmitter Differential Signal Pair
P34	GND	Return Current Path
P35	GND	Return Current Path
P36	Reserved	No Connect
P37	GND	Return Current Path
P38	Reserved	No Connect
P39	+3.3V	3.3V Source
P40	GND	Return Current Path
P41	+3.3V	3.3V Source

P42	Reserved	No Connect
P43	GND	Return Current Path
P44	Reserved	No Connect
P45	Vendor	Vendor Specific / Manufacturing Pin[2]
P46	Reserved	No Connect
P47	Vendor	Vendor Specific / Manufacturing Pin[2]
P48	+1.5V	1.5V Source
P49	DA/DSS	Device Activity Signal / Disable Staggered Spin-up
P50	GND	Return Current Path
P51	Presence Detection	Shall be pulled to GND by device[1]
P52	+3.3V	3.3V Source

NOTE:
1. Presence detection pin provided for tamper proof functionality
2. No connect on the host side.
3. Pins 30 and 32 are intended for use as a two wire interface to read a memory device to determine device information (an example of this would be for use as SMB bus pins). These pins are not designed to be active in conjunction with the SATA signal differential pairs.