Serial ATA Interoperability Program Revision 1.2
SyntheSys Research, Inc. MOI for RSG Tests
(using BERTScope 7500B with CR)

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MODIFICATION RECORD

Version 0.8, April 11, 2007
Version 0.9, April 26, 2007; Added Grab mode to track disparity and count re-synchronizations to the pattern to get FER; Added “While the Interop testing require the use of the Pretest_MOI_Framed_COMP” and “informatively” to the last paragraph on page 10; Moved Host Worst Port Identification to Appendix with the addition of the following text: “The “worst port” identified during a Pre-test should be used. If pre-test has not yet been run then the following method, which follows and complies with the pre-test “worst port” identification procedure, is applied prior to execution of any testing on a host.”
Version 0.91, July 23, 2007; Added the words “with an initial amplitude of 1 Vpp” and “determined during calibration” to respectively steps 4 and 9 and changed “desired data rate” to “maximum claimed data rate” in steps 2 and 3 of the test procedure.
Version 0.92, August 2, 2007; deleted “Testing results gathered for 33 MHz are informative.”
Version 1.0, merely removed “RC” after workgroup approval and end of 30 day review.
INTRODUCTION

These Methods of Implementations describe the step by step procedures to perform the RSG-01 through RSG-02 tests of the Serial ATA Interoperability Program using the BERTScope by SyntheSys Research, Inc. to qualify a product, host or device, for listing on the SATA Integrators List. Described methods can test products which support disconnect as well as products without support of disconnect.

The test setup is illustrated in Appendix B.

The Framed COMP pattern used for Interoperability Testing is that which is compliant with the definitions of SATA Revision 2.6 and approved ECNs against Revision 2.6.

The tests can be performed in automated fashion using Jitter Tolerance software available on the BERTScope. Please contact SyntheSys Research, Inc. at +1 (650) 364-1853 or info@bertscope.com for the latest information on such software.
REFERENCES

The following documents are referenced in this text:

[1] Serial ATA version 2.6, SerialATA_Revision_2_6.pdf
[4] SATA_PHY_MOI_BERTScope_PHY_TSG_OOB_r12_v0_8.doc

The most current versions of above documents may be found at the Serial ATA document repository:
http://www.serialata.org/testing.asp

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The SATA-IO would like to acknowledge the efforts of the following individuals in the development of:

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Test Title: RSG-01 Gen1 (1.5Gb/s): Receiver Jitter Test and
Test Title RSG-02 Gen2 (3Gb/s): Receiver Jitter Test

Purpose: Verify that the Product Under Test, PUT, meets the receiver tolerance specification of sections 7.2.2.6.7 and 7.3 of Serial ATA Revision 2.5 at 1.5 Gb/s and sections 7.2.2.6.8 and 7.3 of Serial ATA Revision 2.5 at 3 Gb/s if the PUT claims to support both rates.

Resource Requirements:
- See Appendix C

Signal Calibration:
- The setup shall be calibrated using the Calibration section of this document prior to start of the test as the calibrated settings are used throughout the test.

Last Modification: July 23, 2007

Discussion: This requirement is tested only at the highest interface rates which the PUT claims to support, i.e. either at 3Gb/s or 1.5 Gb/s. The BERTScope automatically steps the jitter frequency and verify according to section 7.2.2.1.3 of the Serial ATA revision 2.5. Described methods can test product which support as well as products without support of disconnect.

During the testing execution for all RSG test requirements, it is essential that the product under test be able to complete an initial OOB sequence through the device COMWAKE prior to transmission of a BIST FIS or initiation of the BIST mode sequence. This is to allow product calibration to occur prior to and/or during the initial power on and detect sequences.

There are several different patterns defined within the specification and are intended to be used to verify this requirement. In order to ensure efficient test time of products within the Interoperability Testing, testing of this requirement will be limited to the Framed Long COMP. For consistent transmission of the Framed Long COMP pattern, it is required that 2 ALIGNs are transmitted prior to SOF of the frame, and then subsequently every 256 Dwords. The Framed Long COMP pattern as well as the Pretest_MOI_Framed_COMP pattern in the SATA directory on the BERTScope contain these features.

Test Setup as shown in Appendix B: Connect the CR 12500A sub-rate clock output to the BERTScope clock input using the short SMA Male to SMA Male Cable. Connect the CR 12500A full rate clock output to the BERTScope external clock input using the medium length SMA Male to SMA Male Cable. Connect the Data Output + and - ports of the CR 12500A to the Data Input + and – ports of the BERTScope using the matched pair of cables. Connect the CR 12500A Data Input + and – ports to the respective Instrument RX + and - ports of the SATA Tee via one of the pairs of matched of SMA Male to Male Cables. Connect the Instrument TX + and – ports of the SATA Tee to the respective BERTScope Data Output + and – ports via one of the pairs of matched of SMA Male to Male Cables. Connect the iSATA receptacle-to-SMA-adapter via the four SMA Male to SMA Male adapters to the PUT side of the SATA Tee. The A+ and A- ports of the iSATA receptacle, these are the pins marked 2 and 3 respectively, would be connected to the respective PUT RX Input + and - ports of SATA Tee for drive testing (to PUT TX for host testing). The B+ and B- ports of the iSATA receptacle, these are the pins marked 6 and 5 respectively, would be connected to the respective PUT TX Input + and - ports of SATA Tee for drive testing (to PUT RX for host testing).

Test Procedure:
1. Connect the PUT to the setup via the iSATA receptacle
2. Initiate the PUT in the BIST L mode at the maximum claimed data rate as described in Appendix A. Note: In most cases the BERTScope with the SATA Tee and either a drive or USB adapter can do this as per Appendix A.
3. On the BERTScope, select “View” then “Generator”. Click on the “Generator” box then “User Pattern” and “Load User Pattern” and select the “Pretest_MOI_Framed_COMP” pattern from the “SATA II” folder. Set the “Synthesizer” frequency to match the claimed data rate. Enable the data outputs at or above the desired amplitude, which was determined during calibration.
4. Once the BERTScope data output ports have been enabled with an initial amplitude of 1 Vpp then move the switch on the SATA Tee to the BERTScope position (this can be done either manually or via the electronic input on the SATA Tee).

5. On CR 12500A, choose the appropriate pre-stored selection: “SATA1 (1.98)” for 1.5 Gb/s or “SATA2 (1.98)” for 3 Gb/s; by pressing “Enter”, scroll to the desired setting and press “Enter” again. On the CR 12500A also set the sub-rate clock divider to 1 by scrolling to “SubDiv: 4” press “Enter” select “1” and press “Enter” again.

6. Once the CR 12500A is locked then click the switch in the BERTScope “Generator View” to select “External Clock Input” The PUT input data rate will now be identical to the PUT data output rate.

7. On the BERTScope, select “View” then “Detector” and click on “Auto Align”.
A pop-up window will appear with the Unit Interval measurement result.

8. The detector should be running at zero bit error rate when an un-jittered signal is presented. Set the “Detector” “Pattern” to “Grab” (it will by default grab the length of the Pretest Framed_COMP pattern while now tracking the disparity of the pattern returned by the PUT. The number of Resyncs will be recorded as frame error rate, FER. Verify that the PUT is in loopback mode by injecting a single error from either the “Generator” or “Detector” view and detect that one or more errors occur as a result of the transmitted error.

9. Decrease the generator amplitude to the desired level determined during calibration and start the “Jitter Tolerance” configuration, which was saved during calibration, associated with the data rate being tested. The Jitter Tolerance software will automatically step through and make the jitter tolerance tests 20 minutes at of the 3 jitter frequencies:

- 10 MHz
- 33 MHz
- 62 MHz
10. The test takes approximately 1 hour and 8 seconds. Record the measured error rates; these are displayed in the Jitter Tolerance Table View.
**Observable Results:** The pass/fail criteria are:
- Test is run for 20 minutes and verified to exhibit no more than zero frame errors at each of the 10 MHz, 33 MHz and 62 MHz frequencies above.

**Accuracy:** FER confidence depending on the total test time, 20 minutes test without error at each setting was selected for Serial ATA LOGO testing.

**Possible Issues:** While the Interop testing require the use of the Pretest_MOI_Framed_COMP if the device does not support the Pretest_MOI_Framed_COMP then the COMP_Framed_RD- pattern, which also comply with the 256 word ALIGN spacing, may be used to informatively verify the receiver tolerance level of the PUT. Location of bit errors within the frame may be monitored in the “Pattern Sensitivity” view.
Calibration

**Purpose:** Calibrate the test setup before making any RSG-01 or RSG-02 tests.

**Resource Requirements:**
- See Appendix C

**Last Modification:** April 11, 2007

**Discussion:** This calibration must be done prior to running any RSG-01 or RSG-02 tests.

Tester must save all the calibration data (i.e. screen shot) that is done daily at a minimum, if not for every device evaluation. Valid calibration data must be available per product for review, even if the same calibration data (i.e. daily) is used for multiple products. It is required that calibration be completed for this area of testing to ensure consistent measurements and environment impacts.

The reference plane is the end of the 50 ohm SMA cables that will be connected to the SATA-SMA test fixture.

The following parameters are to be used for creating the appropriate input source involved in the RSG tests (see Table 24 in Section 7.2.1 of SATA Revision 2.5 for specification requirements):
- No SSC
- Pre-emphasis: 0 dB
- No CDR (Clock Data Recover unit) to be used for jitter calibration. The BERT detector uses a 1.5 or 3 GHz square wave direct from the clock output dependent on the data rate.
- Rise/Fall Time : 100 ps (20/80%)

**Test Setup:** as shown in Appendix B and further described in Test Titles RSG-01 and RSG-02 with the exception that the SATA Tee Output + and – ports (which usually are connected to the Comax adaptor) will be connected directly to the BERTScope Data Input + and – ports and the BERTScope Clock Output + will be connected to the BERTScope Clock Input port to provide the direct clock as required for Interop calibration.

**Calibration Procedure:**

The following high level procedure is used to implement the defined Receiver Tolerance test:

1. Turn the BERTScope clock on at 1 V nominal amplitude and the desirable data rate 1.5 GHz or 3 GHz.

![Diagram](image)

2. Select the Mid Frequency Test Pattern (MFTP) from the “Generator” view with an approximate differential voltage of 325 mV for 1.5 Gb/s or 275 mV for 3.0 Gb/s for the RJ calibration. The MFTP is stored as a “User Pattern” in the “SATA II” directory.
3. Verify that the rise and fall times are approximately 100 ps 20%/80%.
4. Select to have the “Stress” show as a side bar in the “Jitter Peak” view. Adjust the Random Jitter (RJ) using (MFTP) pattern until the “Jitter Peak” measures 0.18 UI total random jitter.
   i. NOTE: Gen1 : 8.57 ps RMS (1 sigma for a 7 sigma 0.18 UI projection)
   ii. NOTE: Gen2 : 4.285 ps RMS (1 sigma for a 7 sigma 0.18 UI projection)
5. On the BERTScope, select “View” then “Physical Layer Test” and “Jitter Peak” and click on “Auto Align”. Click “Yes” to perform delay line calibrations if prompted by a pop-up window. Wait until at least three points has been measured on each side of the Jitter Peak and record the TJ value in UI (DJ may be recorded at the same time as this completes the TSG-12 measurement as well).

The measurement units can be altered from pico seconds to UI by right click on “Total Jitter” on the left side bar; then click on “Configure”, select “Percentage Unit Interval”, click “OK”. 
6. All calibration screen shots need to be saved. This is done by clicking on “Print” and select “Print to file” then create a unique file name for each calibration data including the serial number of the equipment.

7. Add Deterministic Jitter (DJ) using the internal BERTScope sinusoidal jitter (SJ) source on top of the existing RJ source using the Pretest_MOI_Framed_COMP pattern for a total of 0.45 UI total.

8. Finally using “Q-Factor” view with the “Data Generator” sidebar enabled adjust the amplitude so that the Differential Voltage of the smallest bit (LBP portion of TSG-01 method) is respectively: 325 mV (1.5Gb/s), or 275 mV (3 Gb/s). Confirm that the maximum differential voltage does not exceed 600 mV for 1.5 Gb/s or 750 mV for 3.0 Gb/s respectively. The resulting signal must have a Total Jitter (TJ) amount of 0.45 UI, while meeting the required parameters outlined in section 2.16 (namely Rise/Fall Time, Voltage etc.).

9. Record the jitter settings and enter these in the Jitter Tolerance Template Builder. Set the “Jitter Tolerance” “Test Limit” to 1200 seconds (20 minutes) and save the calibrated configuration.

The above steps must be repeated and validated on the product under test for the frequencies listed below. The signal must be calibrated at each frequency by adjusting the SJ amplitude to get the desired DJ. The stored Jitter Tolerance Template configuration will run the RSG test automatically at the 3 jitter frequencies for 20 minutes each.
Appendix A: BIST

Initiation of PUT using BIST L mode.

**Purpose:** Place the PUT in the BIST L mode as an initiation before the BERTScope measurements.

**References:**
1. Serial ATA version 2.5, SerialATA_Revision_2_5_RC.pdf, section 10.3.9 BIST Active
2. U-Link Operating Help Files
3. Catalyst BIST MOI

**Resource Requirements:**
- SATA Tee for testing of PUTs without support of disconnects.
- **Stimulus Tool:** Any device or system capable of:
  i. Generating SATA OOB, negotiate speed and bringing the PUT to a state where it can receive a BIST Activate FIS.
  ii. Generating the required BIST Activate FIS for BIST L mode.

**Examples of Stimulus Tools:**
- The BERTScope with a BERTScope SATA Tee and a USB-to-SATA adaptor (for test of HDD or ODD) or a HDD (for test of Hosts).
- Intel ICH7 based computer with NazBIST
- Intel ICH7 based computer with U-Link DriveMaster 2006 software version 3.0.198e or later.
- SCT-BIST Drive
- Serial ATA Protocol Analyzer
  a. Catalyst
  b. Finisar
  c. CATC

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**Discussion:** The BERTScope acts as a monitoring tool fully capable of verifying the patterns transmitted by the PUT and merely need a stimulus tool to generate SATA OOB, negotiate speed and bring the PUT to a state where it can receive a BIST Activate FIS in according to section 10.3.9 of the Serial ATA revision 2.5.

**Test Setup:** Stimulus Tool with an iSATA cable.

**Test Procedure:**
1. Connect PUT to the Stimulus Tool using the SATA cable (via the SATA Tee if the PUT is without support of disconnect).
2. Make sure that the Stimulus Tool is turned on and ready.
3. Allow the PUT to power up and go through OOB.
4. Initiate speed negotiation using the Stimulus Tool if change of speed is required.
5. Generate a BIST Active FIS with the appropriate bits set for BIST L as required using the Stimulus Tool. This might be done using a BERTScope.
### 10.3.9 BIST Activate - Bidirectional

<table>
<thead>
<tr>
<th></th>
<th>Reserved (0)</th>
<th>Pattern Definition</th>
<th>R</th>
<th>R</th>
<th>R</th>
<th>PM Port</th>
<th>FIS Type (58h)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td></td>
<td>Data1 [31:24]</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Data1 [7:0]</td>
</tr>
<tr>
<td>2</td>
<td></td>
<td>Data2 [31:24]</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Data2 [7:0]</td>
</tr>
</tbody>
</table>

#### Figure 197 – BIST Activate - Bidirectional

**Field Definitions**

- **FIS Type**: Set to a value of 58h. Defines the rest of the FIS fields.
- **PM Port**: When an endpoint device is attached via a Port Multiplier, specifies the device port address that the FIS should be delivered to or is received from. This field is set by the host for Host to Device transmission and this field is set by the Port Multiplier for Device to Host transmission. Endpoint devices shall set this field to 0h for Device to Host transmissions.
- **R**: Reserved – shall be cleared to zero.

#### Pattern Definition

- **F**: Far End Analog (AFE) Loopback (Optional)
- **L**: Far End Retimed Loopback* Transmitter shall insert additional ALIGNn primitives
- **T**: Far end transmit only mode
- **A**: ALIGNn Bypass (Do not Transmit ALIGNn primitives) (valid only in combination with T Bit)
- **S**: Bypass Scrambling (valid only in combination with T Bit)
- **P**: Primitive bit (valid only in combination with T Bit) (Optional)
- **V**: Vendor Specific Test Mode. Causes all other bits to be ignored

**Data1**: Dword #1 of data information used to determine what pattern is transmitted as a result of the BIST Activate FIS. Applicable only when the T bit is set to one.

**Data2**: Dword #2 of data information used to determine what pattern is transmitted as a result of the BIST Activate FIS. Applicable only when the T bit is set to one.

#### Example Using the U-Link Stimulus Tool:

1. Start the U-Link program
2. Click “Power Up” and observe the power supply spin up. Leave it on.
3. Click “CtlSATA”
4. Click COMRESET and observe that COMRESET was received on the log on the right side of the DriveMaster window.
5. Select the appropriate data rate “1” or “2” and observe that the “RDSTATUS” displays “00000113” or “00000123” for 1.5 Gb/s and 3 Gb/s respectively.
6. Select the “BIST mode L” for RSG Testing
7. Click “BIST” and observe that “BIST FIS SUCCEEDED” is displayed in the lower left corner of the SATA Control Panel.
8. PUT should now be ready for test.

#### Possible Issues:

Some PUTs may require sequences of ALIGN words to be transmitted when switched from the U-Link initiation to the BERTScope set-up when doing RTL tests. This can be accomplished by using the pattern sequencing on the BERTScope having the A pattern be ALIGNs followed by the B pattern being the desirable test pattern. AB patterns are pre-stored on the BERTScope for this purpose.
Appendix B: Setup

Serial ATA Interoperability Program Unified Test RSG Setup using BERTScope.

Setup including cables and adaptors to have return loss per SATA specifications.

- Serial ATA RSG Receiver Tolerance Setup

  A pair of matched length short SMA Male to SMA Male Cables, Suhner Sucoflex 104 or equivalent Instrument Outputs (SATA Tee) ➔ Data Input (CR)

  iSATA receptacle to SMA Female Adapter, Comax H303000202

  A pair of absorptive rise time filters, Pico Second Pulse Labs, 5915-110-100PS, followed by a pair of matched length short SMA Male to SMA Male Cables, Suhner Sucoflex 104 or equivalent. Data Outputs (BERTScope) ➔ Data Input (SATA Tee)

  One medium length SMA Male to SMA Male Cable, Suhner Sucoflex 104 or equivalent Clock Output (CR) ➔ Ext. Clock Input (BERTScope)

  One short SMA Male to SMA Male Cable less than or equal to 12” length, Suhner Sucoflex 104 or equivalent

  Sub-rate Clock Output (CR) ➔ Clock Input (BERTScope)

  A pair of matched length low loss SMA Male to SMA Male Cables of approximately 2 meters length, Suhner Sucoflex 106 or equivalent

  Data Output (CR) ➔ Data Input (BERTScope)
Appendix C: Resource Requirements

Resource Requirements Summary for all RSG tests as covered by this MOI:

- One BERTScope 7500B S or BERTScope 12500B S with software version 10.0 or later
- A BERTScope SATA-Tee
- One clock recovery instrument BERTScope CR 12500A with software version SW 0.9.6 FPGA 2.8 or later
- One iSATA receptacle to SMA Female Adapter, Comax H303000202, H303000204 or equivalent
- One short SMA Male to SMA Male Cable less than or equal to 12” length, Sucoflex 104 or equivalent
- One SMA Male to SMA Male Cable approximately 24” length, Sucoflex 104 or equivalent
- Two pairs of matched length short SMA Male to SMA Male Cables, Suhner Sucoflex 104 or equivalent
- A pair of matched length low loss SMA Male to SMA Male Cables of approximately 2 meters length, Suhner Sucoflex 106 or equivalent
- Four SMA Male to SMA Male Adapters, SUHNER 32SMA-50-0-1 or equivalent
- A pair of absorptive rise time filters, Pico Second Pulse Labs 5915-110-100PS or equivalent
- One BIST initiation tool as per Appendix A

Last Modification: July 23, 2007
## Appendix D: Accuracy

Measurement Accuracy:

The following Table highlights some of the measurement and instrumentation uncertainties related to the RSG tests.

<table>
<thead>
<tr>
<th>Test #</th>
<th>Measurement</th>
<th>Accuracy</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>RSG-01</td>
<td>TJ Calibration</td>
<td>+/-(((0.2)^2 + (0.2)^2) ps = +/-0.28 ps</td>
<td>Time delta on left and right CDF</td>
</tr>
<tr>
<td>FER</td>
<td>TJ Calibration</td>
<td>+/-(((0.2)^2 + (0.2)^2) ps = +/-0.28 ps</td>
<td>Depends on test time</td>
</tr>
<tr>
<td>RSG-02</td>
<td>TJ Calibration</td>
<td>+/-(((0.2)^2 + (0.2)^2) ps = +/-0.28 ps</td>
<td>Time delta on left and right CDF</td>
</tr>
<tr>
<td>FER</td>
<td>FER</td>
<td>TBD% Confidence</td>
<td>Depends on test time</td>
</tr>
</tbody>
</table>
Appendix E: Host Worst Port Identification

**Purpose:** Prior to execution of any testing on a host, a “worst port” must be identified. The “worst port” identified during a Pre-test should be used. If pre-test has not yet been run then the following method, which follows and complies with the pre-test “worst port” identification procedure, is applied prior to execution of any testing on a host.

**Resource Requirements:**
- One BERTScope 7500 or BERTScope 12500 with software version 10.0 or later
- One clock recovery instrument BERTScope CR 12500A with software version SW 0.9.6 FPGA 2.8 or later
- One iSATA receptacle to SMA Female Adapter, Comax H303000202, H303000204 or equivalent
- One short SMA Male to SMA Male Cable less than or equal to 12” length, Sucoflex 104 or equivalent
- A pair of matched length short SMA Male to SMA Male Cables, Suhner Sucoflex 104 or equivalent
- A pair of matched length low loss SMA Male to SMA Male Cables of approximately 2 meters length, Suhner Sucoflex 106 or equivalent.

**Last Modification:** April 26, 2007

**Discussion:** The intent of identifying a worst port is not to validate each port to the specification, but to simply identify the worst port based on a single relative jitter measurement across all ports within a host. The Interoperability Tests must then be executed on the worst port identified per the procedure below.

**Test Setup as shown in Appendix B:** Connect the CR 12500A sub-rate clock output to the BERTScope clock input using the short SMA Male to SMA Male Cable. Connect the Data Output + and - ports of the CR 12500A to the Data Input + and – ports of the BERTScope using the matched pair of cables. Connect both of the B+ and B- ports of iSATA receptacle, these are the pins marked 6 and 5 respectively, to SMA Adapter via the short matched pair of SMA Male to Male Cables to the respective CR 12500A Data Input + and - ports.

**Test Procedure:**
1. Power-on host and ensure test ports are enabled & functional. Run the following on each individual port.
2. Connect a 3.0 Gb/s device, i.e. HDD or ODD or device emulator, and complete OOB sequence
3. Connect the host to the iSATA receptacle
4. Execute TSG-09 per SATA_MOI_BERTScope_PHY_TSG_OOB_r12_v0_8 if the PUT is transmitting at 1.5 Gb/s or TSG-11 per SATA_MOI_BERTScope_PHY_TSG_OOB_r12_v0_8 if the PUT is transmitting at 3.0 Gb/s while the host is in NRZ idle following OOB and record results for the Total Jitter (TJ) for each port

**Observable Results:**
- The “worst port” is identified as that which has the highest TJ value recorded on the measurement above