Design Guide for the Control of ESD in the eSATA Interface

Pat Young
Principal Engineer
Silicon Image, Steelvine Storage Products

Scope

This document is an informative design guideline only. It is intended to provide general information for the control of ESD energy in the eSATA interface. The regulatory agency test information is based on current requirements for consumer ITE equipment as of the date of publication. The example configurations and component ESD performance values cited are not exactly defined parameters. They are provided as examples of working eSATA systems that meet international agency requirements for ESD performance. It is entirely possible that eSATA systems utilizing more sensitive components can be designed to meet most requirements for ESD performance. Conversely, it is also possible that systems with more robust components would fail in poorly designed configurations.

1. Standard Circuit Models for Performing ESD Tests

The following describes some standard test models typically used to simulate actual ESD events. These models are used to characterize the ESD resiliency of both components and systems. Components can be classified based upon ESD sensitivity to one or more models. Complete operational systems are normally classified using only the Human Body Model.

Human Body Model

The human body model (HBM) is used to simulate discharge events from the human body into a device or system under test, at various potentials. It is essentially a high-voltage potential stored on a small capacitance and switched into the test probe through a fixed source resistance (typical ESD test equipment uses 150pF through 330Ohms). This is the test model used to assess the resiliency of a fully assembled running system under normal usage and is therefore appropriate for qualifying a host *and* device communicating over the eSATA interface. The human body model is the oldest and most widely recognized ESD test model. It is the model used for specifying the acceptable limits for ESD performance of eSATA and similar ITE equipment per EN55024-4-2.

Machine Model

The Machine Model (MM) simulates a worst-case ESD event between a physically large, charged conductive object (tool, fixture, work stool, chair, or cart) and the device or system under test at various potentials. This model is commonly used to test the ESD resiliency of individual components or systems by simulating what they may be exposed to during assembly or during normal service. The actual difference from the human body model is that the machine model has more capacitance (several hundreds of pf) to store the charge, and the machine model has no source resistance. For accuracy and consistency, the machine model specifies a source inductance. With this lower source impedance, the energy and current transferred in these tests can be very large. These tests are mostly performed in specialized test fixtures with very accurate repeatability.

Charged Device Model

The Charged Device Model (CDM) simulates the ESD event when a charged device (under test) is rapidly discharged to ground. This test is generally a component test used to simulate ESD events that occur when a device acquires a charge during assembly or service and is suddenly discharged. A component can acquire a charge, for example, after sliding through a charged tube or coming into contact with a charged assembly fixture. The amount of charge energy stored in the device is a function of the device body-to-ground plate capacitance in the test fixture. Therefore, for a given voltage, the discharge energy in these tests is generally lower than the Machine Model. The capacitance is typically very small, (about 10 pf) and has a very low source resistance (approximately 1 ohm). These

tests are mostly performed in specialized test fixtures with very accurate repeatability.

2. Component Qualification

Good PCBA design will deflect a substantial portion of ESD energy away from fragile semiconductors. However, even under the most ideal conditions, a percentage of the ESD energy will be dissipated by the interface circuitry. Choosing quality components is essential to designing reliable systems.

Component Test Standards

Components should ideally be characterized using all three models. However, it is critical that interface components directly exposed to the outside, like eSATA PHY pins, are tested to reliably operate in the external environment. Reliable eSATA products can be made from PHYs tested to the following levels:

- 2KV minimum for the HBM (JEDEC JESD22-A114-B)
- 200V minimum for the MM (JEDEC JESD22-A115-A)
- 500 to 1KV for the CDM (JEDEC JESD22-C101-A)

These values above are suggested as a general guideline, not a hard requirement. Components that are used in better designed systems may operate safely at lower values.

In general, components used *only* inside of a product have limited ESD exposure and may be tested to lower voltages. This is why a disk drive not specifically designed for eSATA use ***must have an eSATA buffer*** on the data interface.

3. Consumer ITE Equipment ESD and EFT Test Standards

The applicable ESD test standard for consumer ITE equipment is EN55024-4-2. This standard lists the performance ***criteria*** for the minimum acceptable levels for ESD sensitivity. Products must meet EN55024 performance criteria A or B only.

- Performance Criteria A is no operational disruption at all.
- Performance Criteria B products may exhibit momentary disruptions as long as they recover without operator intervention.
- Performance Criteria C is an error condition that requires operator intervention to correct.
- Performance Criteria D is a product failure.

The applicable EFT test standard for consumer ITE equipment is EN55024-4-4. This standard lists the performance criteria for the minimum acceptable levels for EFT sensitivity for this kind of product. Products must meet EN55024-4-4 performance criteria A or B only, (same criteria as above).

These tests are required to obtain the CE mark for products sold in the European Union. While the United States has no *legal requirement* for ESD and EFT immunity for consumer ITE equipment, good design practices for reliable equipment dictate this as a minimum acceptable level.

a. EN61000-4-2 ESD Test Procedures

The actual ESD test *procedures* are called out by EN61000-4-2. The following is a brief summery of the tests. Please refer to the actual specification for more detailed information.

Direct Discharge

Direct discharge tests are induced *after contact* with a pointed ESD probe at various conductive surfaces of an operating system. The sharp probe simulates a tool in a charged human hand. This test is only applied to only those areas that are accessible to persons during normal use. ESD test voltages are increased in 1KV steps from the minimum to the maximum voltage to determine the threshold of failure. Tests are performed at least 25 times in both polarities up to 4KV for consumer ITE products.

Air Discharge

Air discharge tests are performed by bringing a pre-charged, round (finger shaped) probe close enough to various points of a running system to facilitate an ESD arc. Tests are performed at least 10 times in 1KV or 2KV steps to determine the threshold of failure. Tests are conducted in both polarities up to 8KV for consumer ITE products.

Indirect Discharge in the Horizontal Coupling Plane

Indirect discharge tests are used to simulate an ESD event in close proximity to a horizontal surface the system is on, such as a metal desk or shelf. The test is performed with the system under test placed on a 1mm insulator over a metal plate where the ESD events are induced. 50 ESD pulses are generated using HBM direct discharge at a distance of 10cm from all four sides of the product under tests. Tests are performed at 2KV and 4KV for consumer ITE products.
Since the product under test is insulated from the metal plate where the ESD events occur, any energy coupled to the product will be field-induced only, H-field, (magnetic), and E-field, (electric).

Indirect Discharge in the Vertical Coupling Plane

Vertical plane tests are used to simulate an ESD event in a vertical conductive surface in close proximity to a running system, such as a filing cabinet. Tests are performed by inducing 50 ESD events in a metal plane 10cm away from the system under test, on all four sides. Tests are performed at 2KV and 4KV for consumer ITE products.
Since the product under test is insulated from the metal plate where the ESD events occur, any energy coupled to the product will be field-induced only, H-field, (magnetic), and E-field, (electric).

b. EN61000-4-4 Electrical Fast Transient / Burst Test Procedure

The actual EFT test *procedures* are called out by EN61000-4-4. EFT testing is a related test that gauges a given system's sensitivity to voltage anomalies on the external connections. The test pulses are 5 kHz for 15ms with a period of 300ms. The pulses are 50ns long and have a rise time of 5ns.

I/O cables less than 3 meters are not tested. Therefore, a device with a 2-meter eSATA interface is limited to testing the power supply and any additional cables greater than 3 meters. Power supply connections are tested to 1KV. I/O cables greater than 3 meters or DC power supply inputs are tested using 500V pulses through a 1-meter capacitive clamp to couple the test bursts into the I/O cable.

4. Ground Configuration for eSATA

Like other external standards, the eSATA interface uses a protective shield electrically isolated from signal grounds and a shield around the signal conductors. The shield provides a low impedance path for EMI causing, common-mode current and ESD energy. This does not imply that products using eSATA must completely isolate the signal and chassis ground internally. However, *the way* they are connected is extremely important for preventing ESD damage (see PCB design examples below).

> *Note that because of the limited distance for eSATA, there is no requirement to totally isolate the chassis and signal grounds. Other interfaces (like RS-232) capable of 1000ft or more must isolate the grounds to prevent any current on the shield from flowing on the signal ground. This shield current happens when a shielded cable is connected between buildings at different AC ground potential.*

The amount of ESD energy imparted to the system under test is a function of the impedance to AC ground. If the enclosure is made entirely of plastic or some other insulator it may be impossible to actually cause an ESD discharge. This would obviously improve the products chances of surviving ESD testing, but may not be the best scenario to prevent EMI. If the system has *no connection to AC ground anywhere*, its capacity to discharge ESD energy is greatly diminished and therefore it may be difficult to create a discharge event during testing. In any case, the energy level of a discharge event will be lower than a similar device with a direct AC ground connection. (Note: controlling ESD and EMI *without any* AC ground connection can be very difficult).

ESD events occurring near the AC ground connections are easily controlled with good PCB design. However, ESD events induced at the opposite end of an eSATA connection from the AC ground connection must rely on the eSATA cable shield to conduct the ESD energy without sending destructive energy into the signals or signal grounds. This is the worst-case situation since the ESD energy has the entire length of the eSATA cable to couple to the signal or signal ground conductors. It is imperative that the shield ground has far lower impedance to AC ground than the signal grounds.

5. Power supply Configurations for eSATA

When a device or host enclosure has a direct connection to the AC ground via a three-wire AC plug, keeping the impedance low on the ESD discharge path is relatively simple. Because the eSATA interface can be used on an ungrounded laptop or an external disk drive with an ungrounded power supply, a direct or even an indirect AC ground path may *not be available*.

a. Example Configurations

Let's consider an example case of a single disk drive connected to a desktop computer thru a PCI-based HBA. If the single drive enclosure has an AC ground, any ESD pulse introduced to the drive enclosure will seek this low impedance path.

However, many external single-drive solutions use low-cost wall transformer power supplies that do not have an AC ground connection. Since the impedance to AC ground in this type of power supply is quite high, any ESD pulse introduced to the single-drive enclosure will instead travel down the shield of the eSATA cable to the desktop PC's chassis ground. If the impedance to AC ground through the signal ground connections is low with respect to the AC or chassis ground, then some of the ESD energy will flow into the signal ground pins of the SATA devices. If the impedance to AC ground through the signal ground pins is only $1/10^{th}$ the impedance to AC ground on the shield, then a significant portion of the energy from the ESD pulse will flow through the signal ground pins.

The key to diverting energy away from fragile semiconductors is to ensure that the AC ground impedance is much lower than the signal and signal ground impedance path. If *no* AC ground connection exists, it may be difficult or impossible to cause a discharge event during testing. In any case, because of the high impedance discharge path, the amount of energy will greatly be reduced.

i. Grounded External Disk Drive to Desktop PCI HBA

In this configuration, both ends of the eSATA cable have a direct path to AC ground. This is the best possible scenario since, regardless of where the ESD event occurs, little ESD energy will flow down the eSATA signal conductors.

ii. Ungrounded External Disk Drive to Desktop PCI HBA

This device configuration will usually have high impedance to AC ground through the power supply. In this situation, the eSATA port shield or chassis ground should be isolated from the signal grounds by a gap or moat, (see section 6). If the chassis and signal grounds are shorted together, ensure that the impedance from the chassis to the eSATA shield is much lower than the impedance from the chassis to the signal grounds.

iii. Ungrounded External Disk Drive to Laptop

This ground configuration presents some special challenges for ESD control since there is *no* connection to AC ground. The power-supply AC connections will still have some finite impedance to AC ground. Assume the impedance is very high and create large clearances between the chassis ground and signal ground. The chassis ground section of the eSATA connector should be isolated from the signal ground section by a large moat. If the chassis and signal grounds are connected together, make the connection close to the power input connection, as far as possible from the eSATA IC.

6. PCB Layout Considerations for eSATA Interface

Correct separation of the signal and shield grounds is required to isolate the ESD energy. This separation is a physical gap between *all* the planes on a PCB with no traces crossing and is commonly referred to as a moat. The AC and signal grounds can be shorted together, but only *after* the main AC ground connection point. The following examples are from actual products designed to meet all international regulatory requirements.

Figure 1 below is a portion of a PCI-X HBA with two eSATA ports. Note the large moat between the chassis ground plane and the signal ground plane. These two planes are shorted together at a single point by a SMT zero Ohm resistor near the top PCI bracket-mounting hole. This connection point is used because it is the closest to the PCI bracket mounting screw, which will have the lowest impedance to the Chassis AC ground connection. ESD energy on the eSATA cable will seek the chassis ground connection rather than the highly inductive path through the zero Ohm resistor and the signal ground plane. Do not use a thermal relief on this mounting hole as it will raise the impedance of this connection.

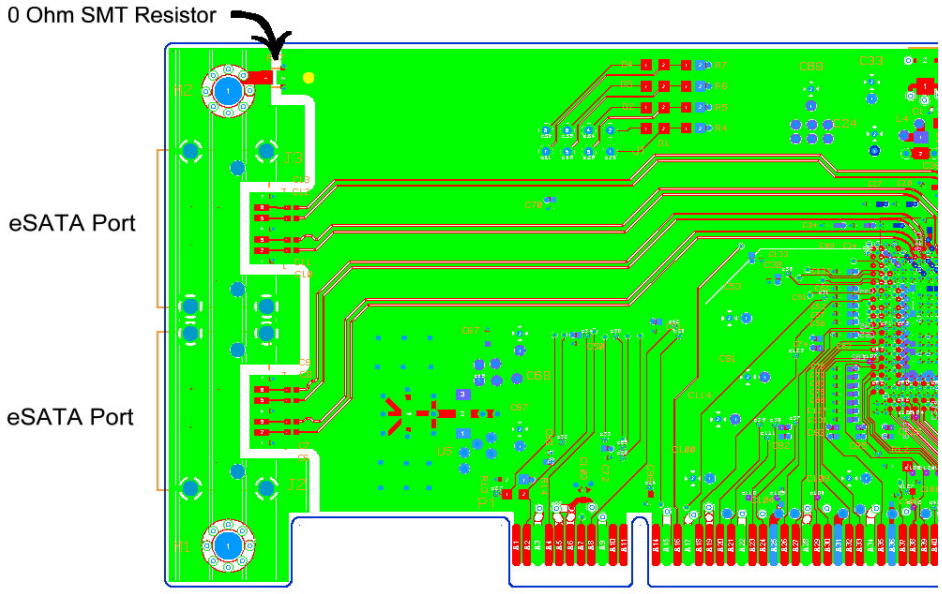

Figure 1

Figure 2 below shows identical moats cut through the power plane of the same HBA. This technique is used to completely isolate the chassis ground section of the PCB. ESD energy can easily jump between planes that are not adequately physically isolated. According to MIL-P-13949/4C for FR4 material, the average dielectric strength (perpendicular to laminations) is 750V per mil (.001") minimum (29.25 KV per mm). This value should be de-rated at least 25 to 50% to allow for material tolerances.

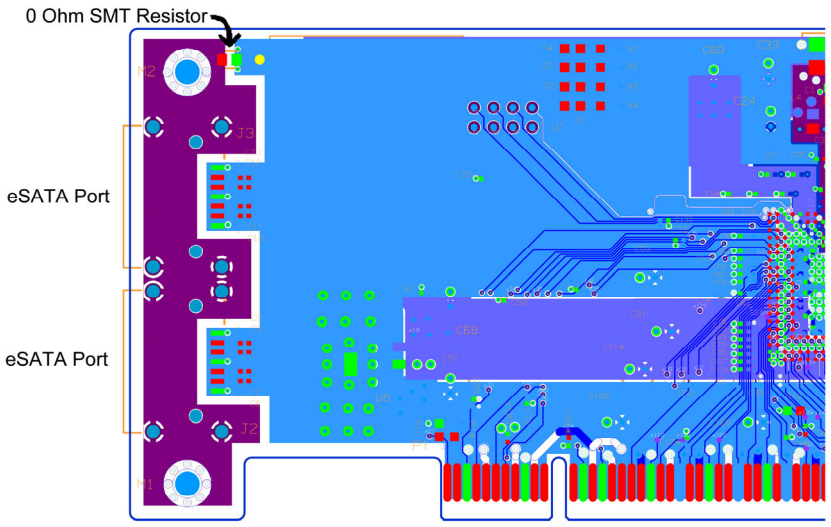

Figure 2

Figure 3 below shows a small section of the PCB isolated by a moat. As in the previous examples, this moat separates the shield and signal ground on an eSATA port. The large hole at the bottom (labeled M4) is a mounting hole tied to a metal chassis. This product uses an ATX-type PC power supply equipped with a grounded AC receptacle. This means that this mounting hole has very low impedance to AC ground for conducting ESD energy. (Do not use a thermal relief on the chassis ground connection hole). The mounting hole has a SMT 0 Ohm resistor to connect the signal ground to the chassis ground at this one point, sometimes called a Mecca ground. The signal ground has no other connection for ESD energy to flow so the ESD energy is routed into the chassis, away from the eSATA port IC.

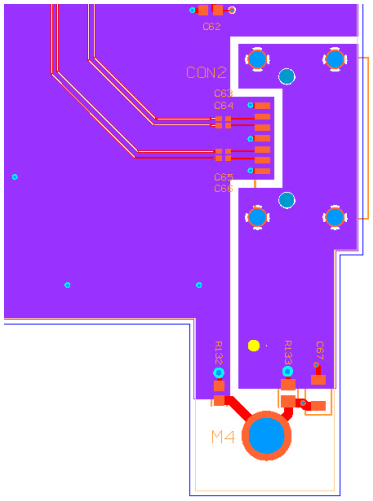

Figure 3

Figure 4 is from a product that uses an ungrounded "floor wart" power supply that supplies regulated DC directly to the eSATA device. Notice that the shield and signal grounds are shorted together by a 0 Ohm SMT resistor *on the far side of the power input connection*, away from the eSATA port.

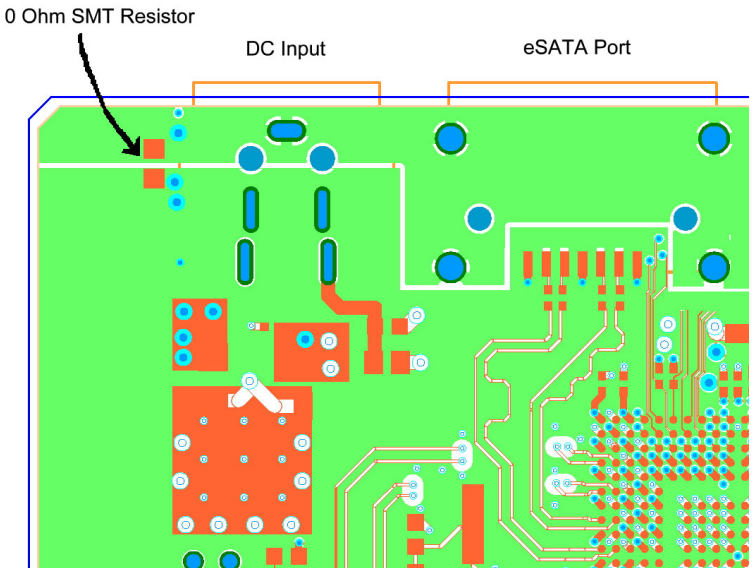

Figure 4

In all the previous examples, the connections between the chassis ground and signal ground is facilitated by a zero Ohm SMT resistor. This component is used instead of a direct trace connection to ground for two reasons:

- The small amount of case inductance of the SMT package helps to filter the very fast rise-time ESD bursts
- The value of the SMT device can be changed for tuning the response time of this connection

Note: To raise the inductance of this connection, an actual bead inductor can be used instead of the zero Ohm resistor. This connection is also the point where EMI causing common mode current is shunted to ground. Be careful not to significantly raise the high frequency impedance of this connection as it will adversely effect EMI emissions. While using an actual resistor may improve ESD immunity, the impedance increase in the signal ground path would *significantly increase* EMI emissions.

Proper impedance control of the PCBs and the eSATA connections will improve both EMI and ESD performance. Other parameters like the size, number and high frequency response of the signal ground connections, may be inversely related and must be balanced between effective EMI shielding and adequate ESD protection. These parameters are very dependent on the particular implementation.

7. Quality Considerations

eSATA PHY Selection

Selecting quality PHY components designed to survive the ESD levels at an external interface is the first step. ESD diodes large enough to survive use on an external interface are usually much larger and are highly capacitive. Designing a PHY to operate correctly with this additional capacitive load requires special characteristics that are normally not found on internal SATA interfaces. Never directly connect a device not specifically designed for eSATA use directly to an eSATA port.

PCB Quality

A significant drop in the SATA bus impedance can create structure for ESD conduction and a significant source of EMI causing common mode current. The most common source of impedance errors in most SATA implementations is the PCB itself. Carefully control the impedance on your SATA bus, and match the SATA trace lengths. Use the smallest SMT component package practical for the DC isolation capacitors on the eSATA ports. Also, cut out the ground plane under the isolation capacitors to compensate for the drop in impedance caused by the wider component pads. Always insist on PCB test coupons and verify them, (and some sample PCBs) on a TDR.

eSATA Cables

Once the PCB quality and layout considerations are addressed, the most important factor in surviving an ESD event is very-low shield impedance on the eSATA cable, (DC resistance of the shield is a good indicator of impedance). The shield termination at the connectors must be very low resistance and mechanically reliable to keep ESD energy off the signal grounds, regardless of the configuration. Low shield impedance will also significantly reduce EMI emissions.