Successful SATA 6 Gb/s Equipment Design and Development

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Abstract:

The new SATA Revision 3.0 enables 6 Gb/s link speeds between storage units, disk drives, optical and tape drives, and protocol host bus adapters (HBAs). Carrying such high frequency signals up to one meter over copper cables, however, tests the limits of signaling technology. As a consequence, the majority of design concerns are expected to arise at the physical layer.

This whitepaper will describe the technical challenges in maintaining signal integrity at 6 Gb/s and how improper test setups can inadvertently degrade signals during product development and testing. Specifically, developers and systems engineers will learn how to deploy test equipment to minimize its impact on signal integrity. In this way, developers can avoid the time-consuming process of attempting to resolve signal integrity issues that are ultimately the result of improper testing practices.

The introduction of SATA 6 Gb/s promises new levels of performance for networks. At these higher speeds, signal integrity becomes a significantly more important design concern for equipment designers and network engineers than for SATA 3 Gb/s architectures, as tolerances drop to the point where test equipment can adversely affect signal integrity. For example, a test setup that was operating at the performance edge for 3 Gb/s will cause undesirable and misleading failures at the 6 Gb/s speed.

Apart from strictly adhering to SATA specifications, the key behind successful SATA 6 Gb/s product development and network debug lays an understanding of the tighter tolerances at 6 Gb/s and several simple steps that will minimize the impact of test equipment on the device under test. By understanding how attenuation and jitter impact signal integrity, developers and systems engineers can adjust test setups to minimize their impact during testing.

Attenuation and Jitter

The higher frequency signals used by SATA 6 Gb/s have increased sensitivity to attenuation and jitter. Higher frequencies attenuate faster than lower frequencies over distance (see Figure 1a). Additionally, higher frequencies are more susceptible to jitter as jitter remains constant even while the signal period decreases (see Figure 1b). When attenuation and jitter become too pronounced, the ability to accurately sample and decode signals on the receive-side is severely compromised.

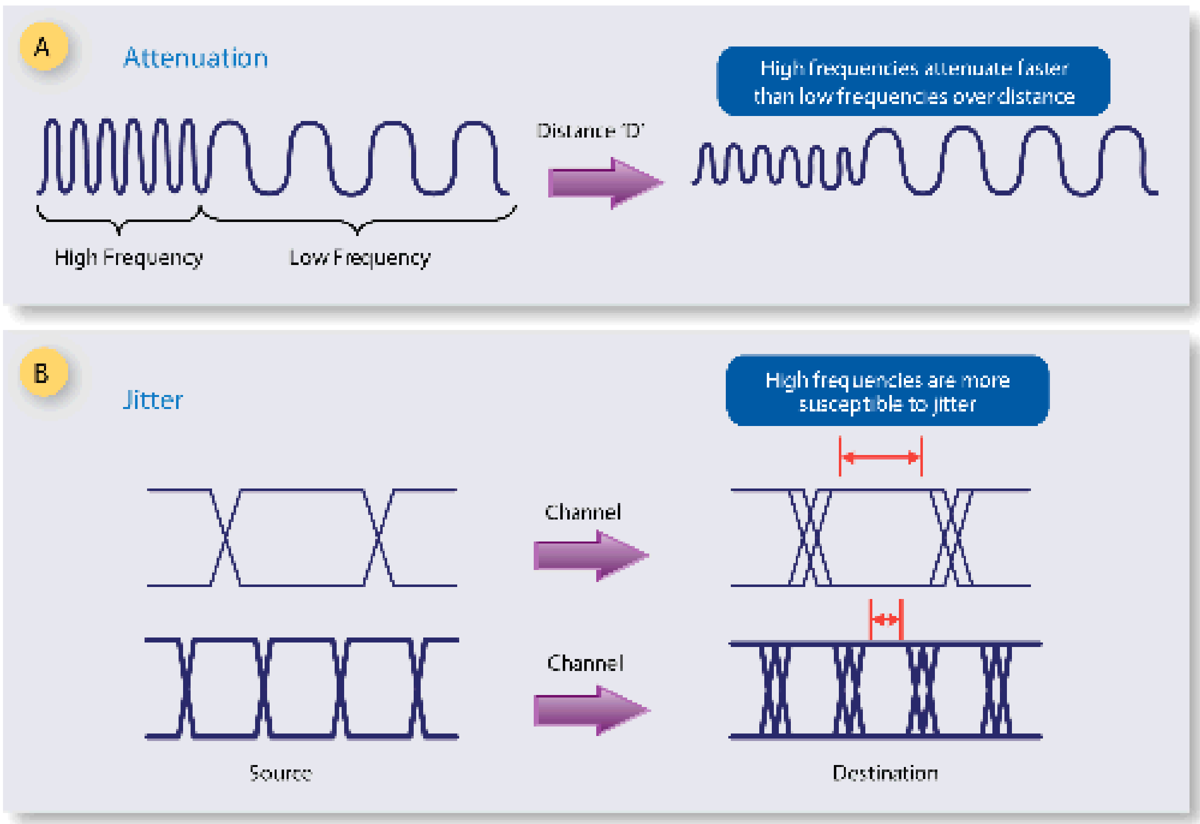

Figure 1: SATA 6 Gb/s signals have increased sensitivity to attenuation and jitter. Higher frequencies attenuate faster than low frequencies over distance (a) and are more susceptible to jitter (b). Proper test setups reduce the additional attenuation or jitter introduced into a system during testing.

Some high-speed communications standards rely upon de-emphasis and equalization techniques to minimize the impact of attenuation and jitter on signal integrity. SATA Revision 3.0 employs neither, thus providing a lower-cost link technology for applications that do not require these capabilities. The lack of de-emphasis and equalization can render SATA 6 Gb/s more susceptible to attenuation and jitter. Testing of SATA 6Gb/s signals with shorter, lower-loss cables than those used to test 3 Gb/s systems is important for this reason.

Connection Methods

While a necessary debugging aide, the insertion of test equipment between devices-under-test introduces electrical discontinuities into the signal path that induce both jitter and attenuation that can adversely affect signal integrity. There are several methods available for connecting test equipment that reduce or compensate for these effects to varying degrees. Users should be aware of the particular advantages and disadvantages of each in order to select the method best suited for their situation.

A. **Analog Passthrough** Some test equipment provides a high-impedance bypass method such as a coupler, pick-off tee, or solid-state switch to pass signals between devices under test. These achieve the lowest impact to signal integrity of the available options (see Figure 2A). While this method keeps induced jitter to a minimum, its primary disadvantage is that it creates a discontinuity in the link, similar in effect to using a connector splice, to join two cables. As a result, the signal becomes attenuated.

B. **Digital Retiming** is a method where test equipment operates as a network device at the link layer. At this layer, the test equipment receives signals that it decodes and re-encodes, then resends to their destinations (see Figure 2B). (For those not familiar with the network stack, devices at the link layer do not receive entire files, for example, but receive and resend network traffic on a frame-by-frame basis.) It is important to note that digital retiming can add latency as well as alter clock-alignment commands at the link layer. For instance, SATA ALIGN characters may be utilized to overcome clock skew between the tester and both the host and target. The tester drops or adds ALIGN characters to maintain clock alignment with the devices under test. Whether a subtle change to network traffic, like the adding or dropping of ALIGN characters, affects testing depends upon the goals of the specific test.

C. **Buffered** or **Re-amplified** connections reduce the attenuation induced by test equipment by electrically amplifying signals (see Figure 2C), thus enabling the use of longer cables and providing the best signal integrity in terms of amplitude, i.e., decreased attenuation. The primary disadvantage of buffering a signal is the introduction of non-deterministic jitter. If the amount of jitter is too high, the advantages of using a buffered approach are lost. Additionally, since buffering entails placement of an electrical circuit in a signal pathway, channel issues such as reflections can be masked.

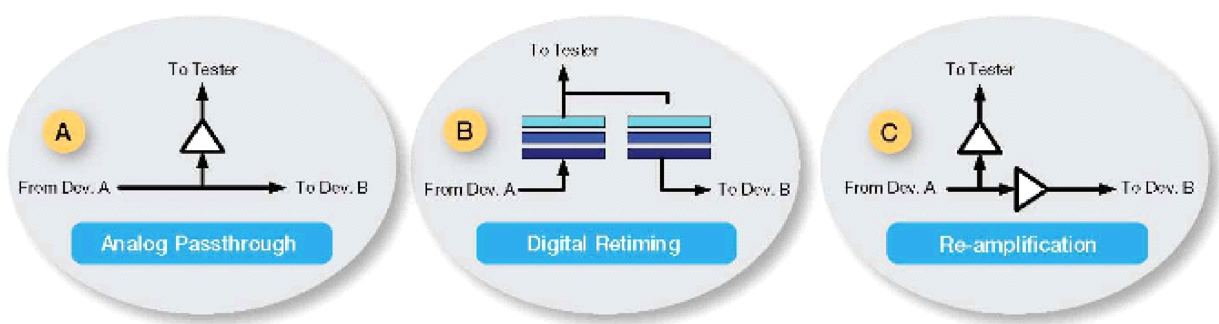

Figure 2: The method used to connect test equipment to the device under test can have a significant impact on signal integrity. Analog Passthrough (a) achieves the lowest impact to the signal's electrical characteristics of the available options by passing signals through a coupler, pick-off tee, or solid-state switch. While keeping induced jitter to a minimum, analog passthrough creates a discontinuity in the link and, as a result, attenuates the signal. A Buffered or Re -amplified connection (c) reduces attenuation to provide the best signal integrity in terms of amplitude, thus enabling the use of longer cables; however, it introduces jitter that can overcome the advantages of using a buffered approach. As it places an electrical circuit in the middle of a link, buffering may mask electrical channel issues such as reflections. Digital

retiming (b) mimics a network device at the link layer, receiving signals, decoding them, re-encoding, and then resending to their destination. Digital retiming can add latency as well as undesirably alter signals at the link-layer, such as adding or dropping align characters

So which method is best? Because analog passthrough tends to have the least impact on the electrical characteristics of a signal, it gives users the most accurate real-world representation of network signals. In some cases, however, analog passthrough, with its characteristic attenuation, fails to maintain sufficient signal amplitude. If attenuation issues arise regardless of the shortness of cable length, i.e., if induced attenuation is discovered to be an issue, a buffered approach may provide better results. Conversely, if long cables are necessary, a buffered connection may eliminate attenuation concerns.

For system designs where there is a high degree of confidence in the physical layer of the network and design concerns are primarily concentrated in the protocol domain, a digitally retimed connection may provide the best results. Digital retiming is also appropriate when a physical setup requires long cables.

Pretesting

An important element of testing is working from a stable foundation. If the network infrastructure has unresolved integrity issues, these may incorrectly appear to be caused by the device under test, thereby complicating or delaying problem resolution. Pretesting of the physical infrastructure (e.g. cables and connectors) before introducing the subject test device can confirm the suitability and reliability of a test setup.

Pretesting before entering into SATA 6 Gb/s device tests is especially important because many test setups were created for 3 Gb/s applications and may not perform well at doubled signal rates. Some previous test setups may also operate narrowly within the tolerance limits of 3 Gb/s systems and will fail if not updated to 6 Gb/s requirements. By first characterizing the speed capabilities of the physical infrastructure between end points, developers can more confidently assume problems found are with the device under test rather than inherent in the test setup.

Using a system test suite to pretest the physical infrastructure is helpful as test patterns specifically designed to test the signal integrity limits of a network are generated. Running a broad spectrum of stress-inducing traffic types across links serves to test both attenuation and jitter tolerances and helps reveal whether the existing physical layer will work at full line rates.

Cabling Issues

A critical element of any test setup is the quality of cables used and how they connect to the analyzer and device under test. Problems arise when cables fail to meet standard specifications or when multiple cables are connected in such a way that discontinuities (e.g. from impedance mismatches in the cable) are introduced.

When standards are under development, a common assumption used in the mathematical models is the use of single cable, particularly one with no connectors or other impedance discontinuities between its endpoints. In practice, however, immediately available cables may be used without consideration that they may be unshielded, longer than necessary, or even configured from a string of multiple interlocking cables. At present only one cable is specified for operation at 6 Gb/s SATA, the internal single-lane SATA cable. And, this cable should be 1 meter or less. However, cables that are compliant with SATA specification revision 2.6 will work at 6 Gb/s; however, if cables beyond 1 meter were used for margin testing at 3 Gb/s, using the same cables at 6 Gb/s may cause indeterminate test results.

Consider the test setup shown in Figure 3. In this example, the signal analyzer generates a signal to the device under test, which is then captured by the analyzer. The original signal is fed back into the analyzer so that both the sent and received signals can be compared.

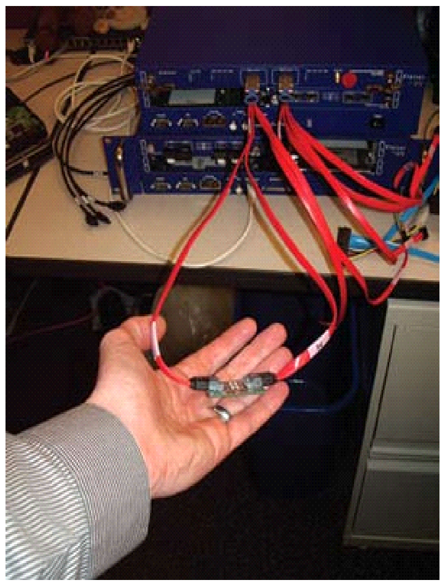

Figure 3: Test Setup to Avoid: Signals are 1) sent over a splice, 2) the extended double cable is longer than required, and 3) the cable used is unshielded.

There are several problems with this test setup. The cable coming out of the back of the analyzer sends the generated signal back to the analyzer across a male-to-male cable segment or "splice". As a result, the electrical characteristics of the link tend to attenuate the signal and appear as an extended length of cable that is much longer than its actual length. Moreover, both the cable and splice shielding are less than that of higher-quality cables, potentially aggravating jitter by this setup.

Compare this to the test setup in Figure 4. A high-quality, miniSATA-to-SATA internal single-lane cable connects the analyzer to the device under test. The cable's length is reasonable (0.5 meters) and it has no discontinuities. With proper signal levels and termination in the host and target, this setup is more likely to provide proper operation.

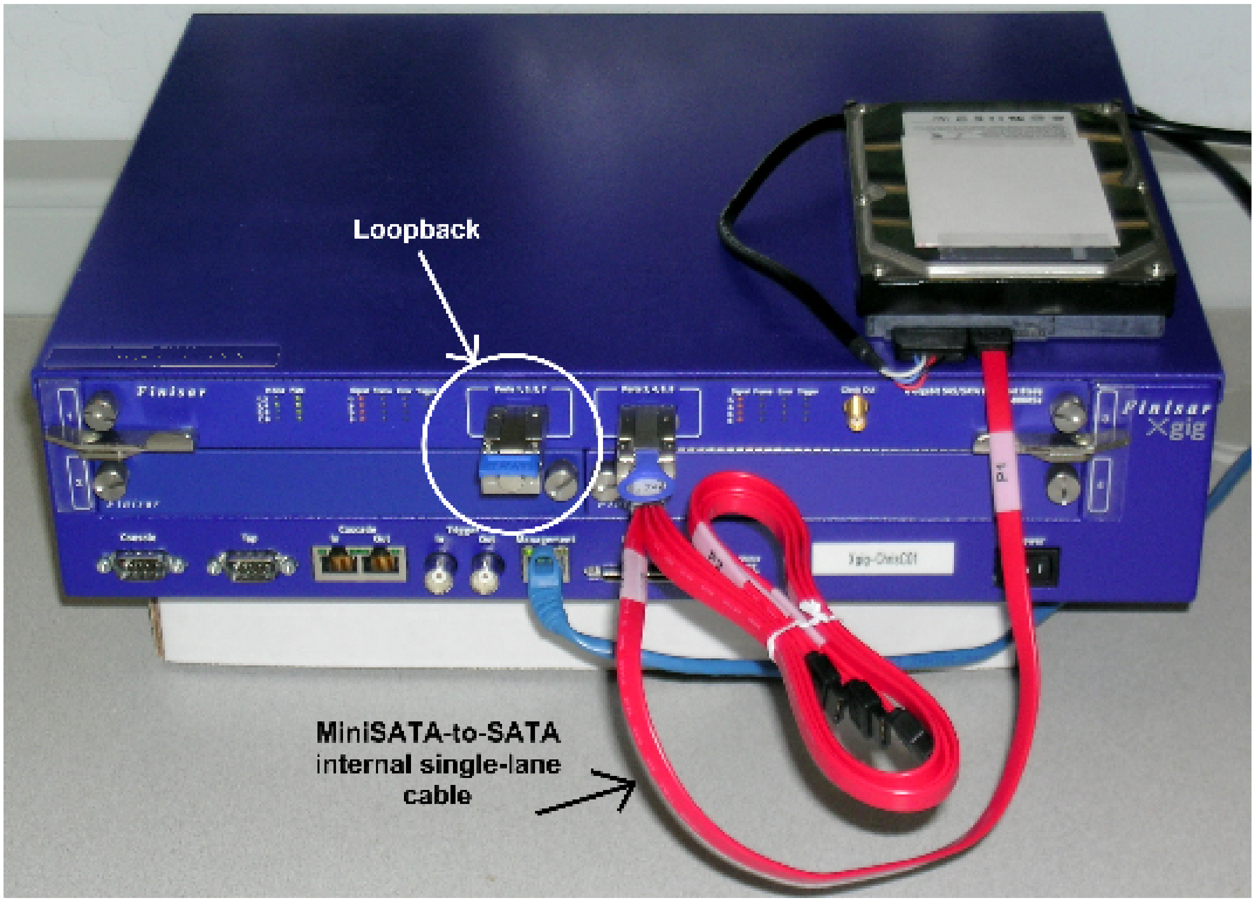

Figure 4: Appropriate Test Setup: Signals are sent over a single cable and the cable is a minimum length, and the setup uses a loopback for looping signals

If looping a signal through a piece of test equipment is necessary, this is best accomplished using a loopback plug, or other suitable short feedback mechanism, which passes the signal over a short (~1 mm) trace of copper, keeping the loop as short as possible, and minimizing the length of discontinuities in the link. (See Figure 4) Every discontinuity (connectors, splices, adapters, etc.) causes reflections that attenuate signals by sending signal energy in the opposite direction and reducing signal integrity. Removal of all but necessary discontinuities is important and can require custom loopbacks, test cabling, or the use of test fixtures such as JBODs.

For the sake of those investigating cables, this paper also includes cable specifications from the SATA specification 3.0 Release Candidate 1 (RC1) in Appendix A. This specification is the working draft of the as yet unreleased 6.0 Gb/s SATA. When completed, SATA specification 3.0 will define the minimum guidelines for cable manufacturers. While this specification's tables are subject to change, and likewise those provided here in the Appendix, the parameters provide an excellent guide when evaluating cables prior to the release of the final SATA 3.0 specification.

Conclusion

This paper has discussed ways developers can improve signal integrity and increase their chances of success when testing 6Gb/s SATA. These points are summarized here:

- **Know and understand your test equipment's connection methods:** The method used to connect test equipment to the device under test can have a significant impact on signal integrity. Know the differences and applicability of Analog Passthrough, Buffering, and Digital Retiming.
- **Use the shortest reasonable cable:** The longer the cable, the greater the attenuation. The best way to reduce attenuation is by shortening cable lengths. For instance, co-locate the analyzer, host, and device under test rather than running long cables between workbenches. This is one of the simplest ways to reduce cable lengths.
- **Use only cables that are compliant with the SATA specification:** Use of inappropriate cables could impact development by introducing 'red-herring' signal integrity issues.
- **Use high-quality shielded cables**: Although more expensive, using high-quality shielded cables can reduce physical layer issues. Unshielded cables can reduce signal integrity, induce jitter through Electro-Magnetic Interference (EMI) and potentially lead to phantom problems.
- **Eliminate all discontinuities:** Every discontinuity (connectors, splices, adapters, etc.) causes reflections that attenuate signals by sending signal energy in the opposite direction and reducing signal integrity. Removal of all but necessary discontinuities is important and can require custom test cabling or the use of test fixtures such as JBODs.
- **Remember the 3 S'es:** use Short, Shielded, and Single cables wherever possible.

Moving to 6 Gb/s increases the difficulty of maintaining signal integrity between network devices. Many signal integrity issues arise from the test setup. The ability to efficiently and accurately identify and resolve protocol system issues is significantly enhanced when the tighter tolerances of operating at 6 Gb/s are observed and appropriate connection methods, system pretesting, and proper cables are employed.

Appendix A: Cable Specifications from the SATA 3.0 Specification, Release Candidate 1

The following tables provide parameters for SATA cabling for the purpose of comparing cables. These tables break the cable varieties into four categories; internal single lane and multilane, external single lane, and external multilane. At present, only the first - internal cables - have version 3.0 (6.0 Gb/s) definitions. However, all other cabling should work at 6.0 Gb/s with suitable source and target signal integrity.

The electrical requirements for internal single-lane and multi-lane Serial ATA cables and connectors.

Parameter	Requirement
Mated Connector Differential Impedance	100 Ohms ±15%
Cable Absolute Differential Impedance	100 Ohms ±10%
Cable Pair Matching Impedance	±5 Ohms
Common Mode Impedance	25 - 40 Ohms
Maximum Insertion Loss of Cable (10-4500 MHz)	6 dB
Maximum Crosstalk, single lane: NEXT (10-4500 MHz)	26 dB loss
Maximum Crosstalk, Multilane: CXT (10 – 4500 MHz)	30 dB loss
Maximum Rise Time	85 ps (20-80%)
Maximum Inter-Symbol Interference	50 ps
Maximum Intra-Pair Skew	10 ps

The electrical requirements for external single-lane cables and connectors.

Parameter	Requirement
Mated Connector Differential Impedance	100 Ohms ±15%
Cable Absolute Differential Impedance	100 Ohms ±10%
Cable Pair Matching Impedance	±5 Ohms
Common Mode Impedance	25 - 40 Ohms
Maximum Insertion Loss of Cable (10-4500 MHz)	8 dB
Maximum Crosstalk: NEXT (10-4500 MHz)	26 dB loss
Maximum Rise Time	150 ps (20-80%)
Maximum Inter-Symbol Interference	50 ps
Maximum Intra-Pair Skew	20 ps

The electrical requirements for the external multi-lane cables and connectors.

Parameter	Requirement
Mated Connector Differential Impedance	100 Ohms ±10%
Cable Absolute Differential Impedance	100 Ohms ±5%
Cable Pair Matching Impedance	±5 Ohms
Common Mode Impedance	25 Ohms - 40 Ohms
Maximum Insertion Loss of Cable (10-4500 MHz)	8 dB
Maximum Crosstalk: CXT (10-4500 MHz)	30 dB CXT
Maximum Rise Time	150 ps (20-80%)
Maximum Inter-Symbol Interference	50 ps
Maximum Intra-Pair Skew	20 ps